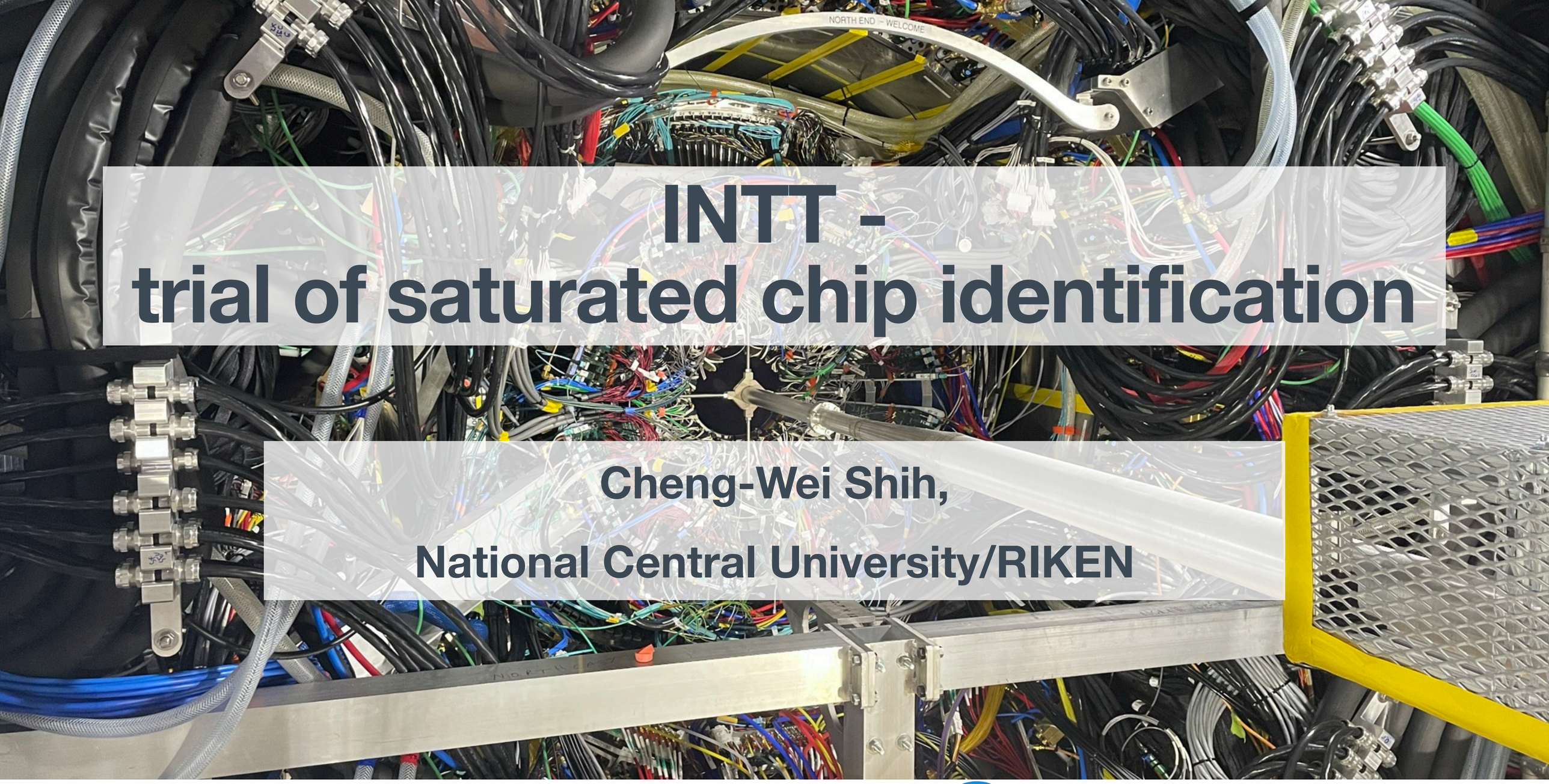

INTT - trial of saturated chip identification

Cheng-Wei Shih,

National Central University/RIKEN

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INTT meeting

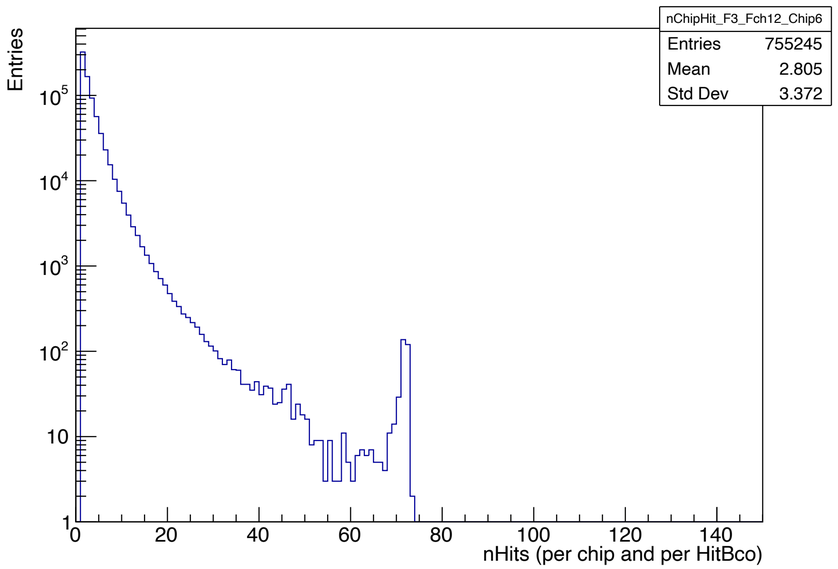
sPHENIX

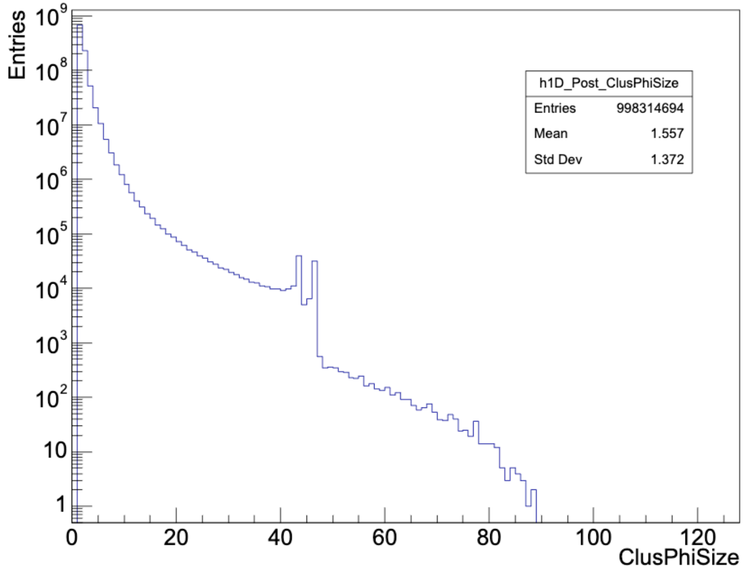
國立中央大學
National Central University

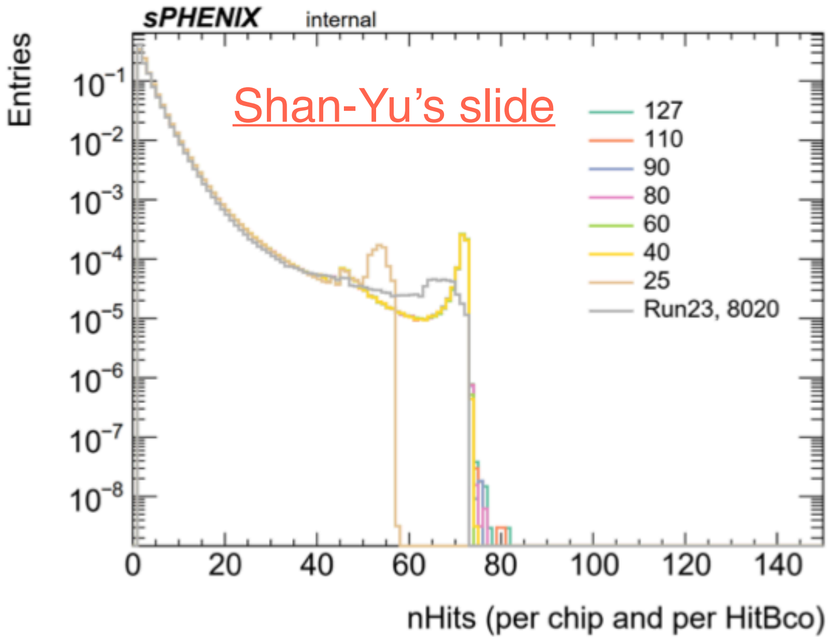
RIKEN

Recap - chip saturation

- A cutoff in chip-hit distribution and a two-spike structure in cluster-phi-size distribution were observed
  - Indication of chip saturation & the two issues are correlated
  - It's a chip-level problem (cannot be resolved by extending the open_time, studied by Shan-Yu)
  - The chip-overflow-flag cannot identify the chip saturation
    - The meaning of the chip-/ROC-overflow-flag is still unclear
  - **It seems NOT a major issue**
    - Ratio of saturated chips < 1% & it's independent of the event activity

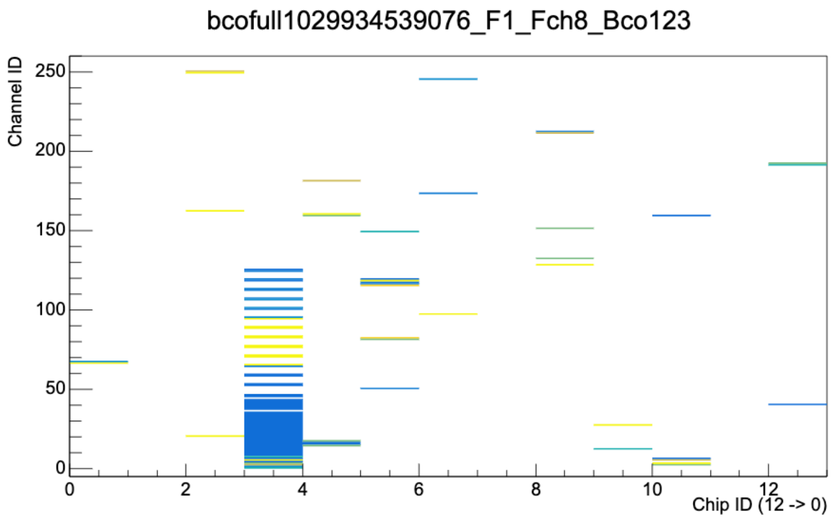


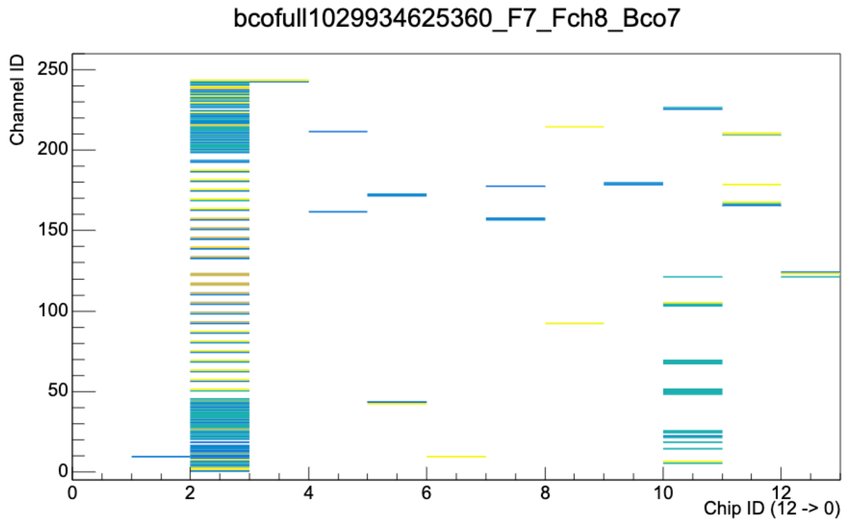


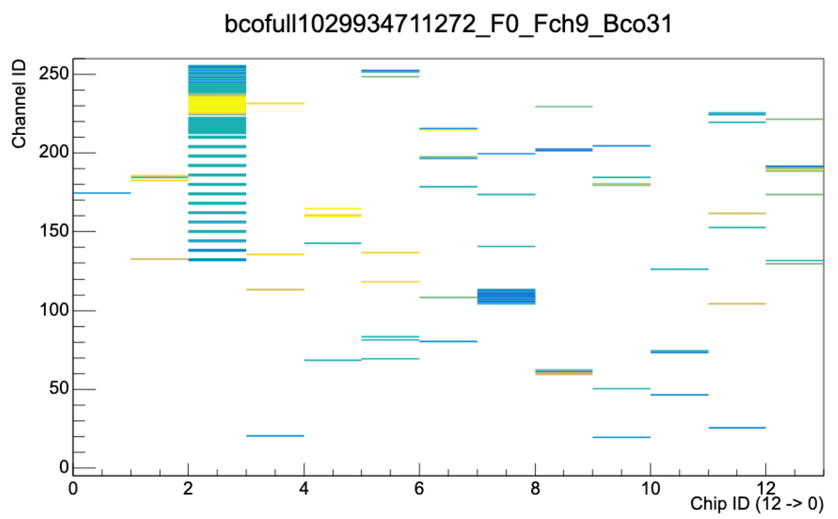


Recap - chip saturation

- Remaining questions
  - Would the chip-saturation issue be relevant to the previous chip activity?
  - Correlation with multiplicity in p+p collisions?
  - Are hits/clusters in the saturated chips real or fake?
  - Any treatments for those hits and clusters?
    - If so, how can those chips be identified?
    - Their patterns could be very diverse (even if disabling the hit adc info.)

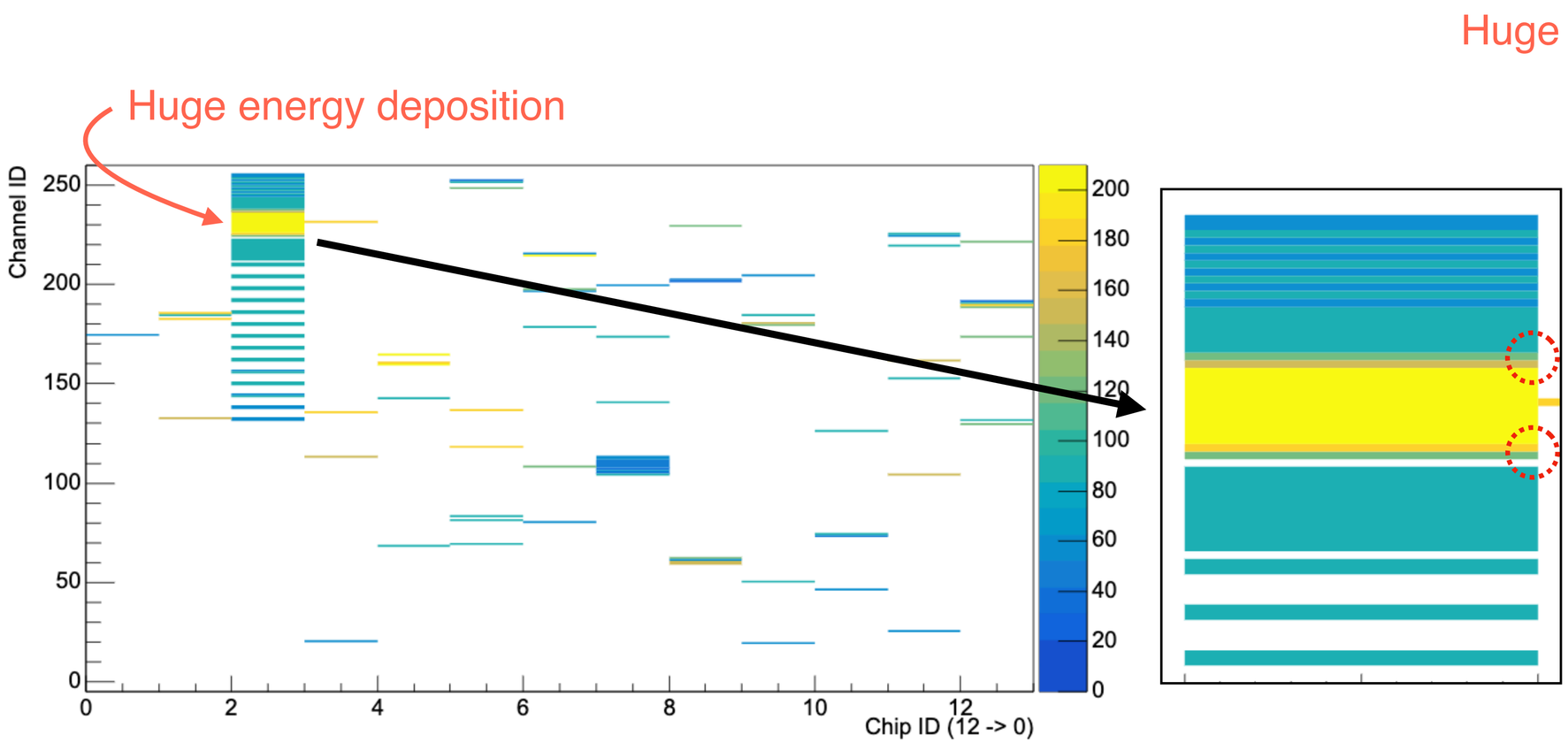


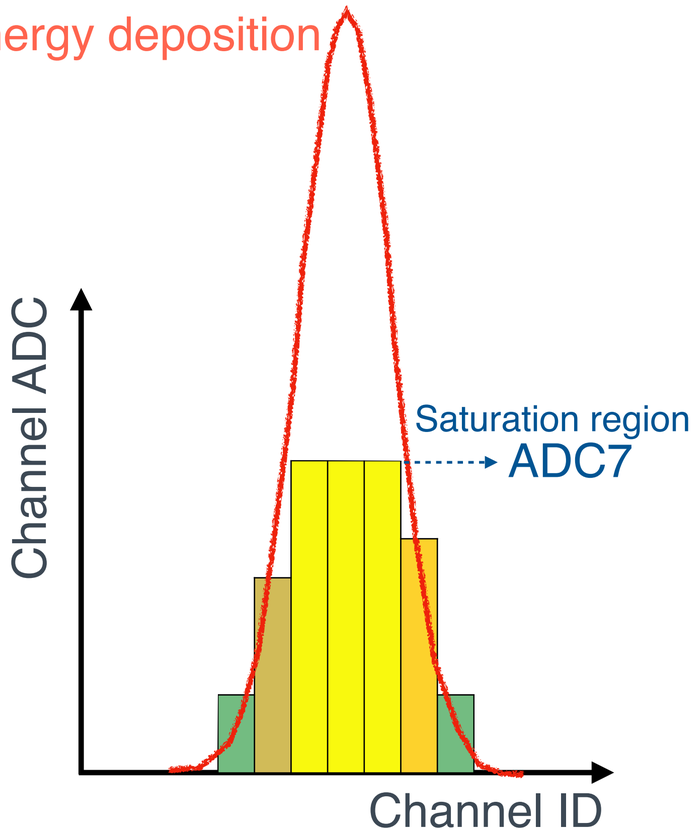




Can those hits be real?

- Pro side:
  - Huge energy deposition leads to a charge cloud large enough to cover the full chip
  - Not a step function when transitioning to the plateau region





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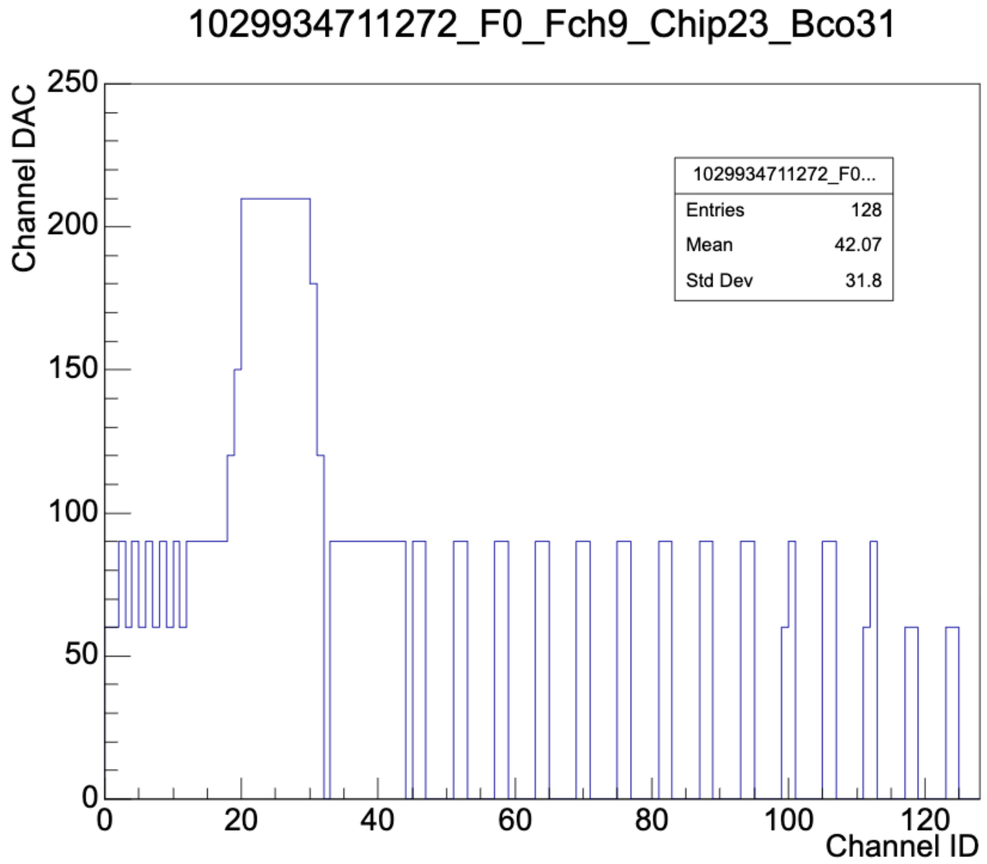

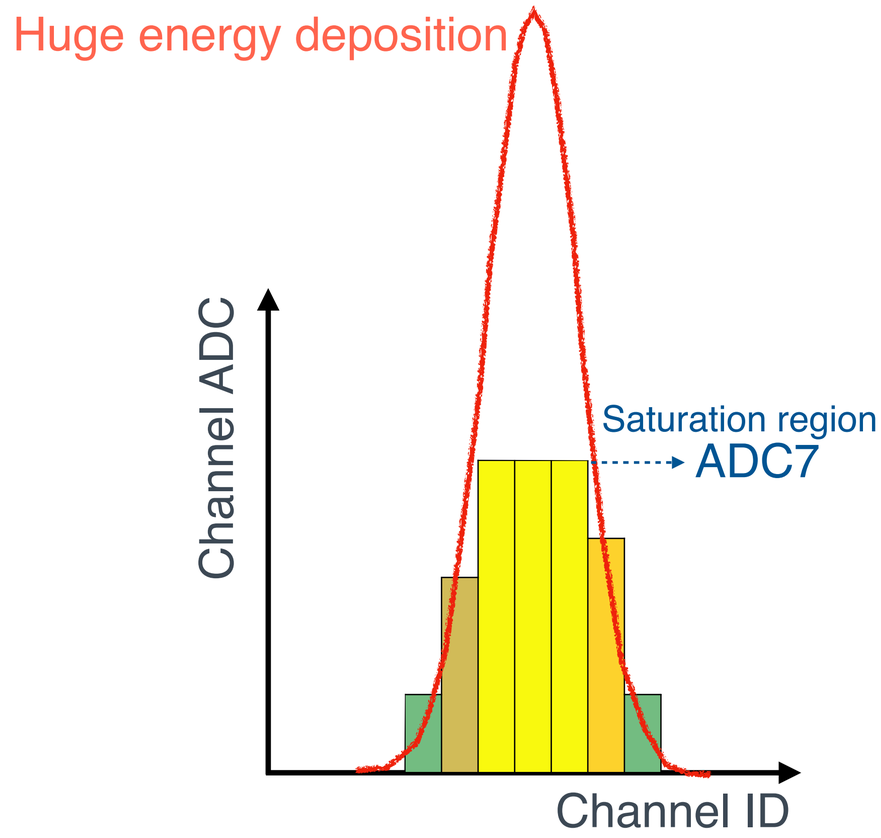

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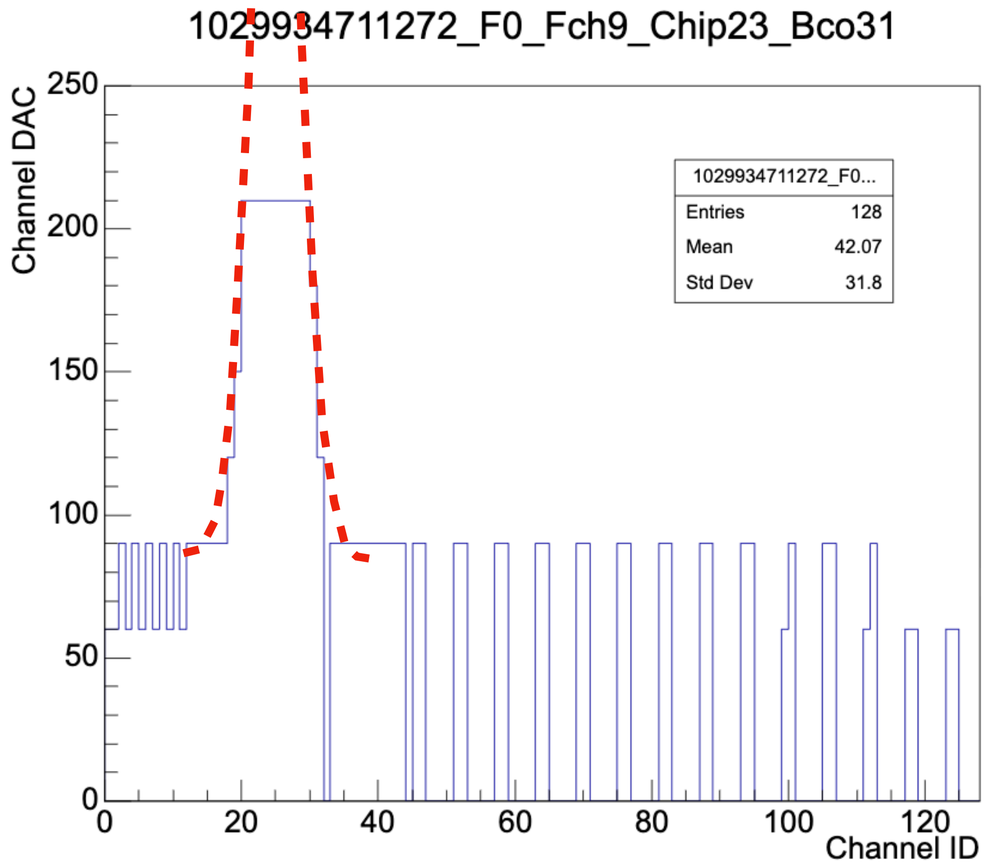
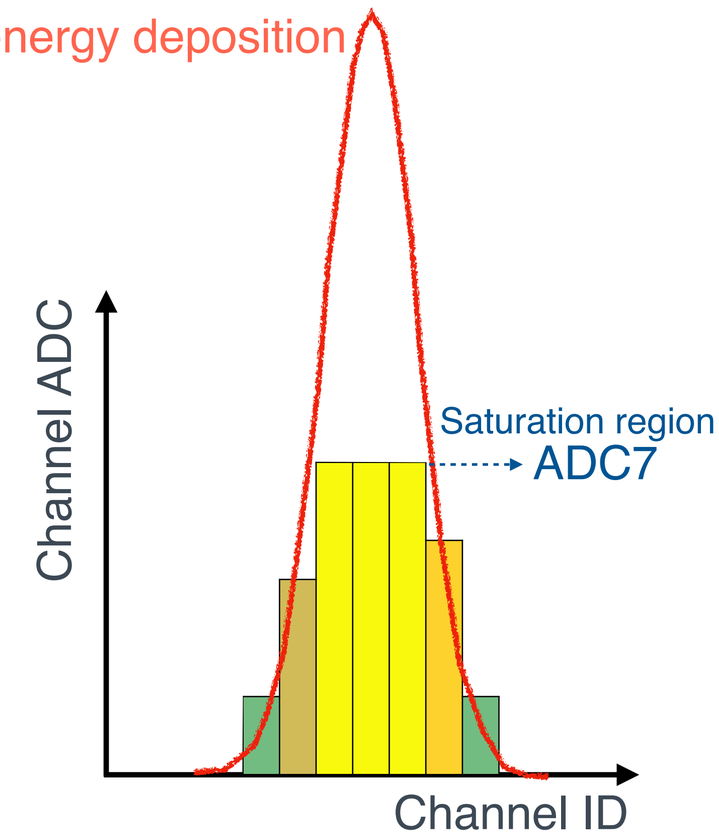
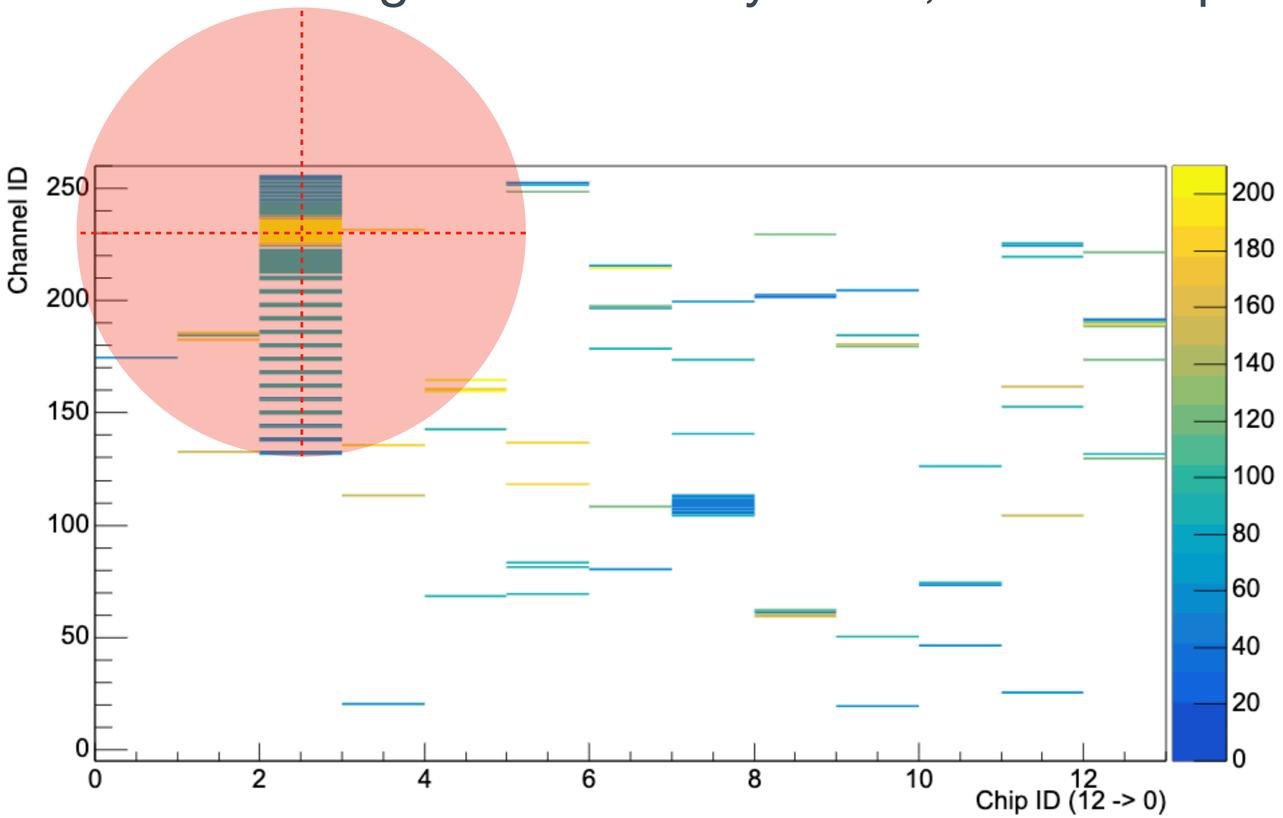
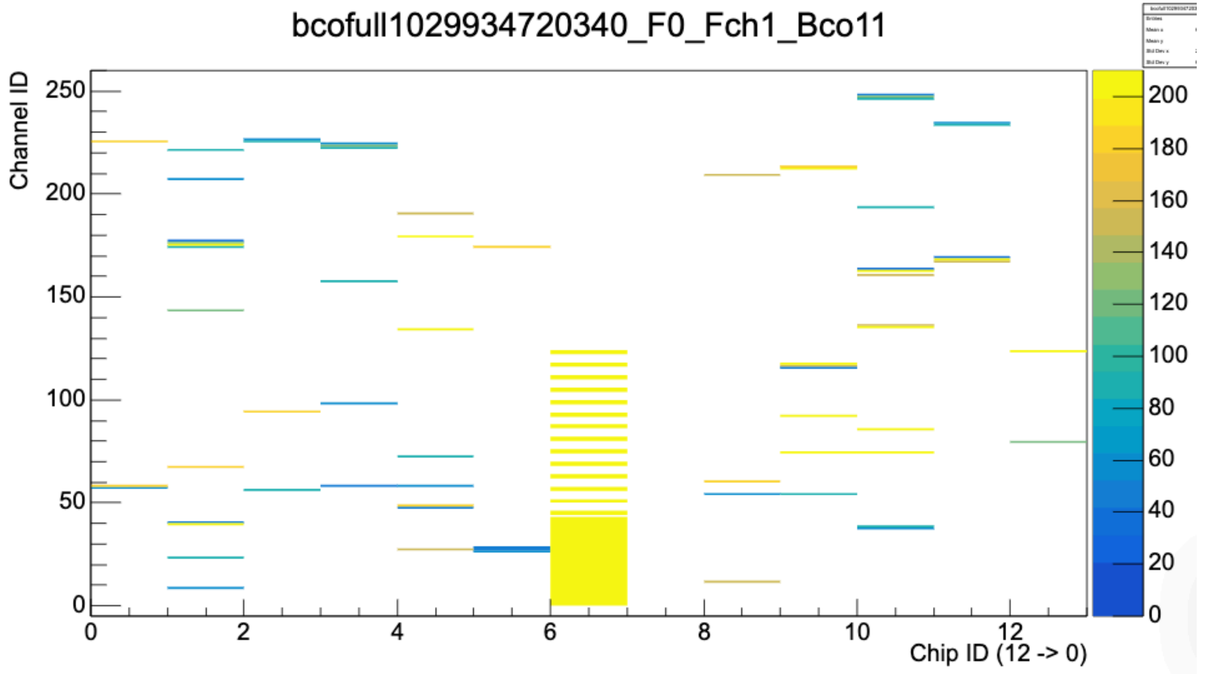




Can those hits be real?

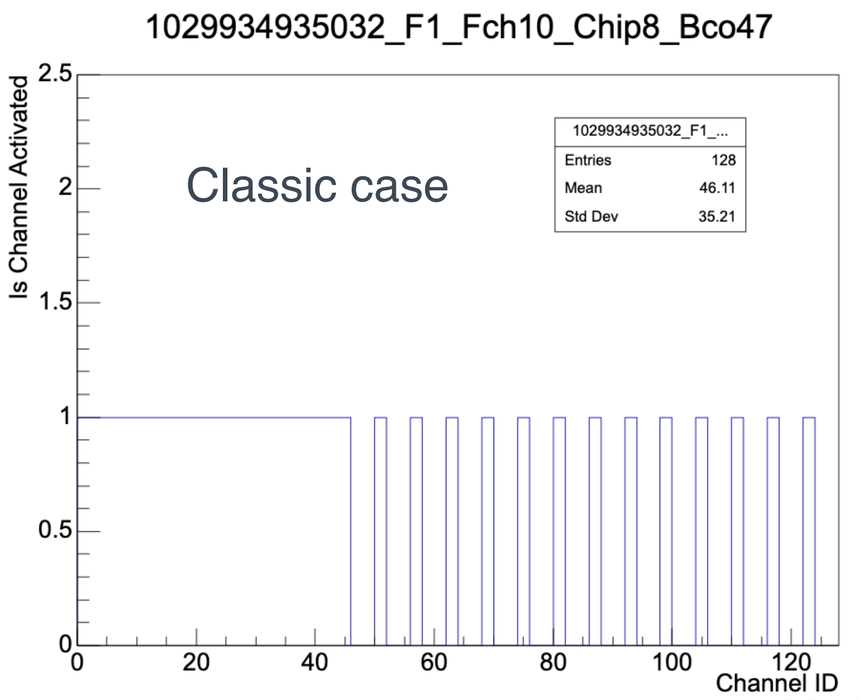
- Con side
  - If the charge-cloud theory holds, how come it (almost) never has charge shared to the adjacent columns?
  - If the charge-cloud theory holds, how come it (almost) extends to the end of one chip (channel 127)?
  - If the charge-cloud theory holds, how to explain the following case?

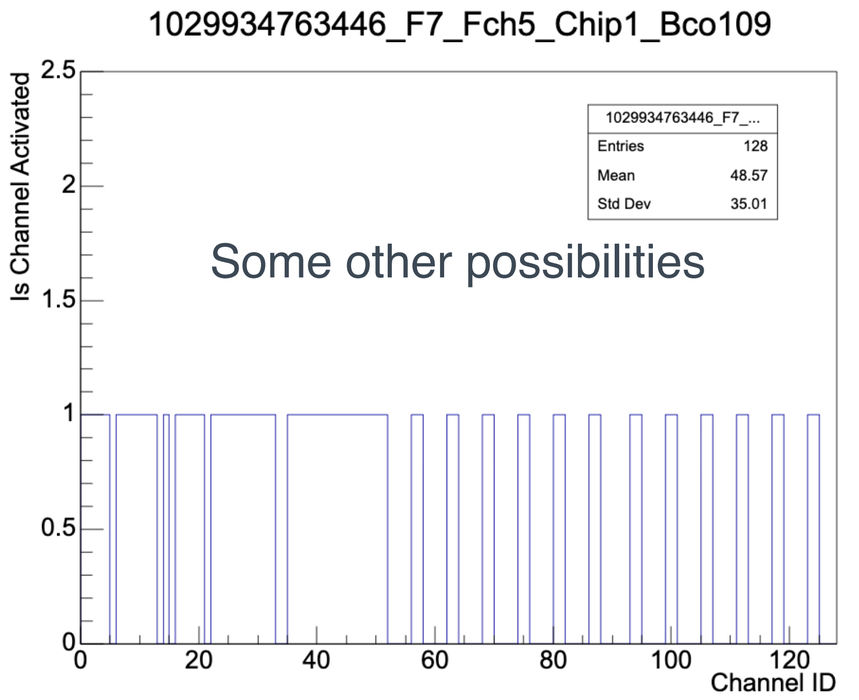


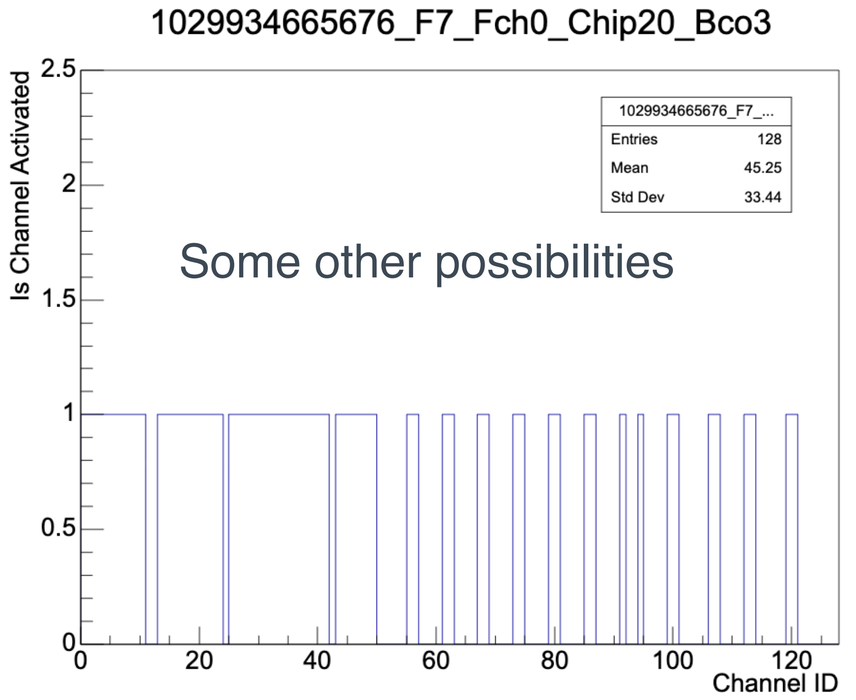


Attempt to identify the saturated chips

- The chip hit maps of saturated chips are so diverse
  - > 80k different patterns in 420k saturated chips (identified based on the ChipHit cut), even if disabling the hit ADC information (only checking whether the channel is activated or not)



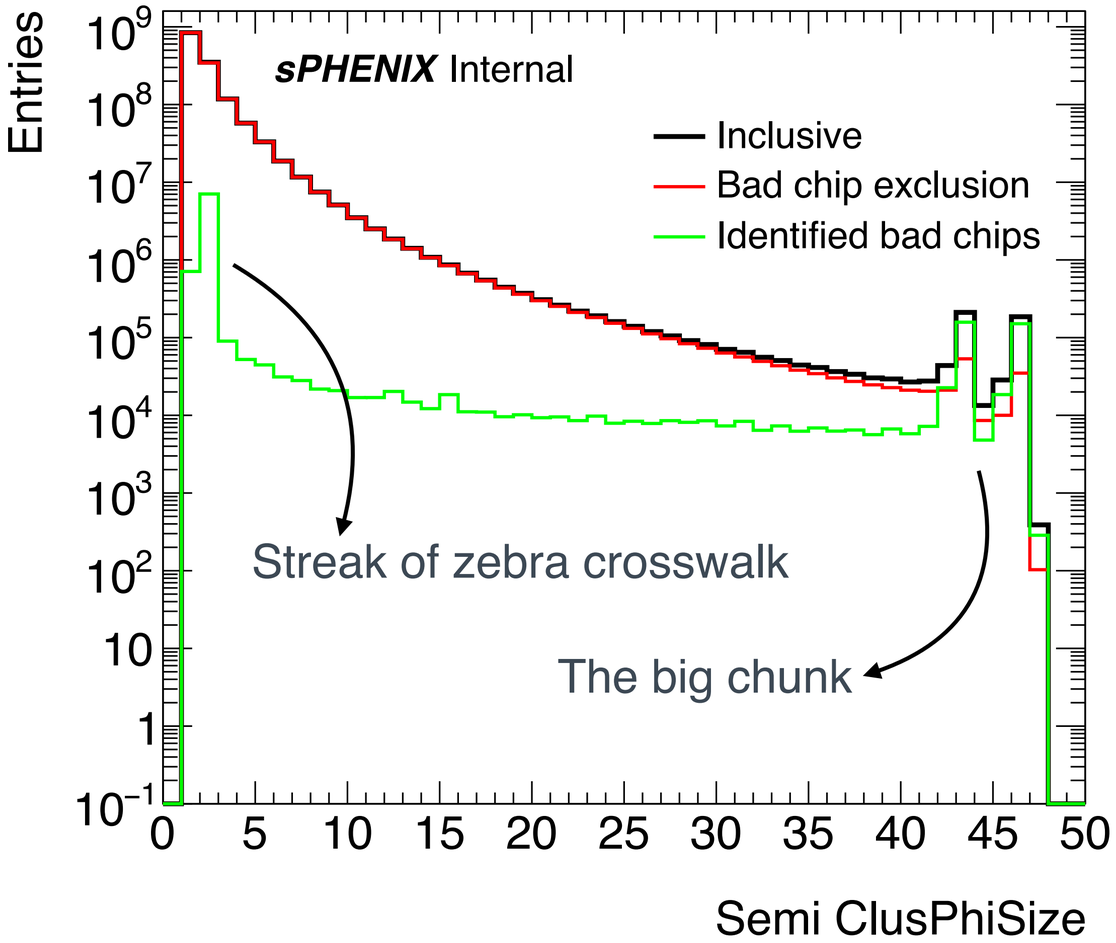


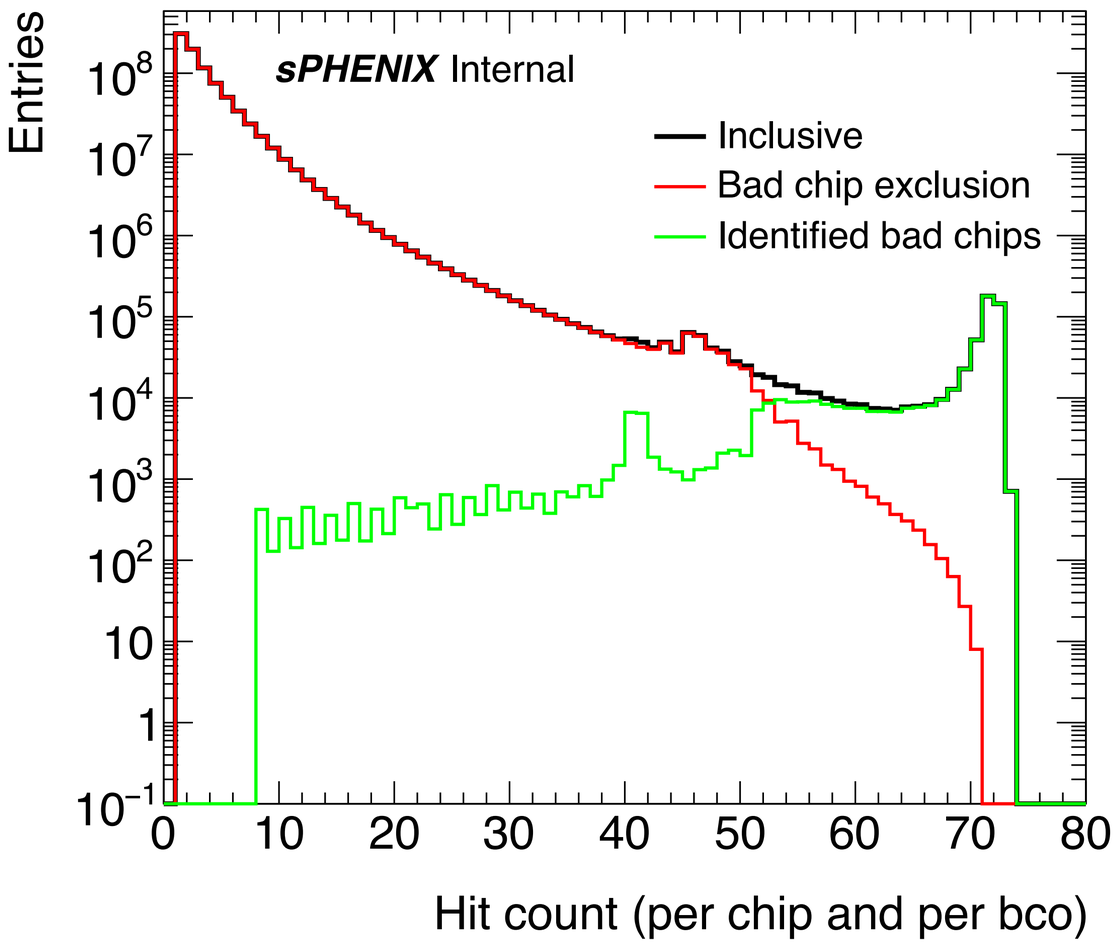


Attempt to identify the saturated chips

- Approach: more like focusing on the zebra-crosswalk region
  - (Largest cluster size > 25 && number of sized-2 clusters >= 5) or
  - One of the following patterns is found in the chip hit map
    - Pattern1: 11000011000011000011 (span b/w streaks: 4 channels)
    - Pattern2: 11000000110000110000 11 (allow one span b/w streaks to be 5 channels)
    - Pattern3: 11000011000001100001 1
    - Pattern4: 11000011000011000001 1

Attempt to identify the saturated chips

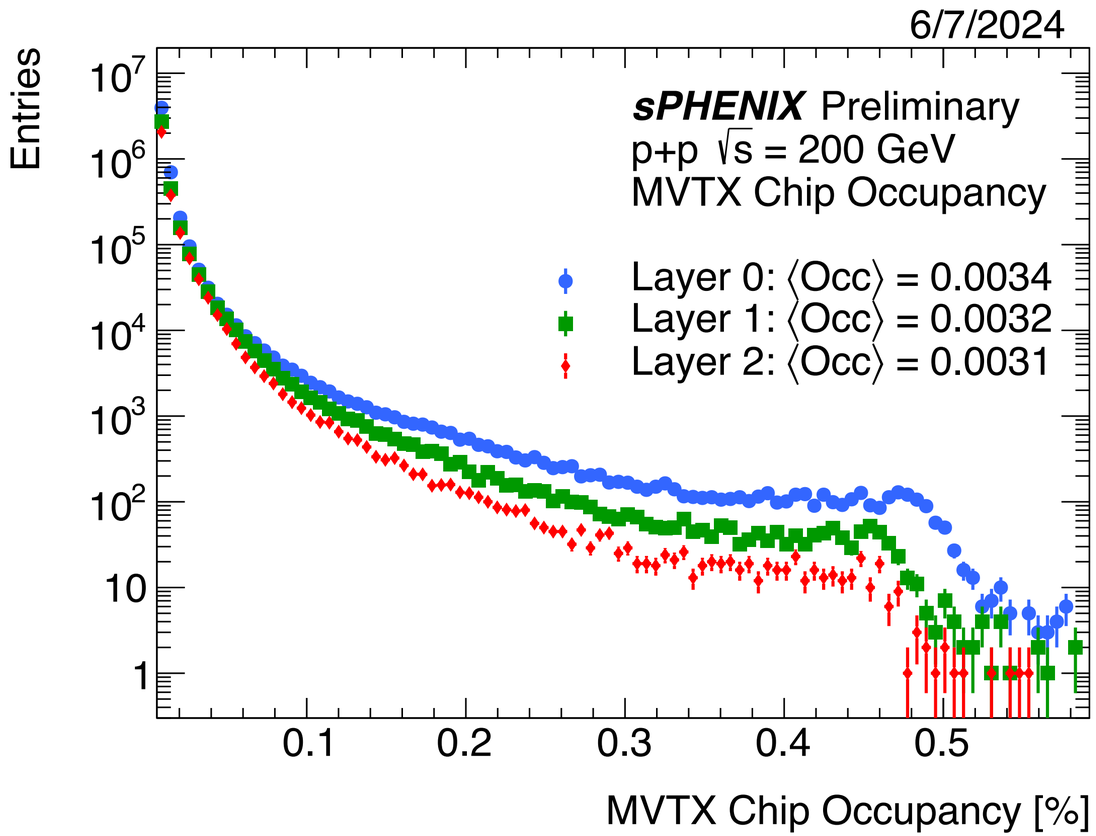




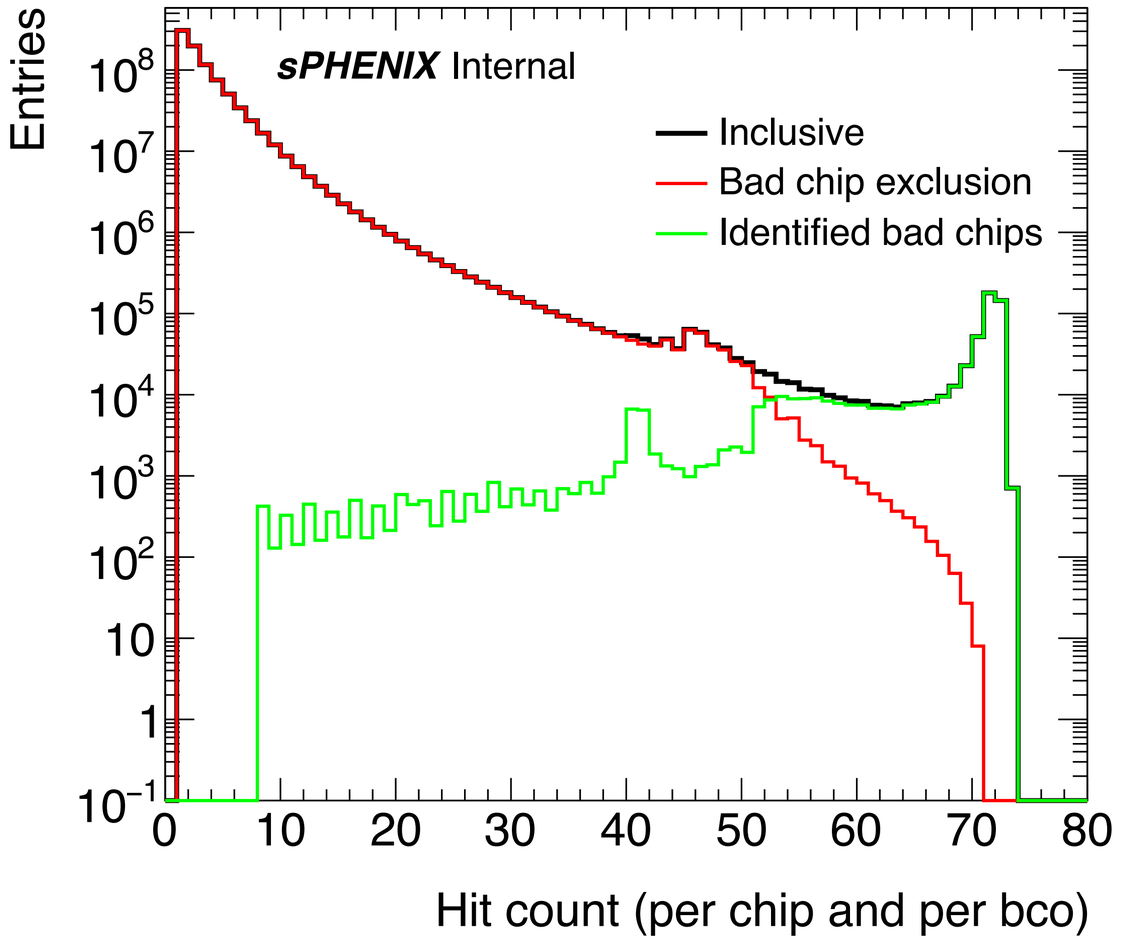
Two spikes still visible → not all the saturated chips can be identified using the current algorithm
But the sizes of the two spikes are reduced by ~ 80% already

Attempt to identify the saturated chips

MVTX chip occupancy in **p+p** collisions

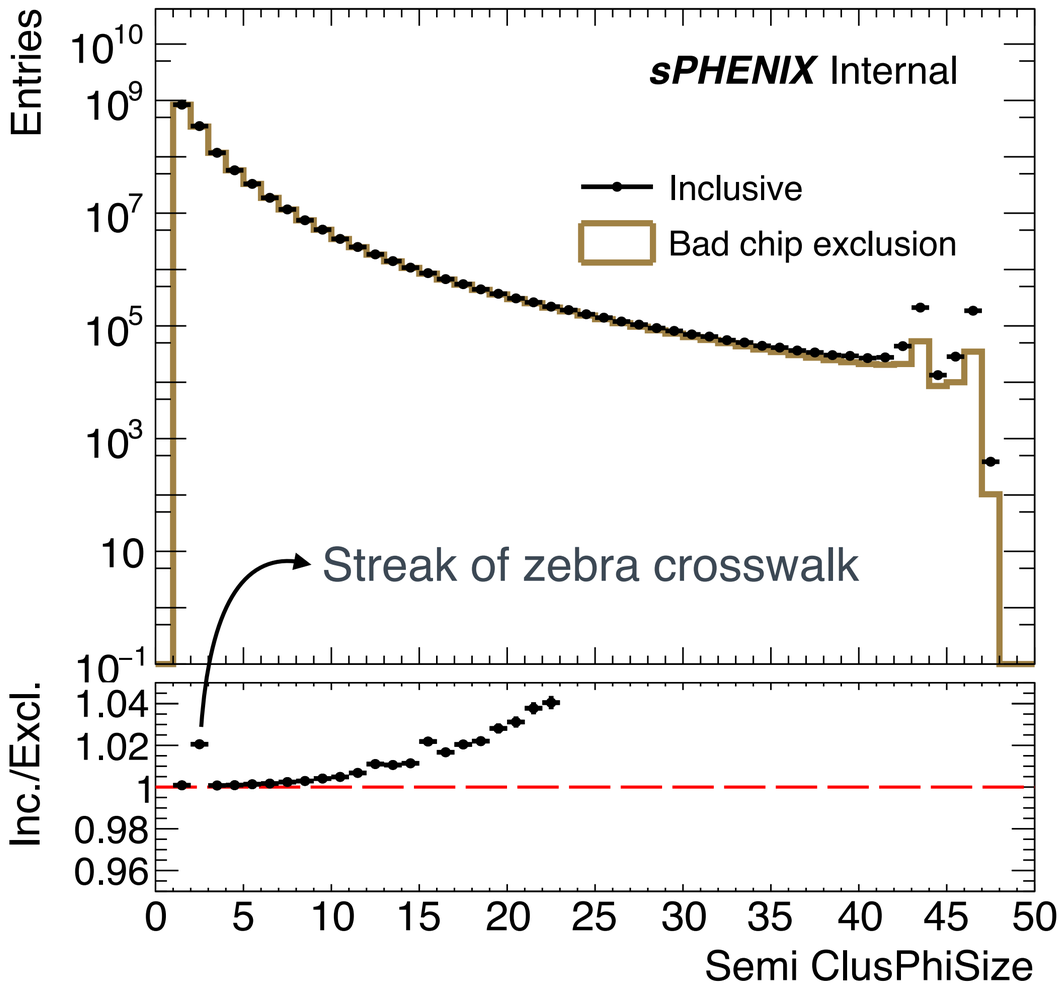


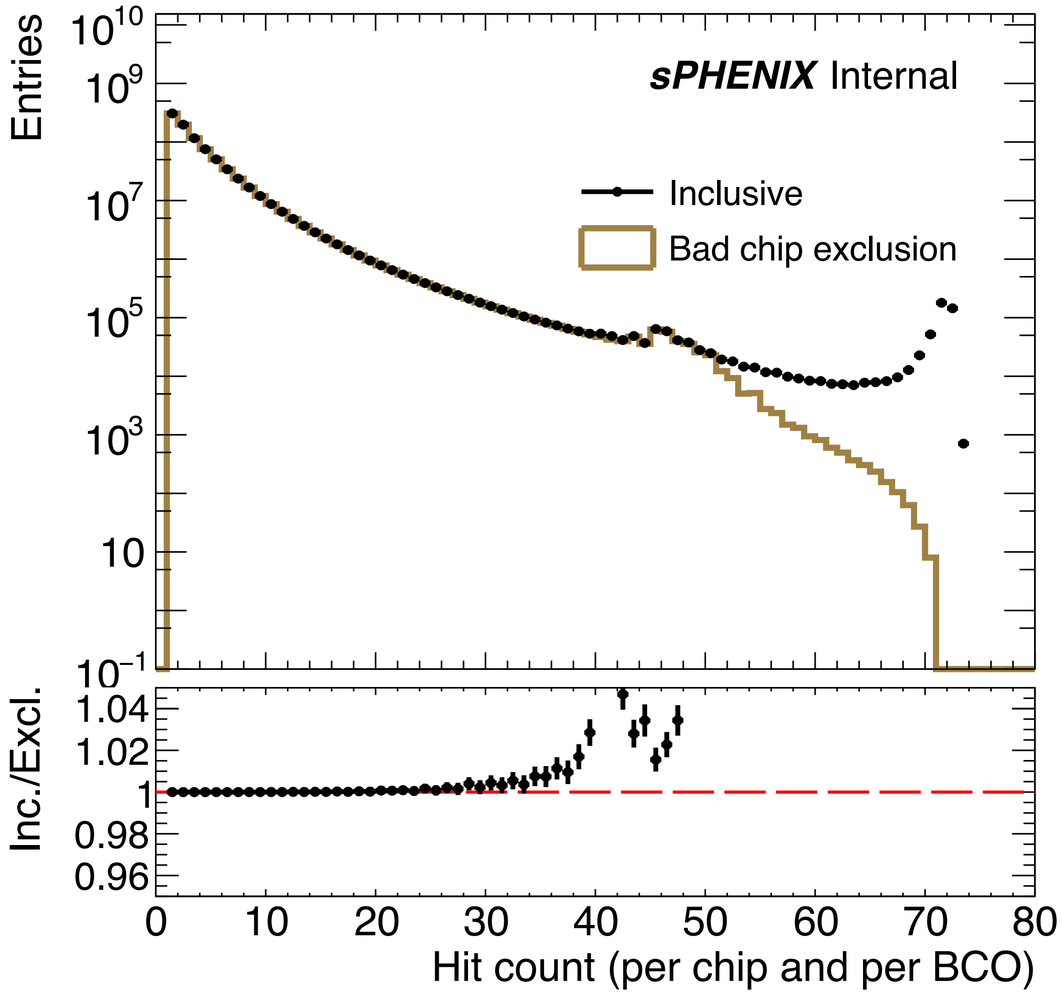
INTT chip occupancy in **Au+Au** collisions



Similar shape, perhaps a good sign?

Attempt to identify the saturated chips





With the semi clustering algorithm (grouping hits chip-by-chip): clusters in the bad (saturated) chips (8.72013e+06) / all clusters (1.45917e+09) = 0.597% → below 1%, not a major issue

Summary

- The chip-saturation issue, an issue in the chip level, should not be a major problem, as it only accounts for ~ 0.6% of the total number of clusters, and it's independent of the event activities

- It's still unclear whether hits in the saturated chips are real or not
  - The charge cloud hypothesis kind of explains some signatures, but can be easily defeated

- Should any measures be imposed to hits/clusters in the saturated chips?
  - If so, we have to find the way to find them first

- A trial to identify the saturated chips was attempted
  - Primarily based on the zebra-crosswalk region
  - It seems that most of the saturated chips can be picked up

- Concerns
  - It's not impossible that some good chips are being misidentified with the current algorithm
    - It's hard to realize
  - The algorithm can possibly be more flexible to pick up more saturated chips, but could also result in more good-chip-misidentification
- Potential solution: develop an unlabeled training model (like LLM)
- Question to the INTT group: whether this is really something we need to do or not?

Back up