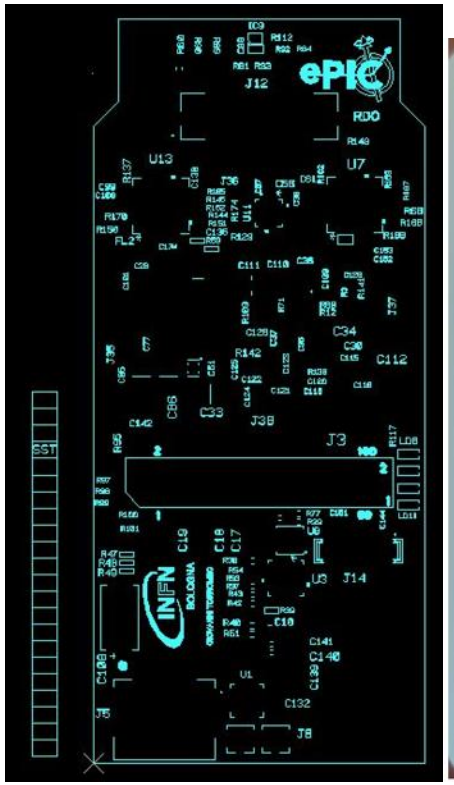
dRICH RDO



P. Antonioli, D. Falchieri, S. Geminiani,
L. Rignanese, G. Torromeo
(INFN Bologna)

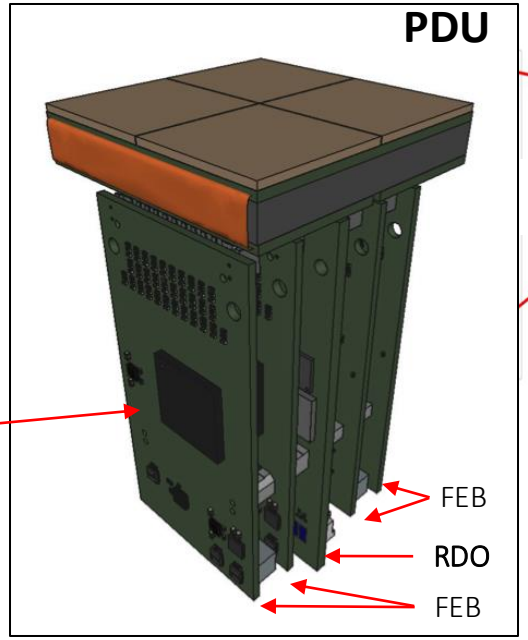
on behalf of dRICH DSC

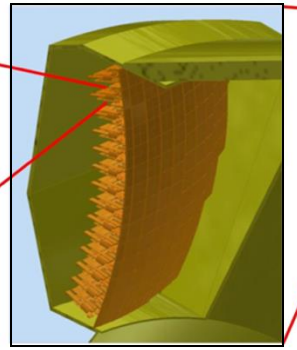
[special thanks to A. Lonardo – INFN Rome, to prepare the dRICH DAQ backend discussion in this presentation]

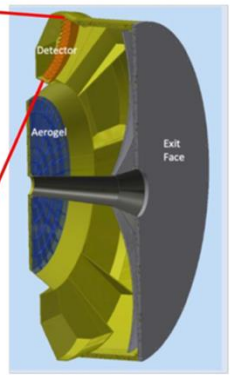
Incremental Preliminary Design and Safety Review of the EIC Detector
DAQ and Electronics
September 3-4, 2025

dRICH RDO re-cap in two slides (I)

dRICH status: M. Contalbrigo at April 2025 PID Review
dRICH SiPM status: R. Preghenella at April 2025 PID Review







RDO is inside dRICH **PDU** photo detection unit

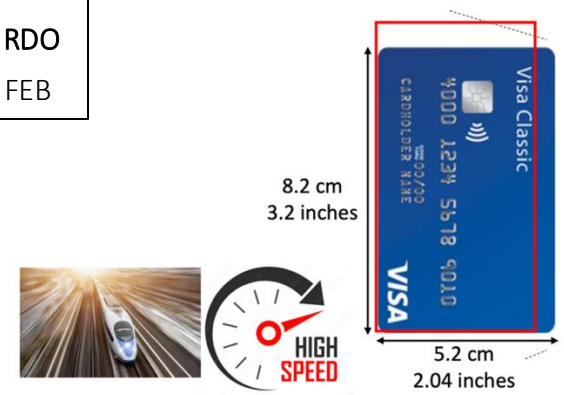
dRICH RDO **requirements** (from DAQ PDR review June 2024)

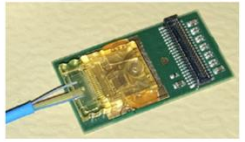
- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus towards FEBs
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- **opt. tranceiver** must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps

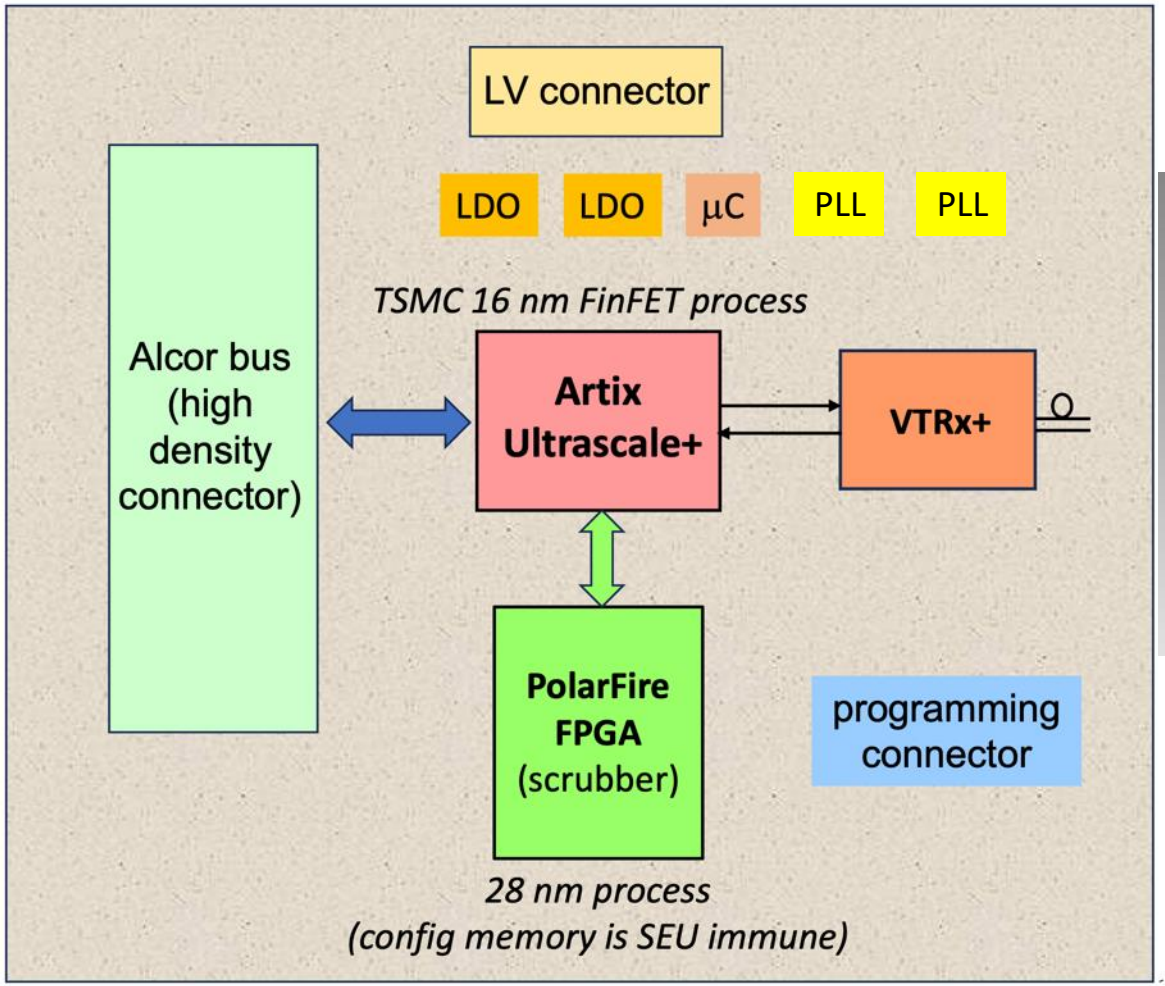




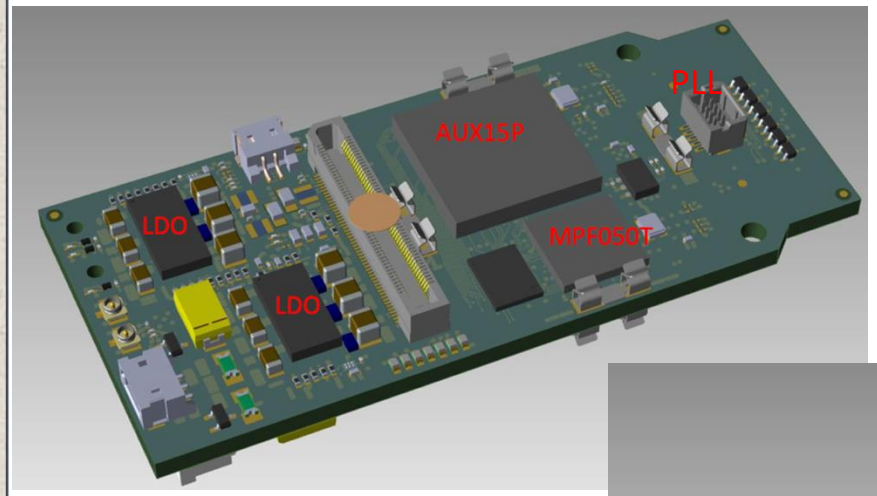
dRICH RDO re-cap in two slides (II)

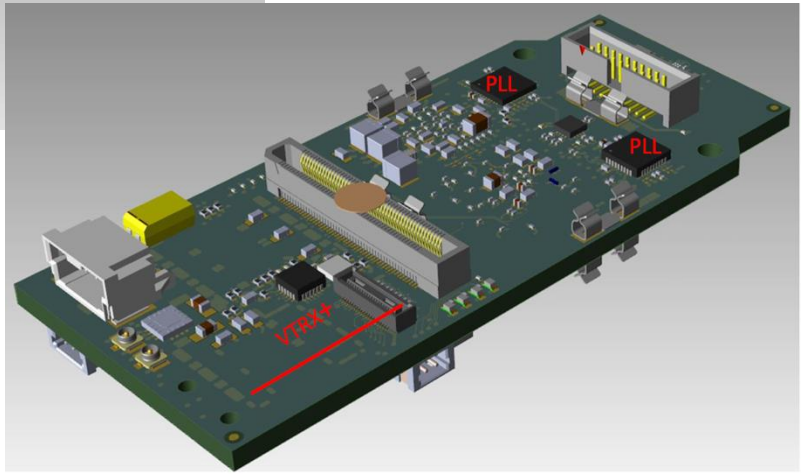
Main design choices

- a performing RAM-based FPGA + scrubbing implemented via a Flash-based FPGA
- devoted PLLs to manage clock (SkyWorks 5319 / 5326)
- VTRX+ as optical tranceiver
- a small uC acts as RDO power manager

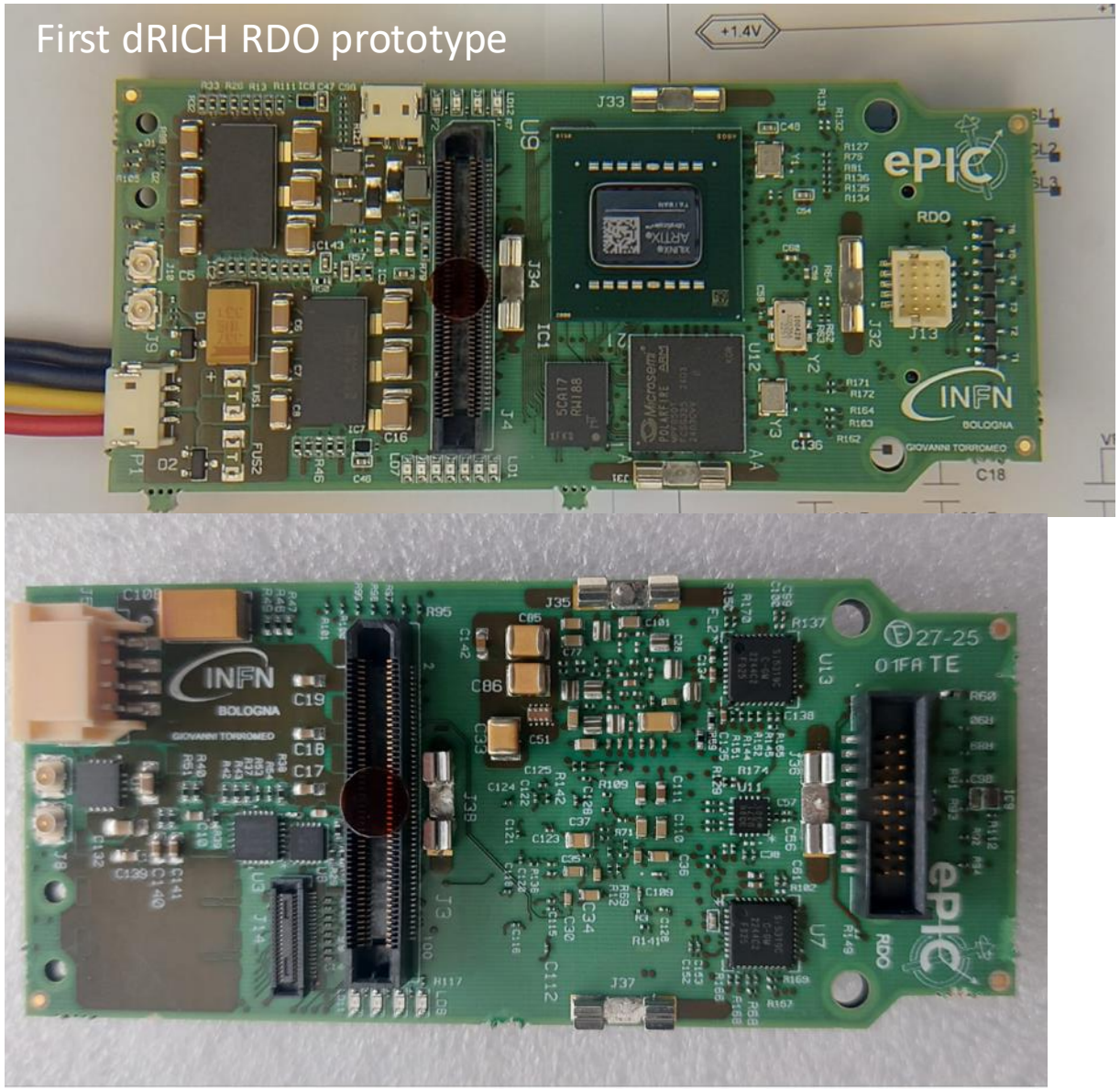


Long and painful elaboration of exact RDO specifications
+ components selection + schematics preparation + layout time +
production time: design started January 2024





dRICH RDO is finally getting real

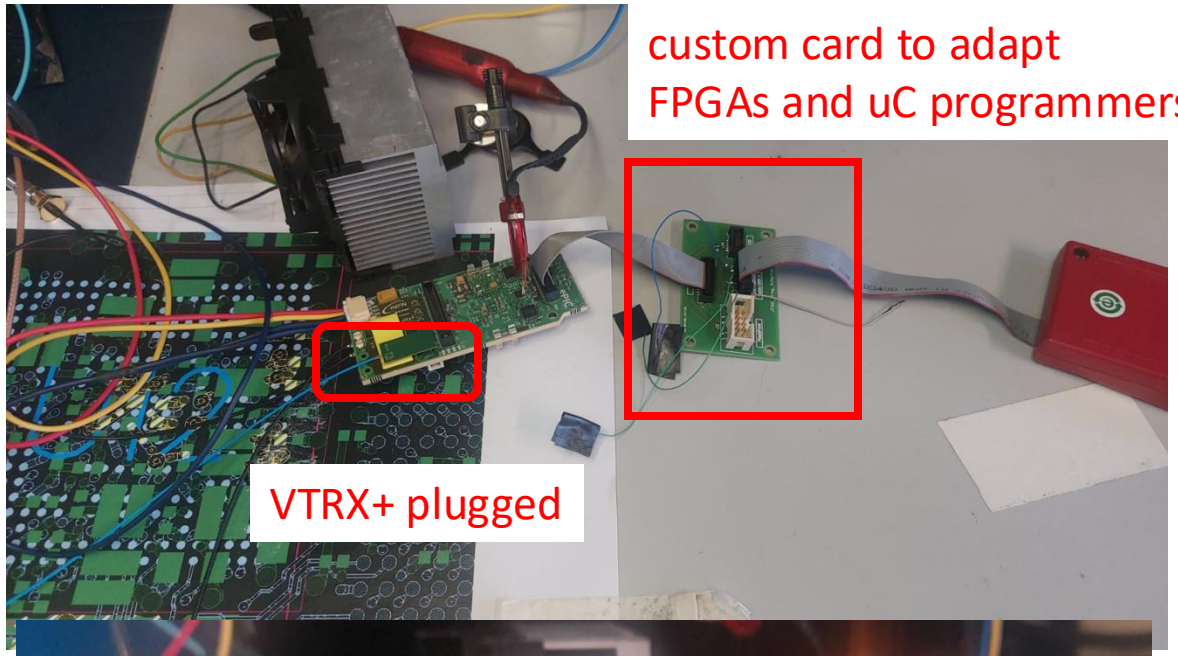


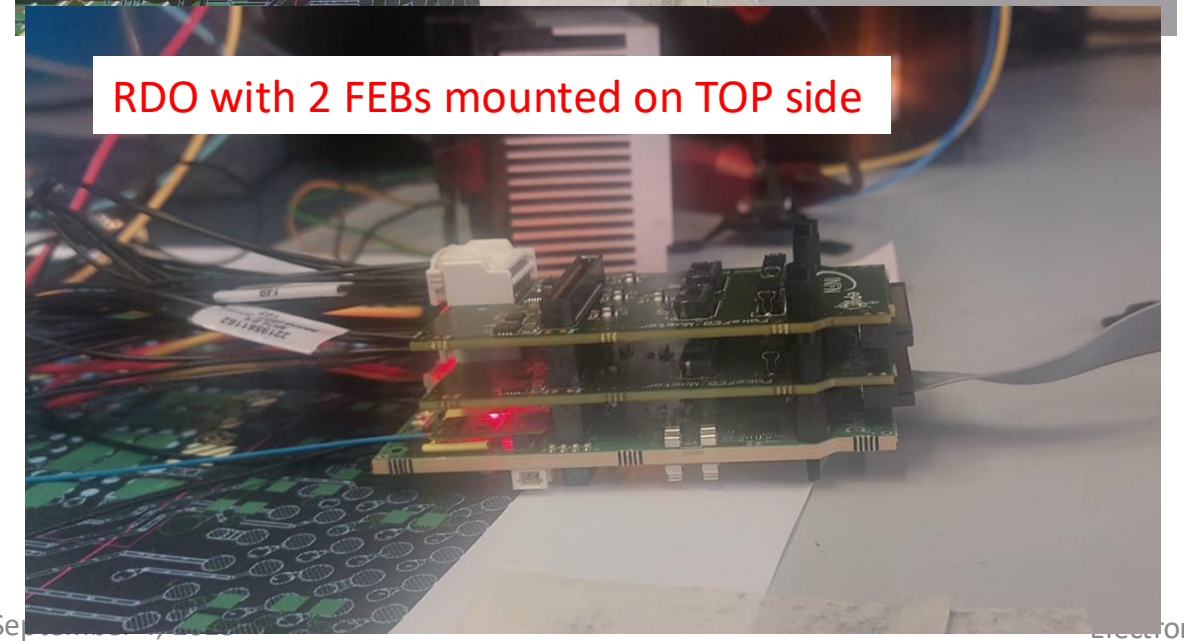
First two prototypes finally received **July 24, 2025!**

This report:

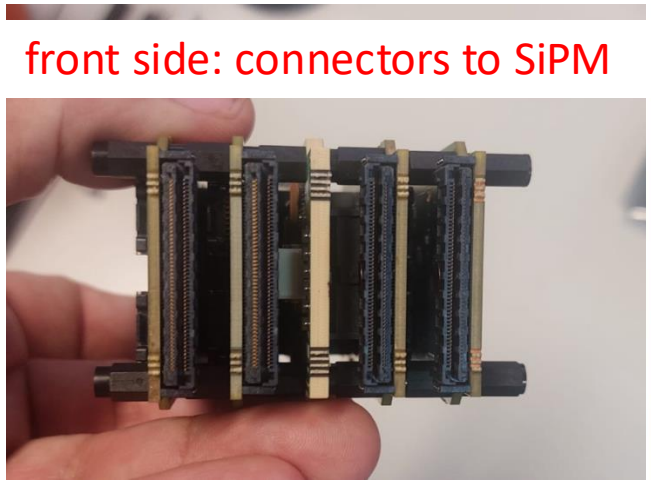
→ updates/activities w.r.t. PDR 2024
as reference: dRICH RDO PDR 2024 presentation
→ ongoing debug / tests on first two prototypes
→ plan (2025/2026)

no longer 3D-rendering: some pics

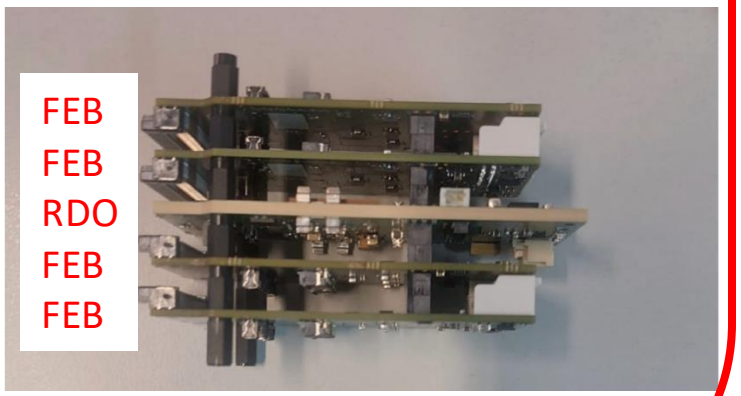




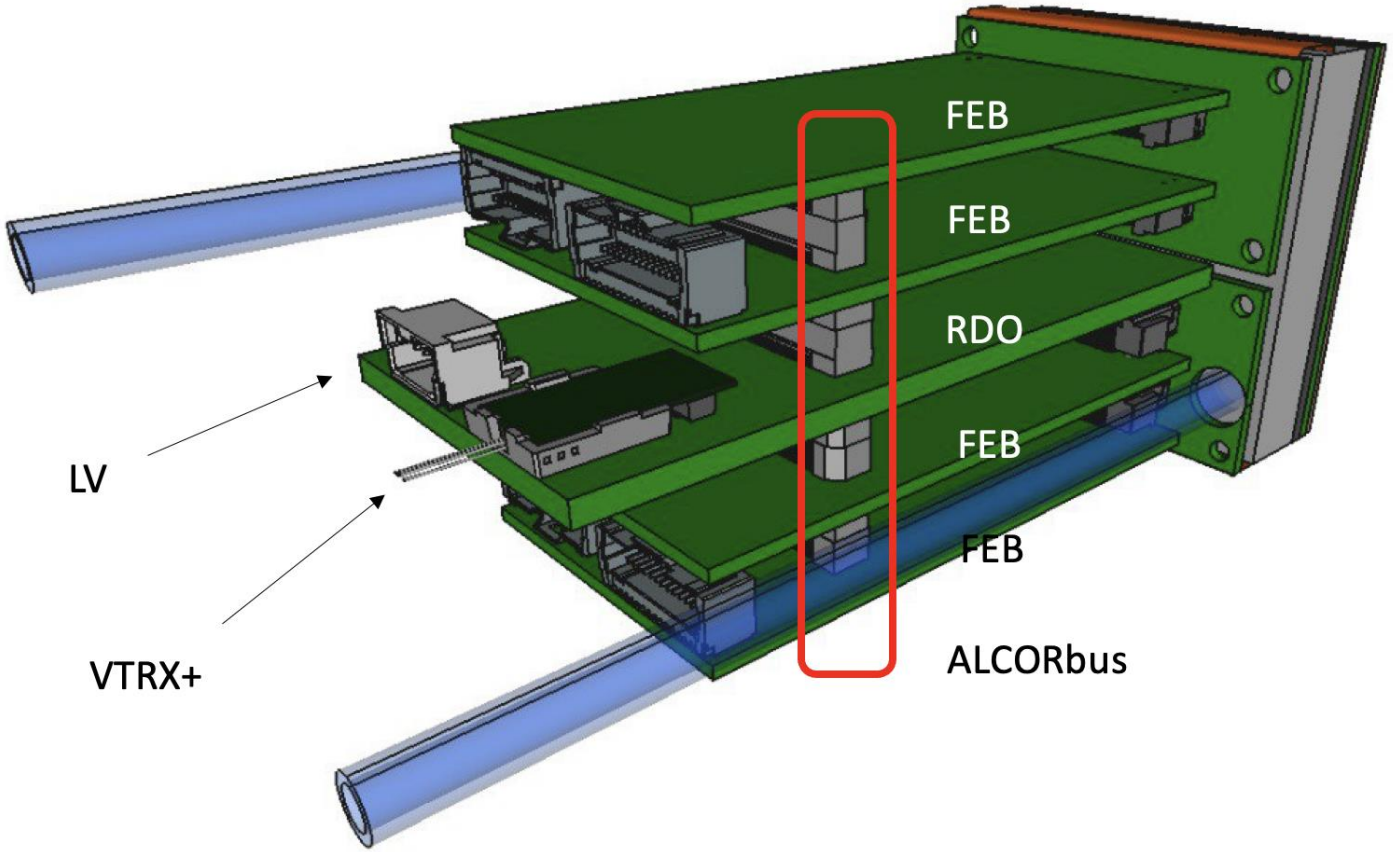
RDO+4 FEB dRICH

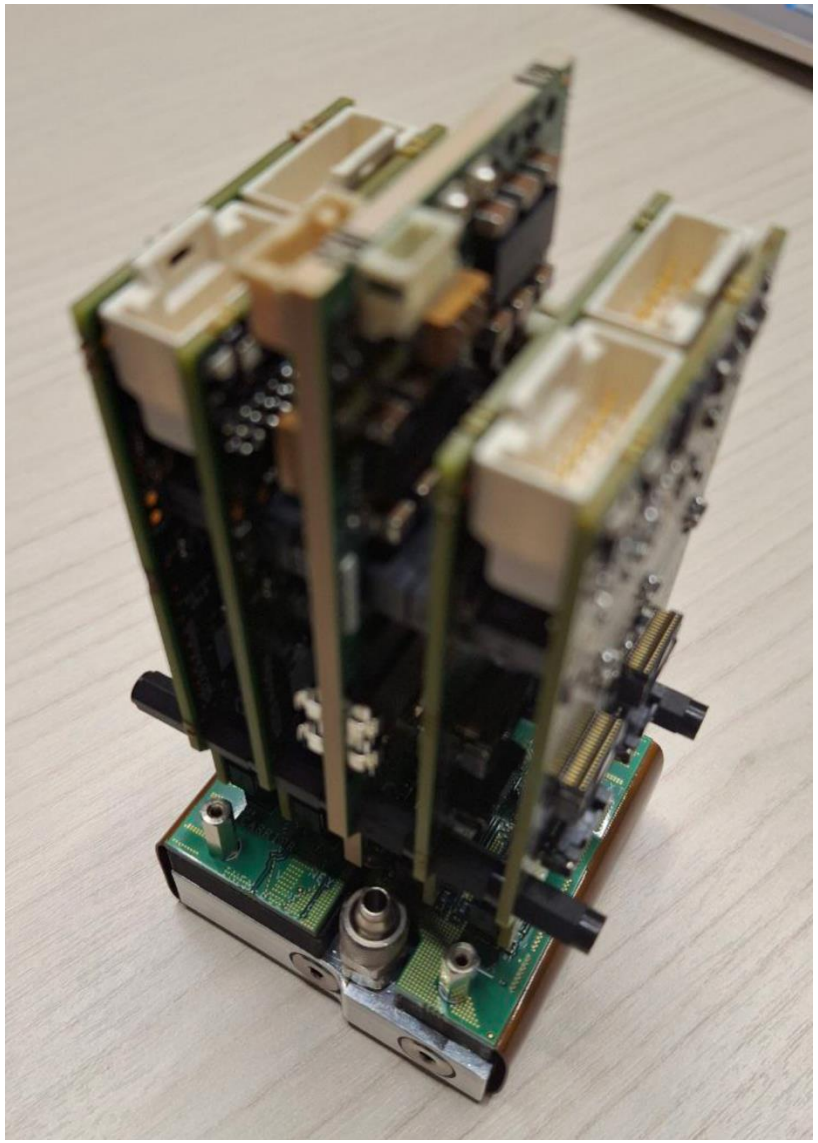


The dRICH electronic burger



from CAD to pics: the PDU



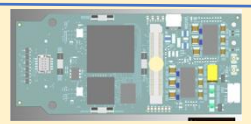


Updates since 2024 PDR

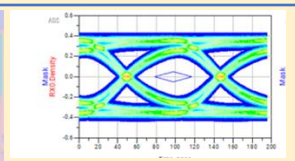
PDR — PDR

June 2024 — Dec — Mar — Jun — Sep 2025

design finalization



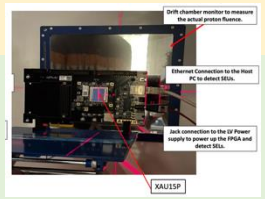
PCB layout / verification



July 24

PCB production

prototypes validation

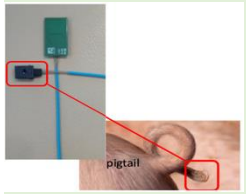


irradiation tests
of RDO components

firmware porting using ALINX AUX15P
analysis of RDO power consumption

VTRX+ tests (light leakage)

back-end DAQ redesign (DAM)

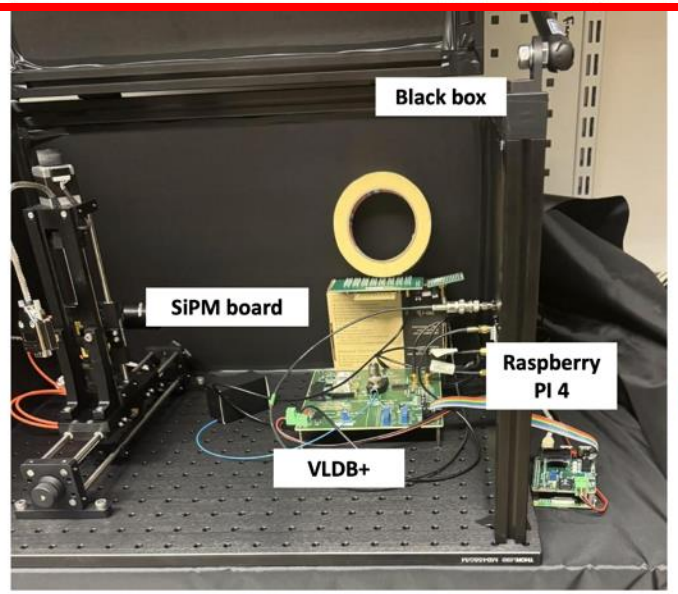


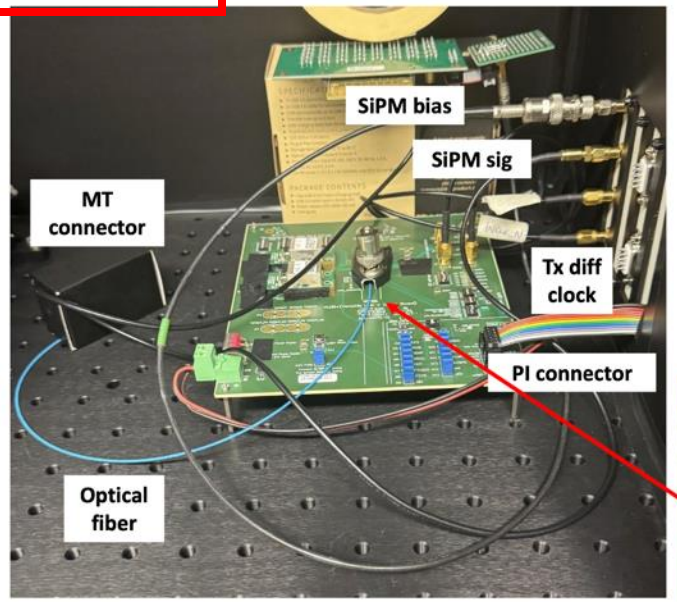
definition of VTRX+
pigtail length

VTRx+: light leakage studies + pigtail length (I)

VTRX+ light leakage tests

Context: LHCb colleagues told us VTRx+ has significant light leakage (from the transceiver + fiber)

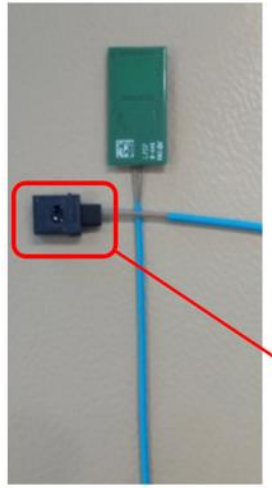


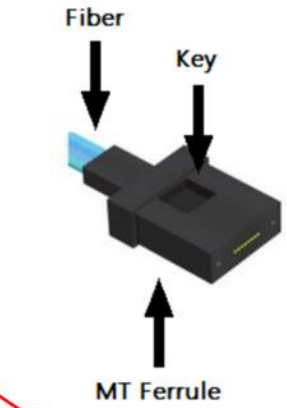


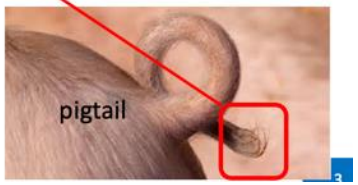
no cover of the fiber
SIPM in front of VTRX+ (not as PDU case, see next slide)
all leds of VLDB+ shielded with dark tape

Test bench: black box + 1 SIPM

"minimal" cover of VTRx+
(+ BNC adapter ;-) to keep it "tight"





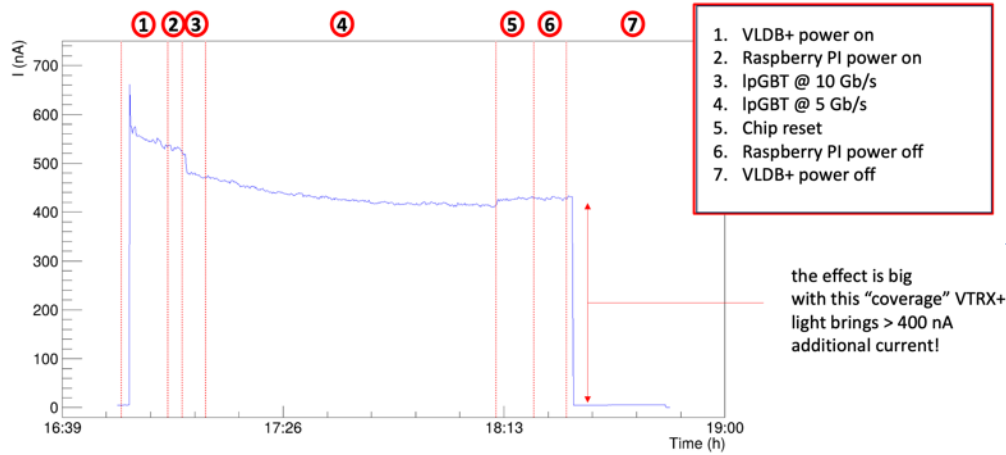


R. Preghenella/S.Geminiani/A. Paladino

More details on PA's talk at DAQ-Electronics WG/eRD109 (March 2025)

VTRx+: light leakage studies + pigtail length (II)

Initial results



1. VLDB+ power on
2. Raspberry PI power on
3. lpGBT @ 10 Gb/s
4. lpGBT @ 5 Gb/s
5. Chip reset
6. Raspberry PI power off
7. VLDB+ power off

the effect is big with this "coverage" VTRX+ light brings > 400 nA additional current!

huge current seen by SIPM (bias=38.7 V, 0 OV → working as a diode → "current monitor")

Additional VTRX+ plastic box + Thorlabs masking tape

→ No measurable extra-current: just 5 nA!

→ moved to 2.7 OV

With oscilloscope and measuring DCR (VLDB+ ON/OFF) we finally see:

(400.0 +- 1.8) kHz. VLDB+ ON
(398.4 +- 2.7) kHz VLDB+ OFF

(ON-OFF) = (1.9 +- 3.3) kHz

→ compatible with zero. Note that some kHz is however close to DCR @ - 30 C
→ need to move to -30 C to check

additional home-made "full VTRX+ plastic box"

Details: PA's presentation at eRD109 (Feb. 2025)

Long story short:

- huge leak of light from VTRx+
- we will need to design an effective shield. CERN ESE-VL+ is doing something similar (details).
- initial results (room temperature only) encouraging
- and note after long discussion (Sep/Dec 2024) we opted **for 20 cm pigtail length**

From 2024 June FDR:

Comments

- VTRX+ pigtail lengths must be defined at least 6 months in advance of VTRX+ production. The mechanical designs of both sub-systems are well on track to allow this definition on schedule.

Going shorter and avoid dangling?
We considered several options but for each of them the number of cons largely exceeds the pros. And if too short we can't come back. We don't have any convincing option for such scheme.

How to proceed? We go baseline
We select a 20 cm dangling pigtail
Design needs to be carefully followed up to setup proper access, secure maintenance etc. (but this is valid for almost what we are doing ;-)

dRICH option: 1500 VTRX+ with total length 20 cm

Details: PA's presentation at dRICH meeting (Dec. 2024)

where we are with prototypes?

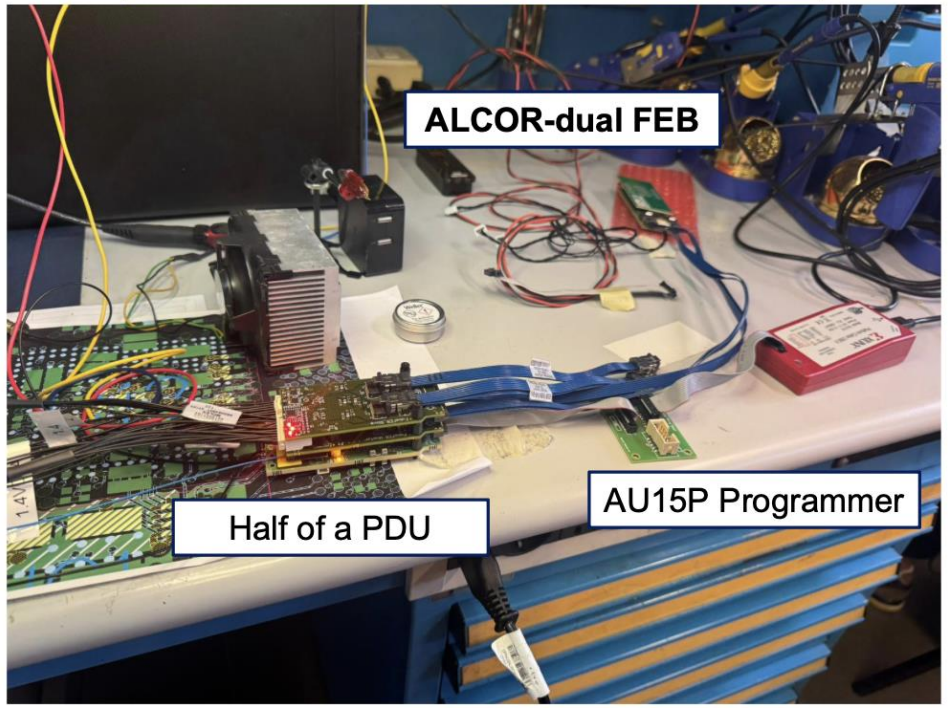
1. Mechanical pairing with fake-FEB (adaptor for ALCOR32 with exactly final FEB-format with ALCOR64)
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Programming uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Programming Artix via external connector
6. Programming Polarfire via external connector
7. Artix at boot makes programming of SkyWorks (programming 125 MHz of Si5319 to setup clock for GTH)
8. Check consumptions
9. Check UFL I/Os
10. IBERT test (loopback tool integrated in Vivado) to check link
11. Link IPBUS via VTRX+ [MT-MPO adapter + fibers]
12. Turn on fake-FEB via I2C from RDO
13. Programming ALCOR via fake-FEB (via IPBUS → VTRX+)
14. ALCOR readout (via IPBUS → VTRX+)

→ RDO team @ work this week on this!

When we reach point 14 we give green light to produce the other 8 RDOs for Nov. 2025 test beam (details)

where we are with prototypes? (UPDATE)

1.
2.
3.
4.
5.
6.
7.
8.
9.
10.
11.
12.
13. Programming ALCOR via fake-FEB (via IPBUS → VTRX+)
14. ALCOR readout (via IPBUS → VTRX+)

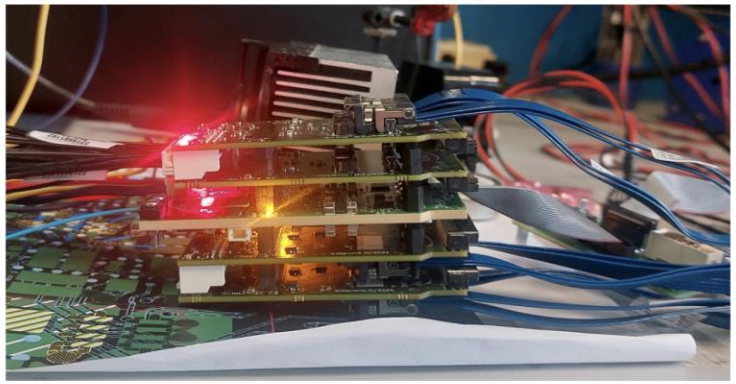


COR32 with exactly final FEB-format with ALCOR64)
er sections

Vout LDO

programming 125 MHz of Si5319 to setup clock for GTH)

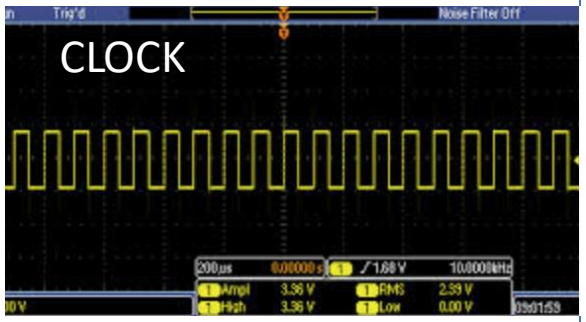
check link
]



- The PDU was mounted and **2 FEBs were powered-on**.
- We **configured all the ALCOR32s successfully**.
- We **read back the data aligned** with the 320 MHz supplied clock.

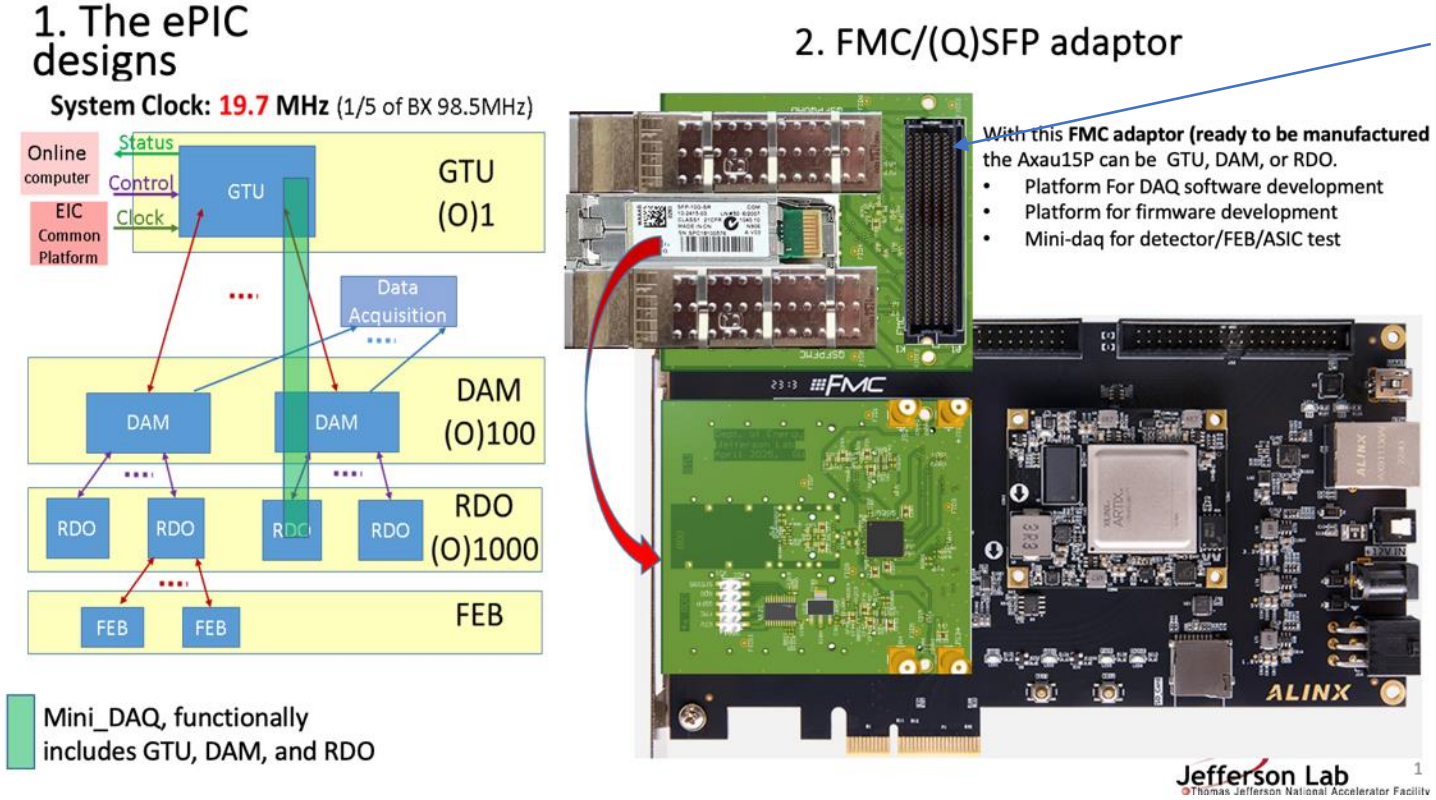
This process was repeated for both sides without any problem from both hardware and software!

which protocol as EIC link protocol for dRICH?



Distribution of a 39.4 MHz was made to support detectors with lpGBT, but also dRICH agreed with ePIC DAQ to receive a **39.4 MHz** clock - close to 40.08 MHz à la LHC. This would be instead of 98.5 MHz (see W. Gu talk)

This will make life much easier with FELIX/RDO: **FULL protocol (GBT on host) to be assessed** (FULL is less resource hungry with respect to lpGBT and we don't have the ASIC, only the VTRX+) → current baseline choice



The piggy back produced by JLab), will allow us (Bologna and Rome) to use a pair of ALINX/AUX15P to first mimic a "RDO" and a "FELIX" link

Second step: FLX-182 (Rome1) ⟷ RDO

Third step: FLX-155 ⟷ RDO

Addressing 2024 PDR report specific comments

Relevant comments:

- We applaud the adaptation of the readout architectures to match detector environment specs, *in particular for the dRICH where steps to mitigate the high DCR will be implemented in the ASIC together with other handles such as triggering within the DAM.*
- We appreciate these steps towards robustness. However, it would be reassuring to see simulations or measurements to demonstrate the effectiveness of the shuttering mechanism for dRICH.

Relevant recommendations:

- Rationalize the dRICH readout with the benefit of simulation/measurement to reassure the community of the benefit of the shutter implementation.

- dRICH backend DAQ was rationalized following studies of ML techniques/NN deployed on DAMs
- Shutter implemented on ALCOR V3 and studies are on-going on shutter performance to assess best (and safe) shutter time width.

→ discussion and results reported in next slides

Updated throughput modelling (I)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM	30
Input link in DAM	42
Output links from DAM to TP	1
Number of DAM Trigger Processor	1
Input link to DAM Trigger Processor	30
RDO-DAM Link Bandwidth (VTRX+) [Gb/s]	10
DAM to Echelon-0 Switch Bandwidth [Gb/s]	100
dRICH Interaction tagger reduction factor	1
Interaction tagger latency [s]	1,00E-04
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	(if you put 10 ns == no shutter)

Reduction factor via shutter
RF = 10 ns/(shutter width)

dRICH backend DAQ reorganized following studies from INFN Rome (see next slides) from 27+1 to 30+1 FLX-155: 30 DAMs + 1 Trigger Processor (TP)

Reduction factor provided by whatever ext. trg (including NN on dRICH DAMs)

Updated throughput modelling (II)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	1		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	2	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

This is worst case!

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	55,20	800,00	
Throughput to serializer [Mb/s]	34,50	788,16	
Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
Input at each DAM [Gbps]	45,28	420,00	
Buffering capacity at DAM [Mb]	4,64		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	1.358,44	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

*Take home message

Using only the shutter with a reduction factor 5 (2 ns over 10 ns BC) we keep 1.3 Tbps throughput and we stay within all limits (including transfer from DAM to Echelon-0)

Updated throughput modelling (III)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	5		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	10	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	276,00	800,00	
Throughput to serializer [Mb/s]	172,50	788,16	
Throughput from ALCOR64 [Mb/s]	1.380,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	5,39	10,00	based on VTRX+
Input at each DAM [Gbps]	226,41	420,00	
Buffering capacity at DAM [Mb]	23,18		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	6.792,19	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

10 ns means no shutter

data reduction via "another method"

further risk mitigation here might be applied using two TX links instead of one

*Take home message

If shutter is not effective we need a reduction factor 5 from a dRICH interaction tagger method and we stay within all limits (including transfer from DAM to Echelon-0)

Will the shutter be effective?

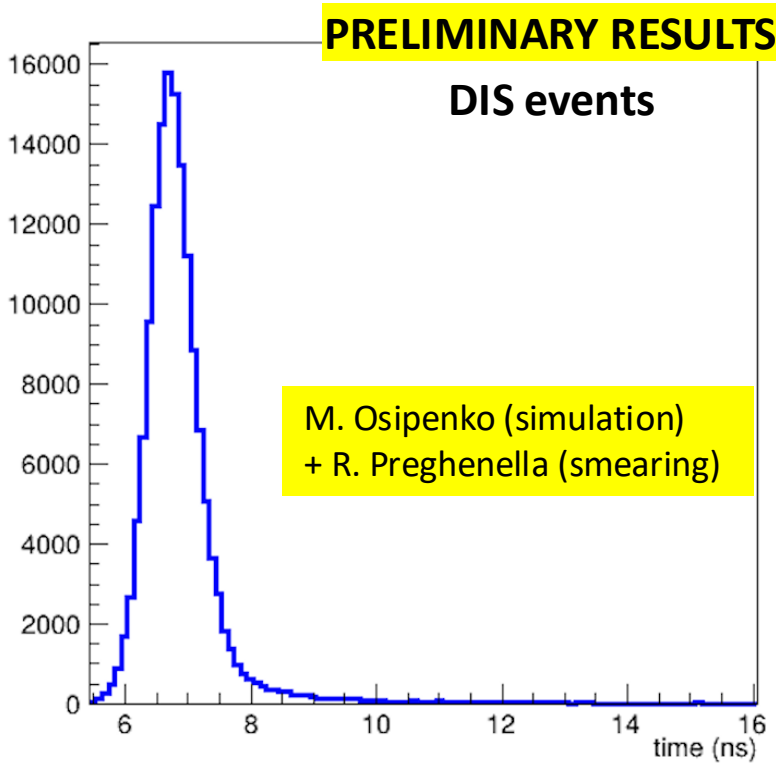
(for all work on shutter *implementation* in ALCOR v3 and related simulations see F. Cossio talk)

Simulations of hit time distribution at dRICH entrance window (before aerogel)

- Hit time distribution (primaries) has Gaussian shape + a tail
- Bulk of primary hits lies **within 2 ns** ($\sigma_{pr} \cong$ 260 ps**)**
- added in quadrature time zero jitter (σ_{t0}= 250 ps) + front-end resolution (σ_{FE}= 150 ps)

$$\sigma = \sqrt{\sigma_{pr}^2 + \sigma_{t0}^2 + \sigma_{FE}^2} \approx \text{ 400 ps}$$

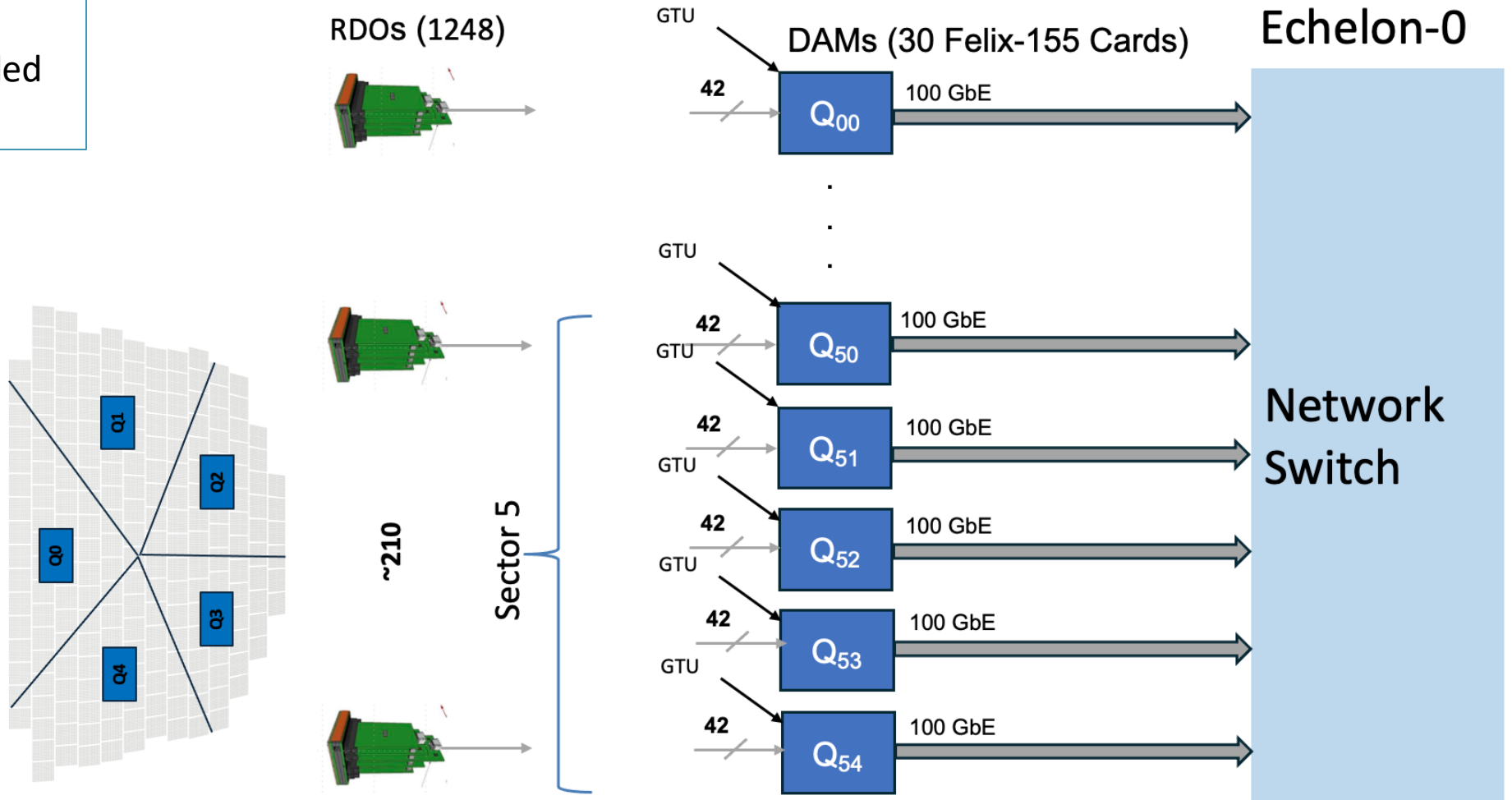
- from cumulative distribution 99% of particles included with a shutter window of 5 ns (from 5.5 ns to 10.5 ns → **50% DCR data reduction**)



Full simulation (including Cerenkov light propagation) in progress:
→ we don't expect a large spread added by photon emission + propagation
→ impact of time slewing effect (see F. Cossio talk) to be assessed

dRICH DAQ: the backend (updates from 2024)

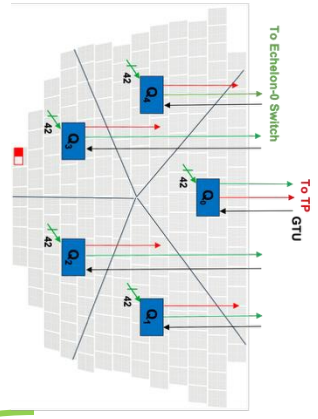
IMPORTANT NOTE:
dRICH DAQ backend is led by INFN Rome



Details about dRICH DAQ backend studies in A. Lonardo's talks at ePIC Jan 2025 meeting and ePIC Italia June 2005 meeting

dRICH data reduction integrated in the DAQ Backend (I)

Neural network distributed over 31 Felix-155



From PDU

Sector 0

Sector 5

To Echelon-0 switch

GTU

Trigger to DAMs

TP

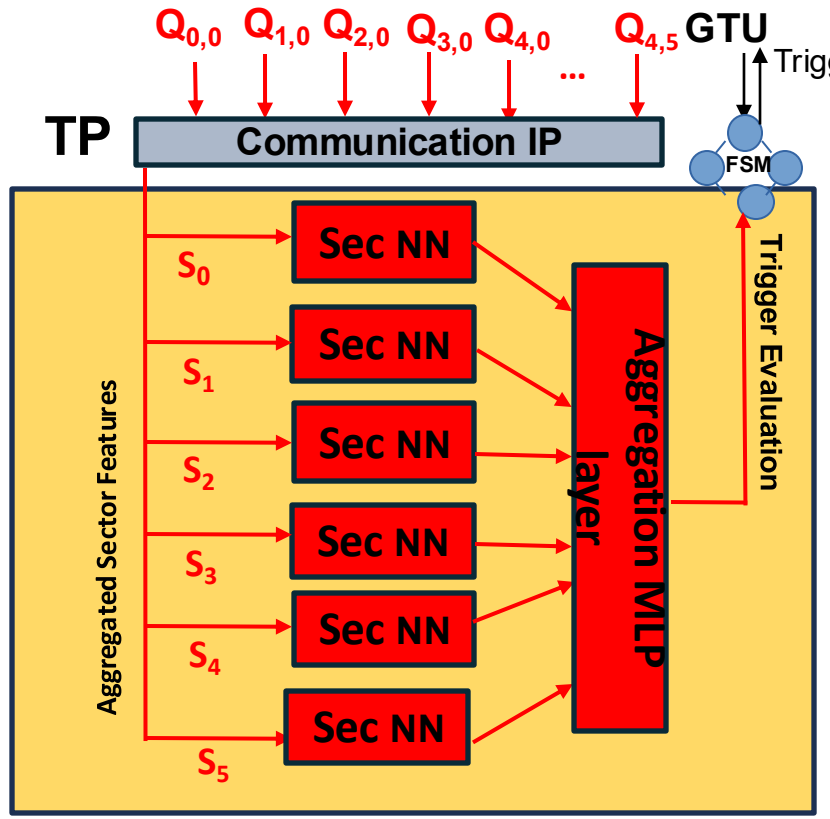
Q_0 To TP 100 GbE

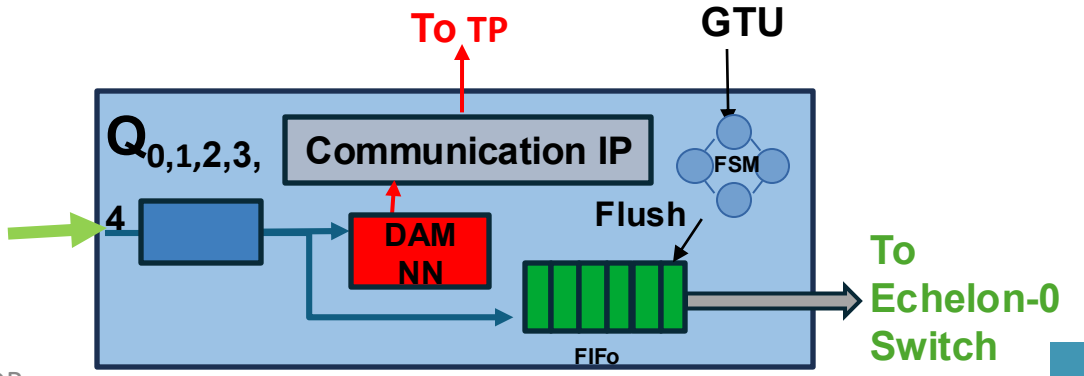
Q_1 To TP 100 GbE

Q_2 To TP 100 GbE

Q_3 To TP 100 GbE

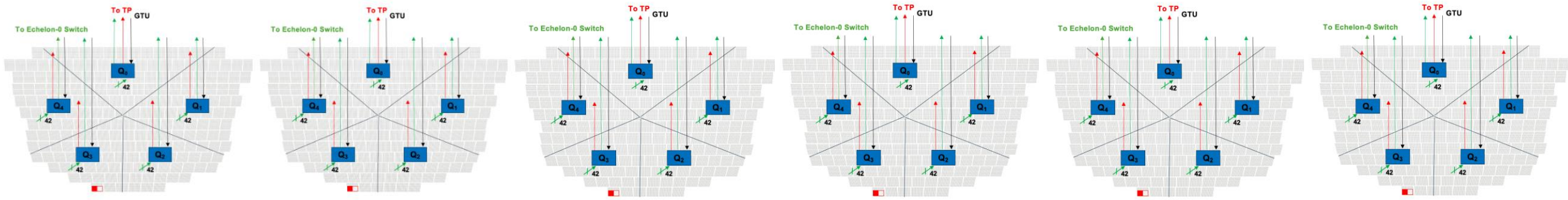
Q_4 To TP 100 GbE

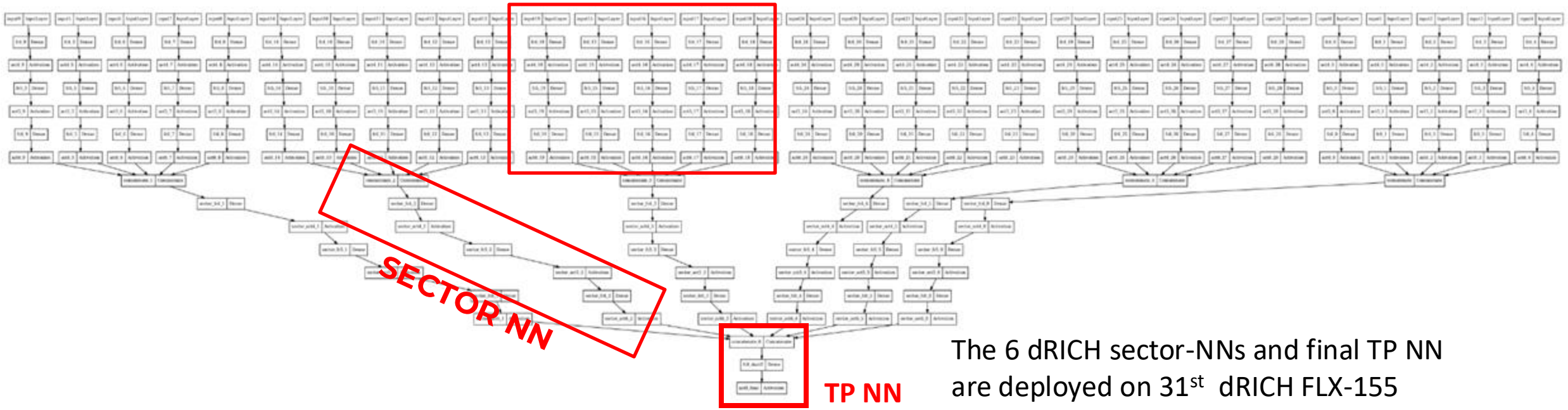




NN deployment model and DAMs

6 dRICH sectors – 5 DAMs/sectors





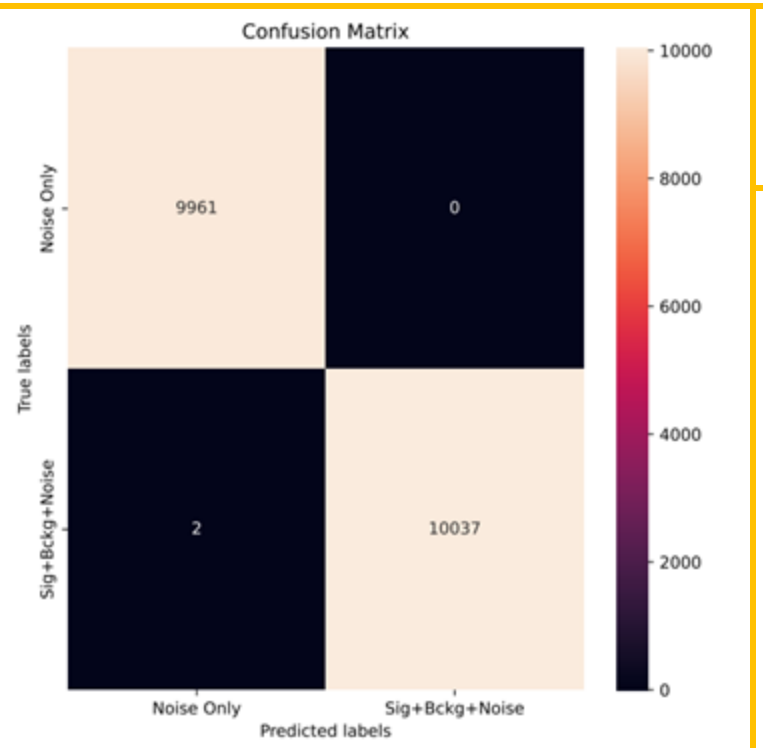
The 6 dRICH sector-NNs and final TP NN are deployed on 31st dRICH FLX-155

Data Reduction performance @ luminosity = 100 fb^{-1}, time window = 10 ns

PRELIMINARY RESULTS

Test with 10000 signal+phys. background (P=Positive) + 10000 pure noise events (N=Negative)

KERAS MODEL



- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.997
- Purity = TP/(TP+FP) = 0.995
- Efficiency = TP/(TP+FN) = 0.999

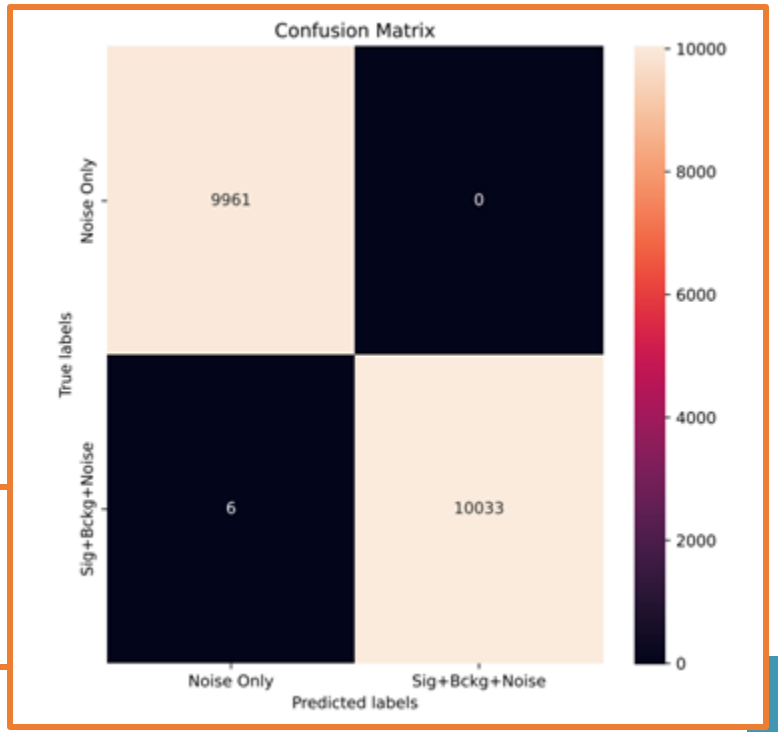
*Take home message

Preliminary result indicate DAM filter could comfortably provide ≫ 5 data reduction factor

Model Quantization

- Inputs, Activations: fixed point<16,6>
- Weights, Biases: fixed point<8,1>

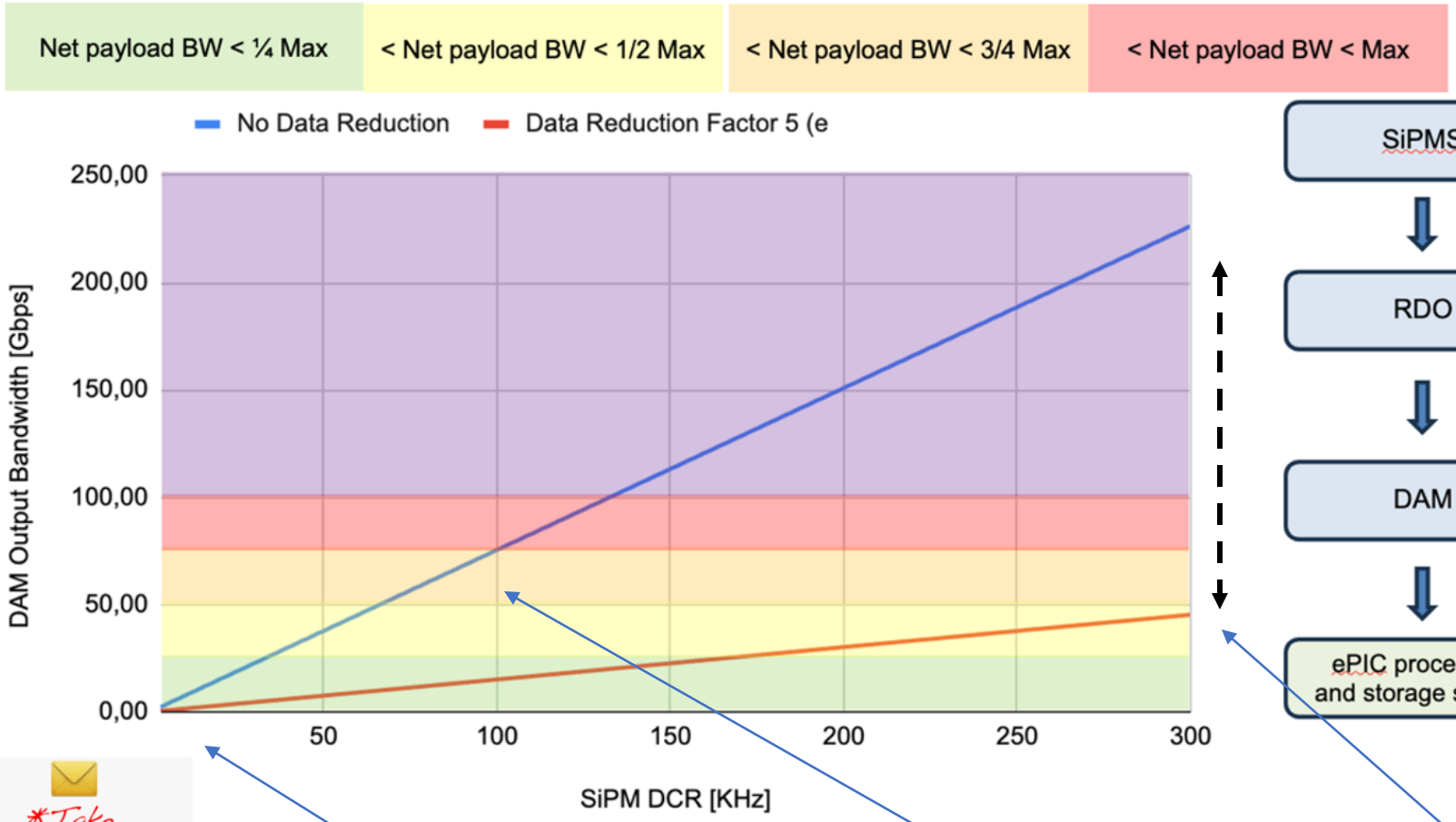
QUANTIZED MODEL

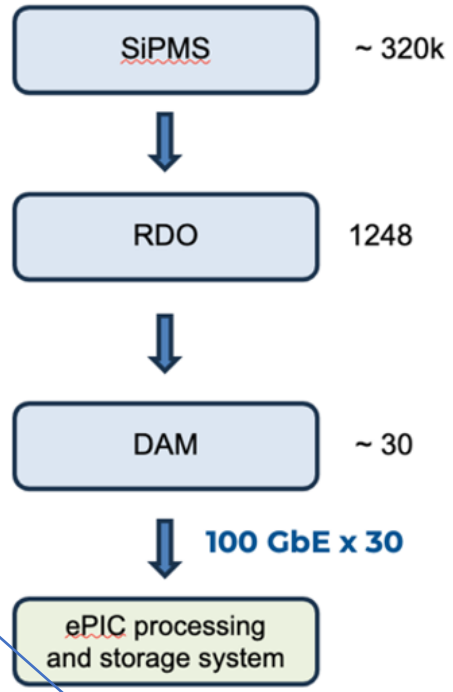


parameterization of DCR background included

- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.997
- Purity = TP/(TP+FP) = 0.994
- Efficiency = TP/(TP+FN) = 0.999

Re-cap on dRICH Output bandwidth





*Take home message

Data reduction factor (RF) five can be achieved via shutter or provided by NN or ext. trigger or a **combination** of them.

$$RF_{shutter} \times RF_{TP} = 5$$

Example:

- shutter window 5 ns → RF=2
- TP RF=2.5

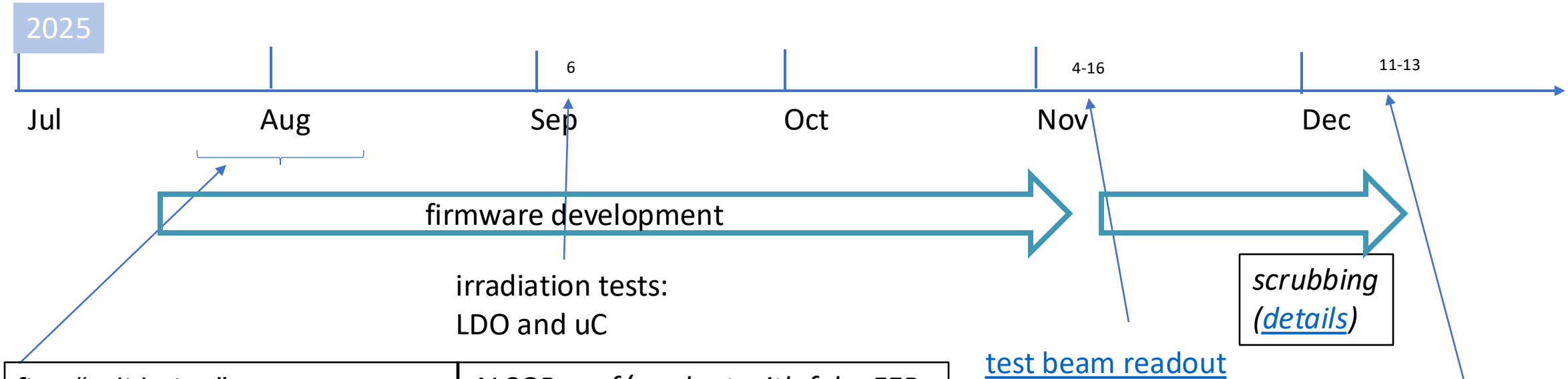
*Take home message

Remember always at day zero dRICH starts with DCR = 3 kHz! Commissioning/first operations will allow tuning of shutter/TP etc.

without data reduction with a 100 kHz DCR we are close to DAM bandwidth limit

a data reduction factor 5 allows us to stay safe up to the 300 kHz limit

Plannning and validation tests (2025)

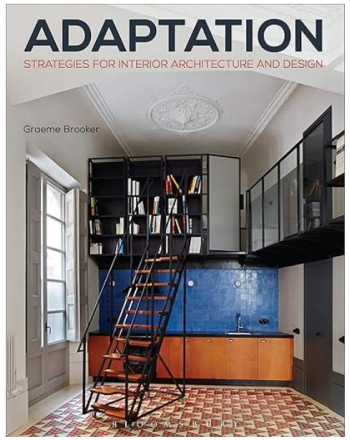


Next steps/challenges for dRICH RDO

During 2026 we need:

- full validation of current prototypes including irradiation tests
- fix any mistake found

- design adaptations due to integration challenges that may arise (cooling, space, FPGA resources, ...)



- validate communication with DAM (implementing a FELIX-supported comm. protocol)

FELIX

Plannning and validation tests (2026)

2026

Jan Feb Mar Apr May Jun Jul Aug Sep Oct Nov Dec

firmware / software development

remote programming
clock reconstruction – FELIX-supported comm. protocol (FULL with GBT on host)
details

second irradiation
test “full RDO”
@Trento

last test beam
readout full PDU
(RDO+ALCOR64)

irradiation tests:
full PDU @CHARM

[details on 2026 irradiation tests]

RDO communication tests with DAM

Developing a RDO testbed to test RDO production (preparing for 2027 RDO production!) [details]

requirements | specs | design | layout and production | validation

Details in backup

Final information and conclusions

- No substantial updates for **requirements** with respect to the ones presented in PDR 2024
- **Cost**: preliminary offers for production (two companies) evaluated. Total cost ~ 700 k€ + VAT (details in backup)
- **Schedule**: one-year shift: pre-production in 2026, production in 2027 (in line with EIC project program)
- **ESH&Q and QA** considerations: as last year. Note funding for RDO testbed asked for 2026 to INFN.

INFN Bologna is following frontend DAQ (RDO) and INFN Rome backend DAQ (FLX-155): hardware is finally available
First weeks of tests on RDO are very promising, no show-stoppers identified
dRICH frontend DAQ and backend DAQ are much closer to finally meet

INFN BO dRICH RDO core team:
- P. Antonioli, physicist
- D. Falchieri, electronic engineer
- S. Geminiani, PhD student
- L. Rignanese, electronic engineer
- G. Torromeo, electronic technician

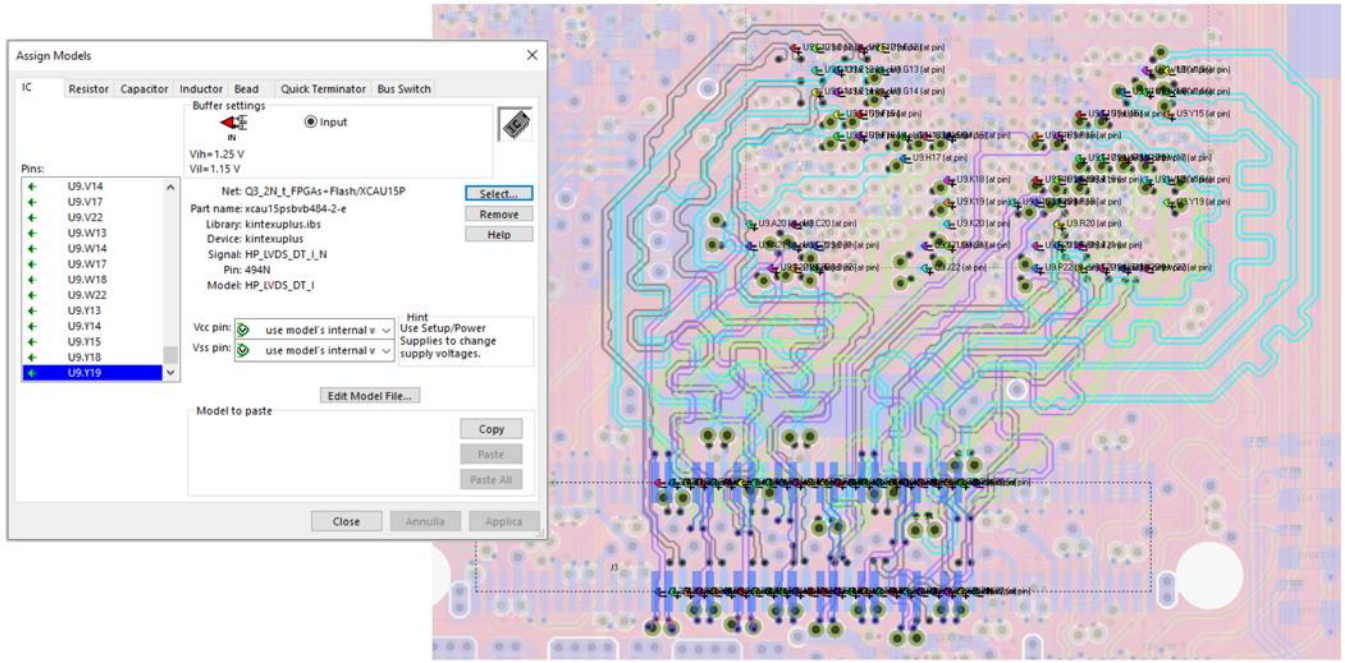
RDO team works obviously very closely with INFN-TO (ALCOR), INFN-FE (detector box), INFN-BO (SiPM and PDU coordination), INFN-RM1 (backend DAQ) colleagues. INFN-GE and INFN-TS are contributing to detector simulations.

Backup

Design finalization on layout and cross-checks

optimization of FPGA pin assignment vs layout

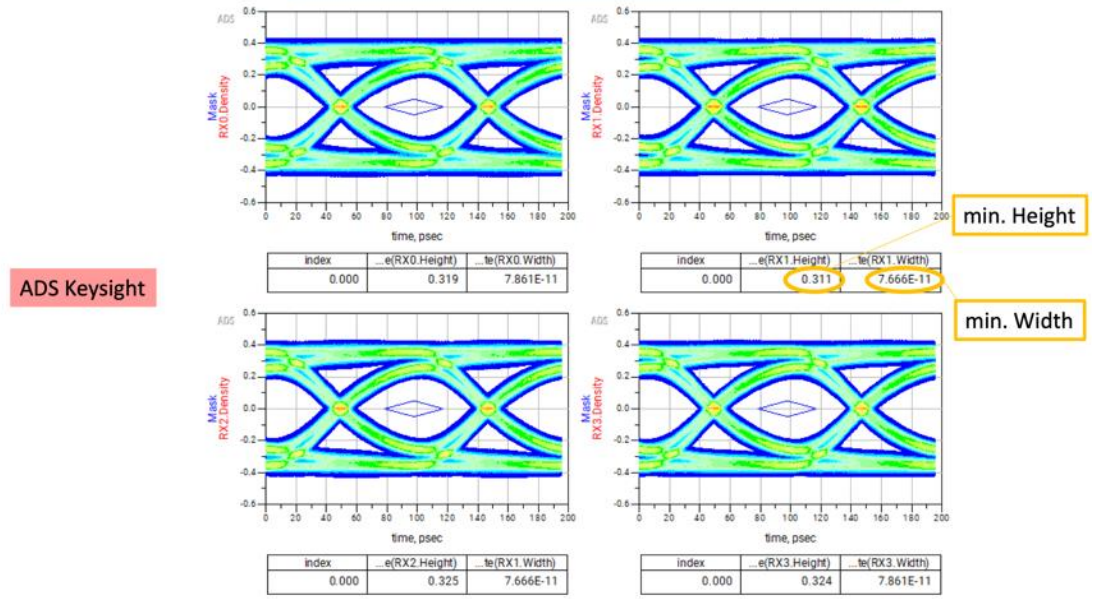
Routing of 32 lanes ALCOR bus



high-speed differential line modeling

ARTEL S.r.l.
PCB ENGINEERING

4 Channels TX ARTIX Ultrascale+ GTH to VTRX+ receiver
AC coupling termination 100 Ω dielectric FR408HR



ADS Keysight

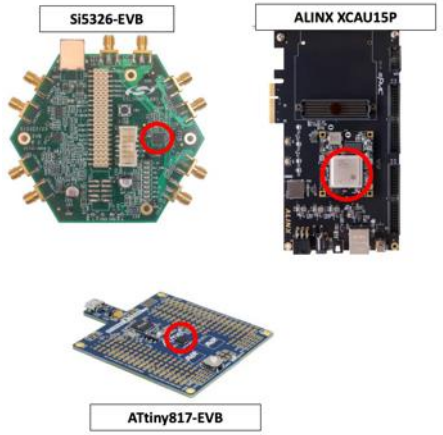
min. Height

min. Width

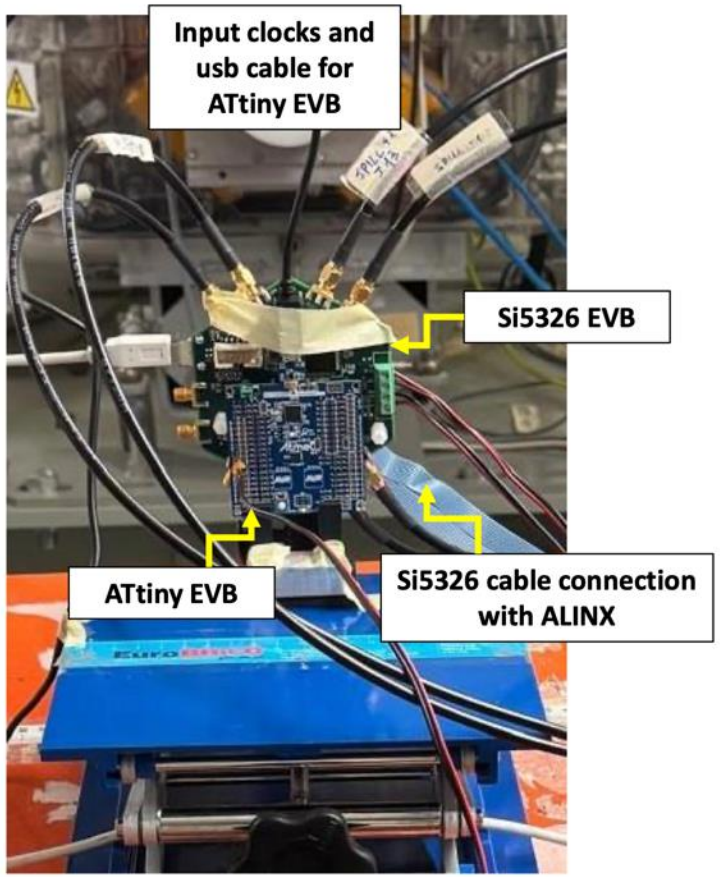
Much more details in D. Falchieri's presentation at WG Electronics and DAQ/eRD109 (April 2025)

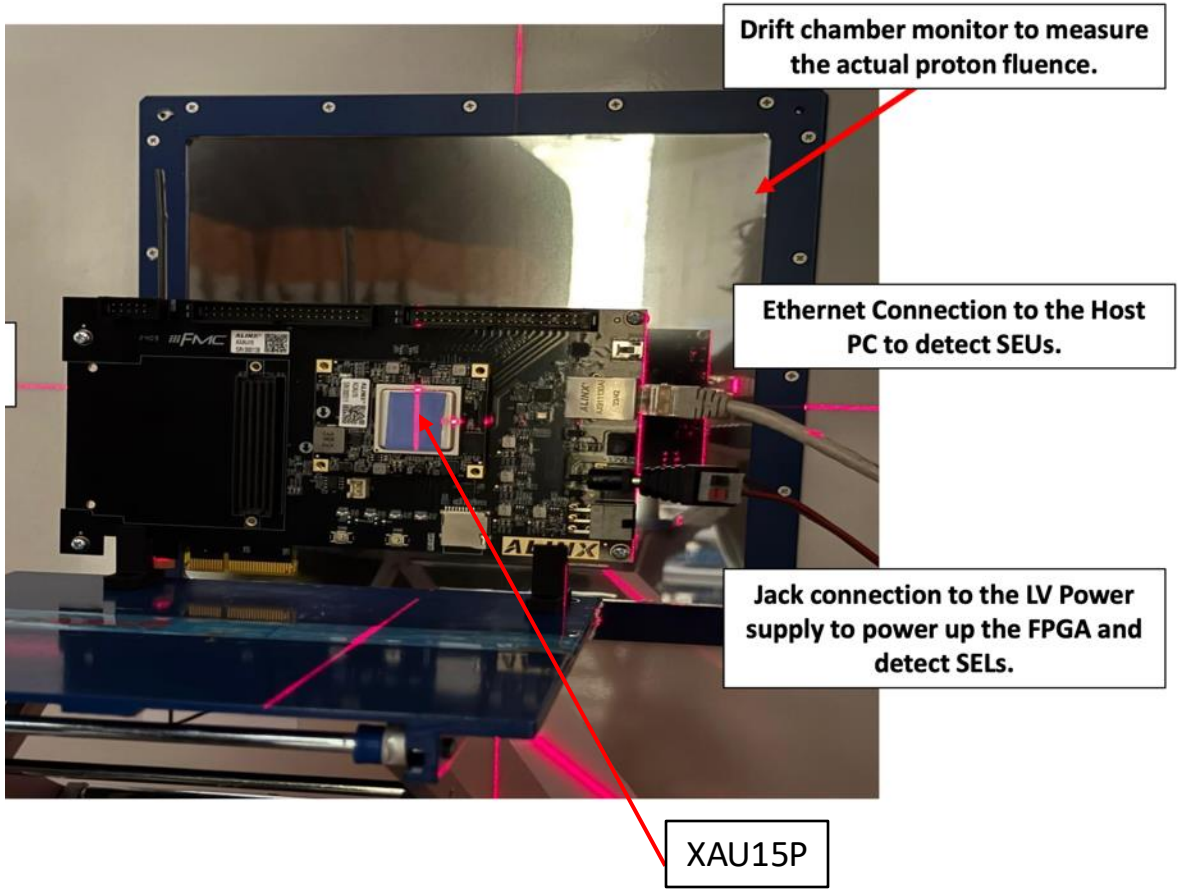
Irradiation tests (I)

- Waiting for full RDO we tested several key components: PLL (Si5326), uC (ATtiny417) and AMD FPGA (AUX15P)
- irradiation with a proton beam at Centro di Protonterapia in Trento / December 2024
- TID_5 ≅2.3 krad (1000 fb^{-1}) and Φ(h>20 MeV) ≅700 Hz/cm^2 (including a safety factor 5)



Note TID_5 estimates increased by a factor 3.5 since PDR 2024





See presentation by S.Geminiani @ePIC Collaboration meeting (Jan 2025)

Irradiation tests (II)

MTBF= Mean Time Between Failure
SEU = Single Event Upset
SEL = Single Event Latchup

from conclusions presented in January:

1. We integrated $\mathbf{TID \sim 2.8 \cdot TID_5}$ for the AU15P, $\mathbf{TID \sim 10 \cdot TID_5}$ for the ATtiny and $\mathbf{TID \sim 18 \cdot TID_5}$ for the Si5326.

   No significative cumulative effect or SEL for Si5326 and AU15P, while the **ATtiny stopped working at TID = 23 krad**.

   → **Devices tested up to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID \leq TID_5}$**

2. **Si5326: MTBF = 3.8 h (for 1248 RDOs)** and the jitter analysis showed the **output clock is very stable.**

   → **The RDO AU15P will control the chip configuration every t ≪ 3.8 h.**

3. **ATtiny: SRAM MTBF = 4 h** and **FLASH MTBF > 43 h (for 1248 RDOs)** .

   → **The FLASH MTBF is a safety limit and key RAM registers will be implemented with TMR checks.**

Comments: investigation addendum for ATtiny + first measurements of this kind in ePIC

Irradiation tests (III)

AUX15P

- **Monitored memory: 8/156 kb** of **FF memory**, **3.6/5.1 Mb** of **BRAM** and **33/33 Mb** of **CRAM**.
- **0 SEUs** detected on **FF memory** and **69 SEUs** on **BRAM** after 2560s.
- **70 corrected SEUs**, **11 uncorrected SEUs** and **1 dead link** detected on **CRAM** after 2560 s.
- **No SEL** detected after 3632 s.
- **TID = 6.36 krad (dose rate = 10-500 rad/min)** after 3632 s.

FF memory (limit @ 95% C.L.): $\sigma < 3.5 \cdot 10^{-14} \frac{\mathrm{cm}^2}{\mathrm{bit}}$
MTBF (156 kb) in the dRICH system (1248 RDOs): > 3.6 min

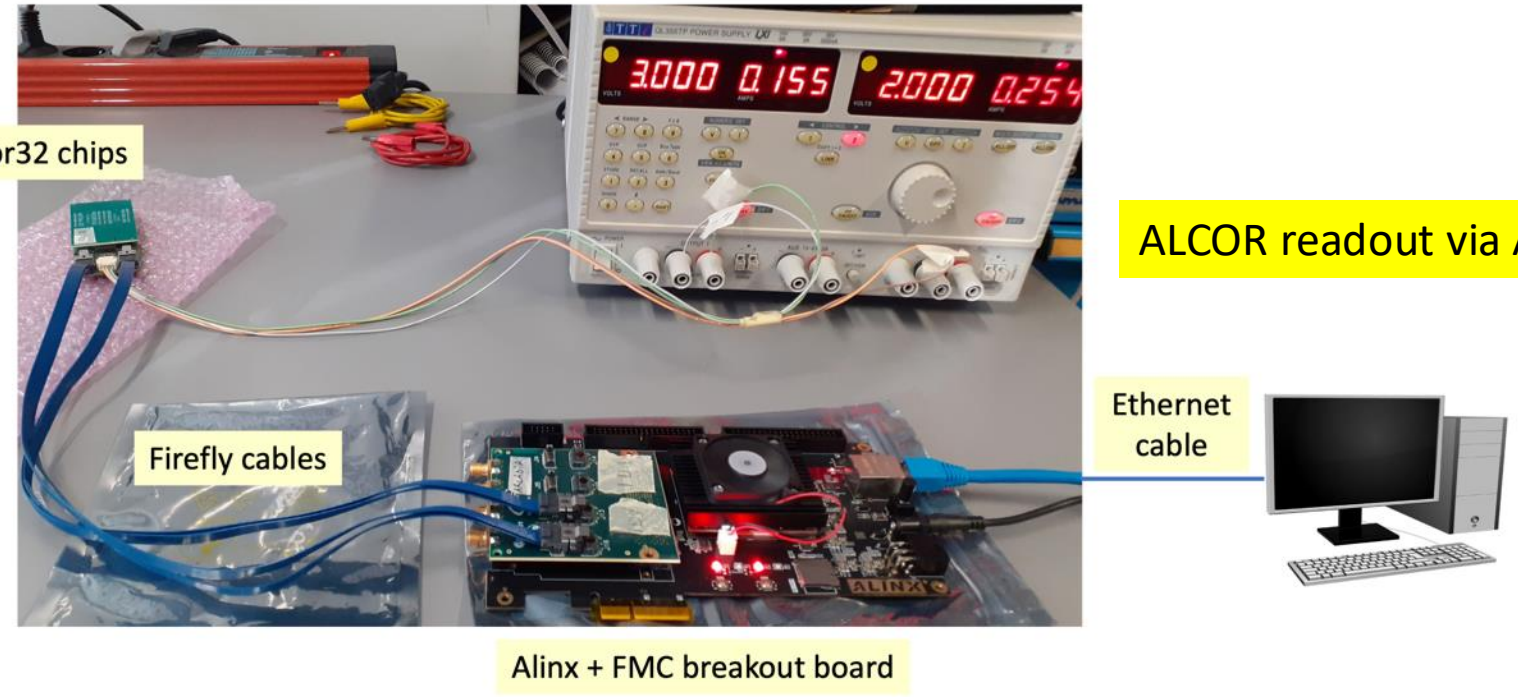
BRAM: $\sigma_{\mathrm{SEU}} = (1.78 \pm 0.23) \cdot 10^{-15} \frac{\mathrm{cm}^2}{\mathrm{bit}}$
MTBF (5.1 Mb) in the dRICH system (1248 RDOs): 2.1 min

SEU cross sections and MTBFs (33 Mb) in the dRICH system (1248 RDOs) for CRAM :

	$\sigma_{\mathrm{SEU}} \left(10^{-16} \frac{\mathrm{cm}^2}{\mathrm{bit}}\right)$	MTBF (min)
COR	(1.96 ± 0.25)	2.9
UNCOR	$(3.09 \pm 0.94) \cdot 10^{-1}$	18
TOTAL	(2.30 ± 0.28)	2.5

RDO firmware progresses (I)

- pin placement for layout design
- intense use of [ALINX AUX15P evb card] (same FPGA) as RDO GYM (waiting for real cards!)



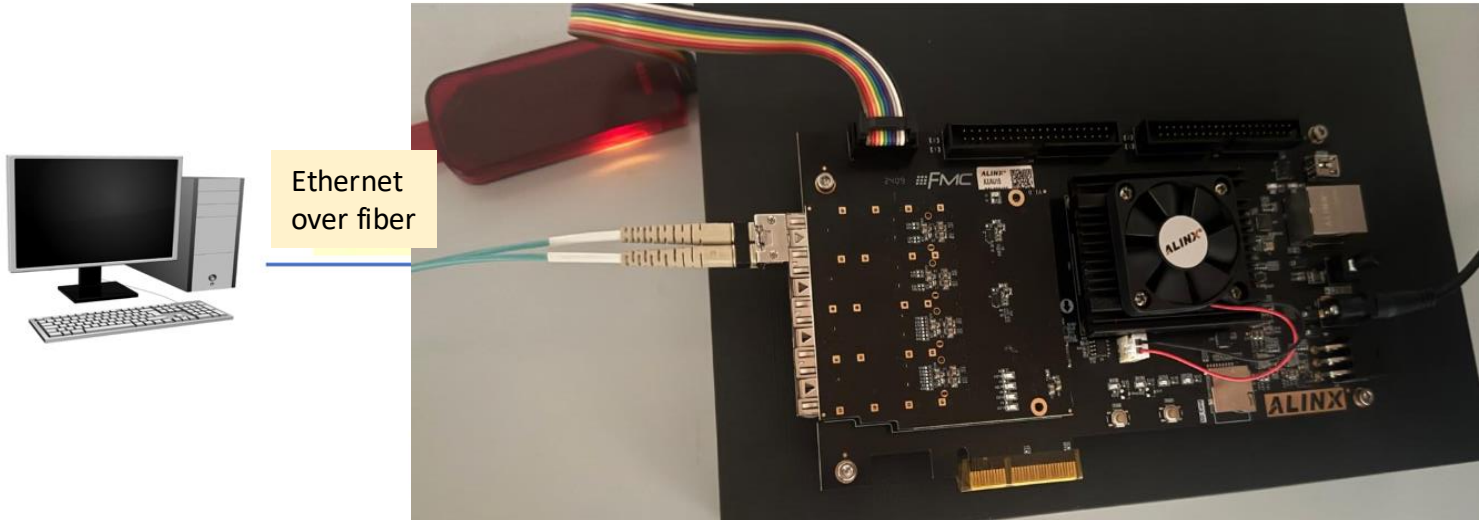
ALCOR readout via AUX15P

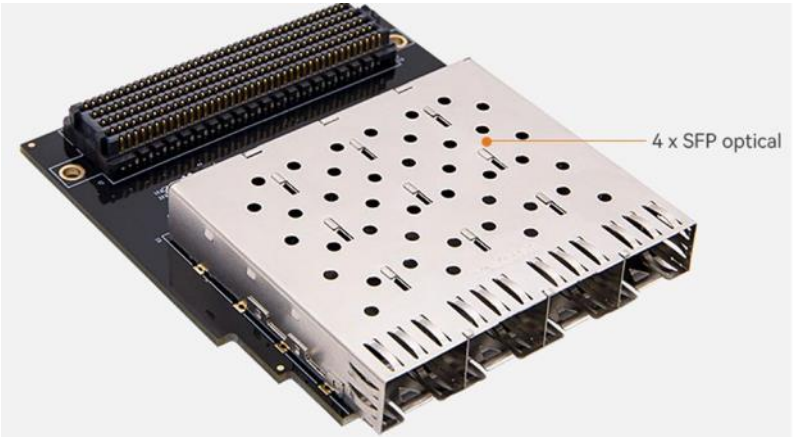
In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI and we can correctly receive the data

successfully ported KC705 FW (reading ALCOR) to AUX15P including SERDES
More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (May 2025)

RDO firmware progresses (II)

- pin placement for layout design
- intense use of ALINX AUX15P evb card (same FPGA) as “RDO GYM” (waiting for real cards!





successfully implemented IPBUS communication over optical link (commercial SFP) → configuration foreseen for test beam

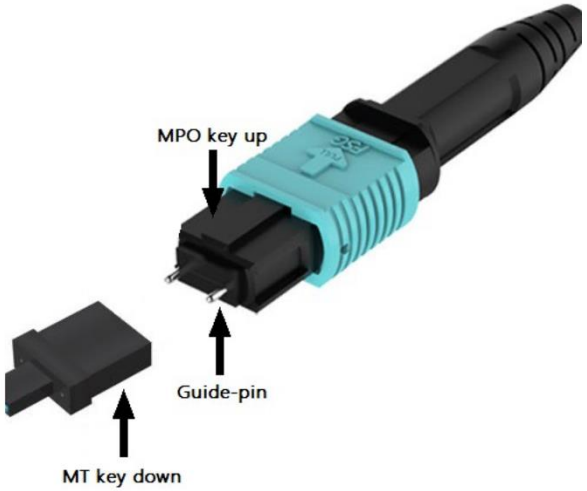
“collecting pieces of the firmware needed on RDO”

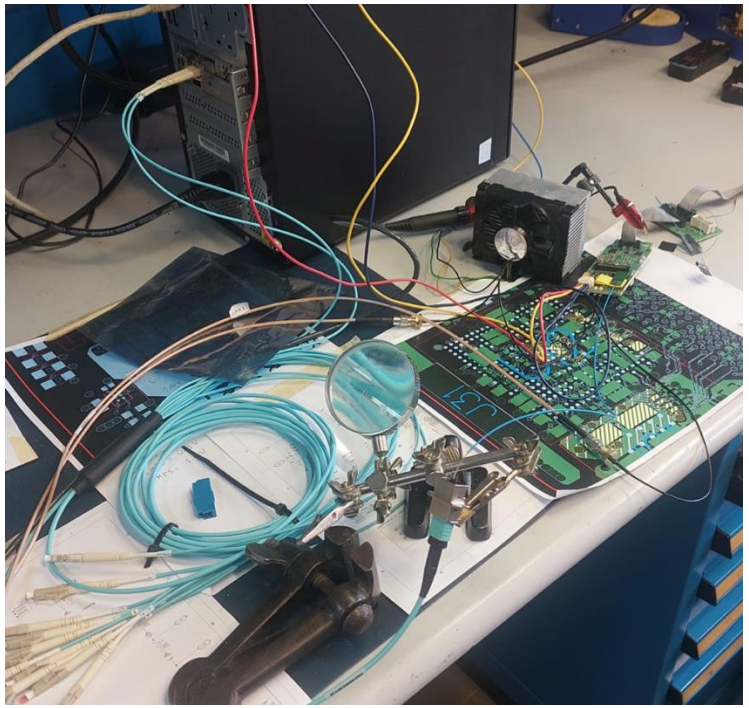
initial debug on prototypes

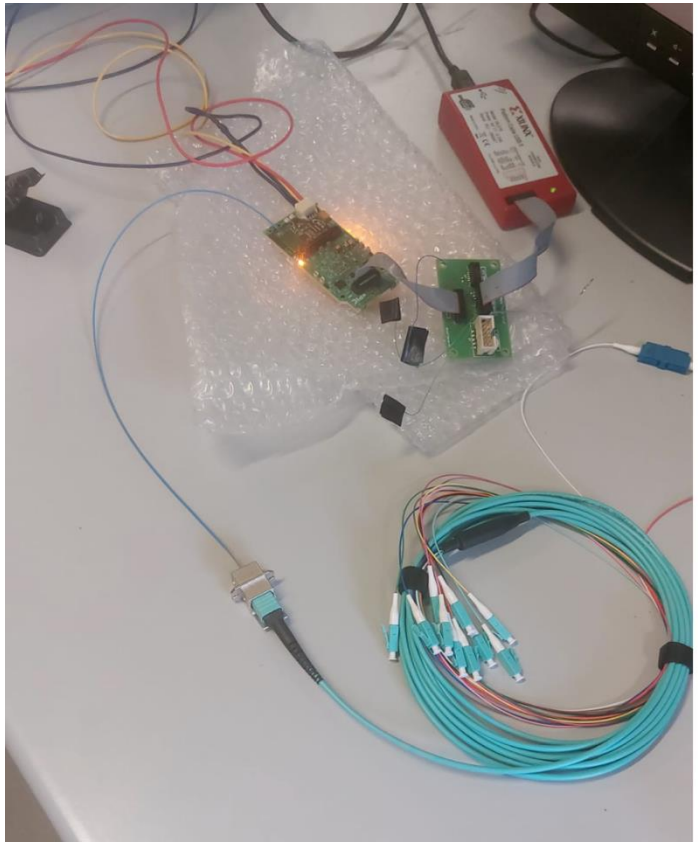
initial debug included the fixing of several problems (“minor issues”)

- mounted 2 Si5319 instead of a Si5319 and a Si5326 → we will do reworking
- mounted “wrong” charge pump component → fixed changing some resistors, we will do reworking
- a short due to a capacitor (layout error): bypassed
- somehow difficult the pairing of VTRX+ MT connector with MPO and then with fibers (we had initially the wrong fanout patchcord)

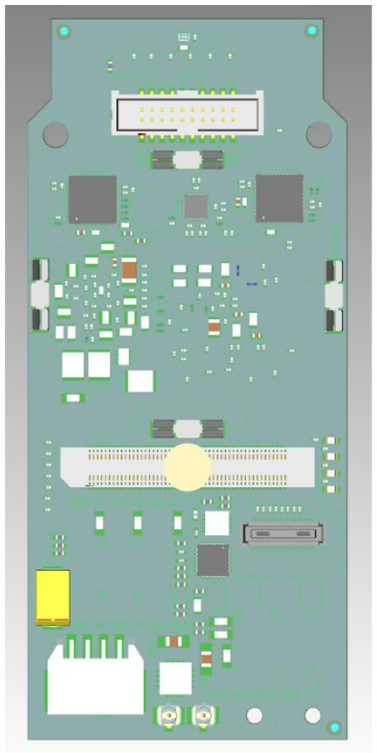
details







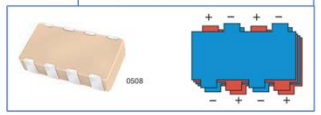
initial debug details



Top layer

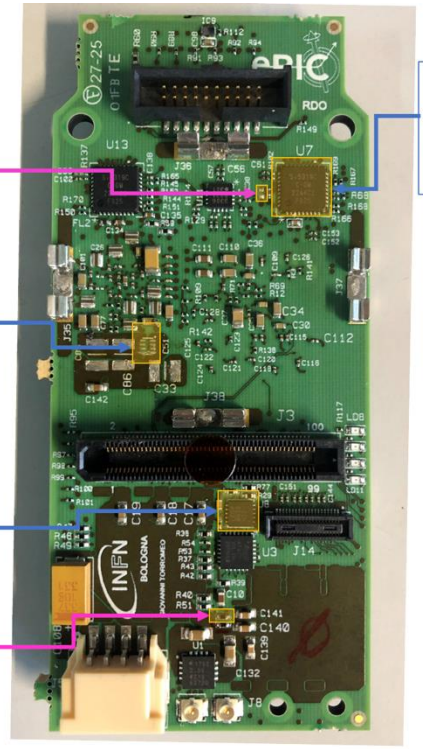
FL1 removed to not power U7

Problem with footprint of **C51**

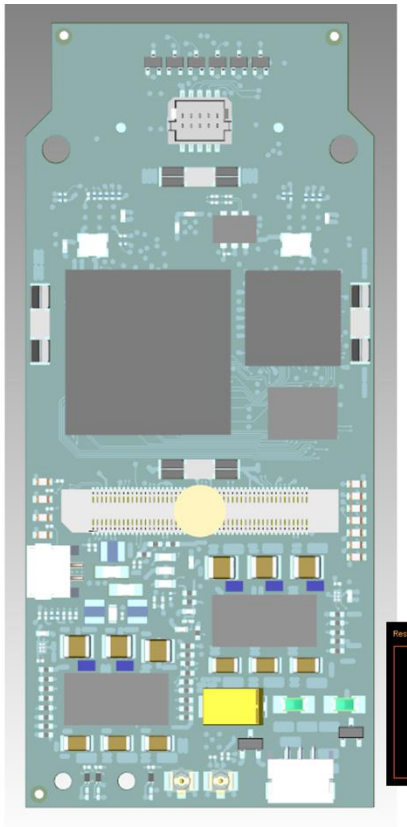


Problem with **U8** LTC3203BEDD-PBF

R19 1.5K changed to 2.2K to correct VOH level with wrong U8 (charge pump a 5V)

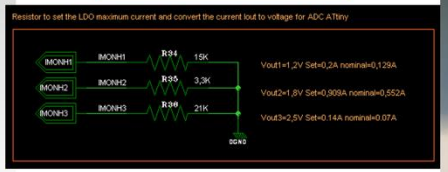


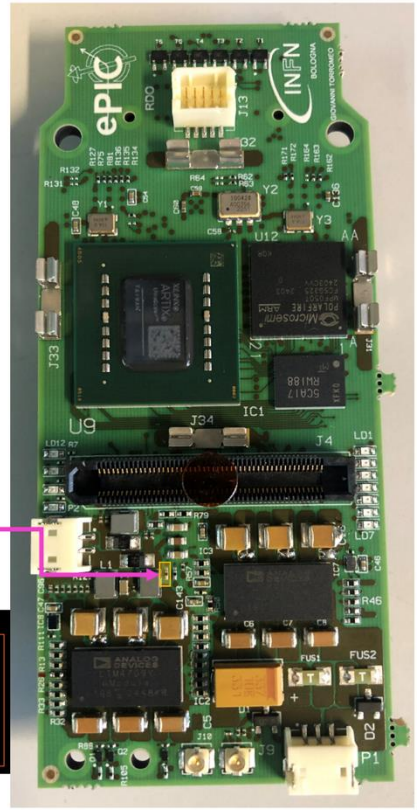
U7 Si5319 instead Si5326



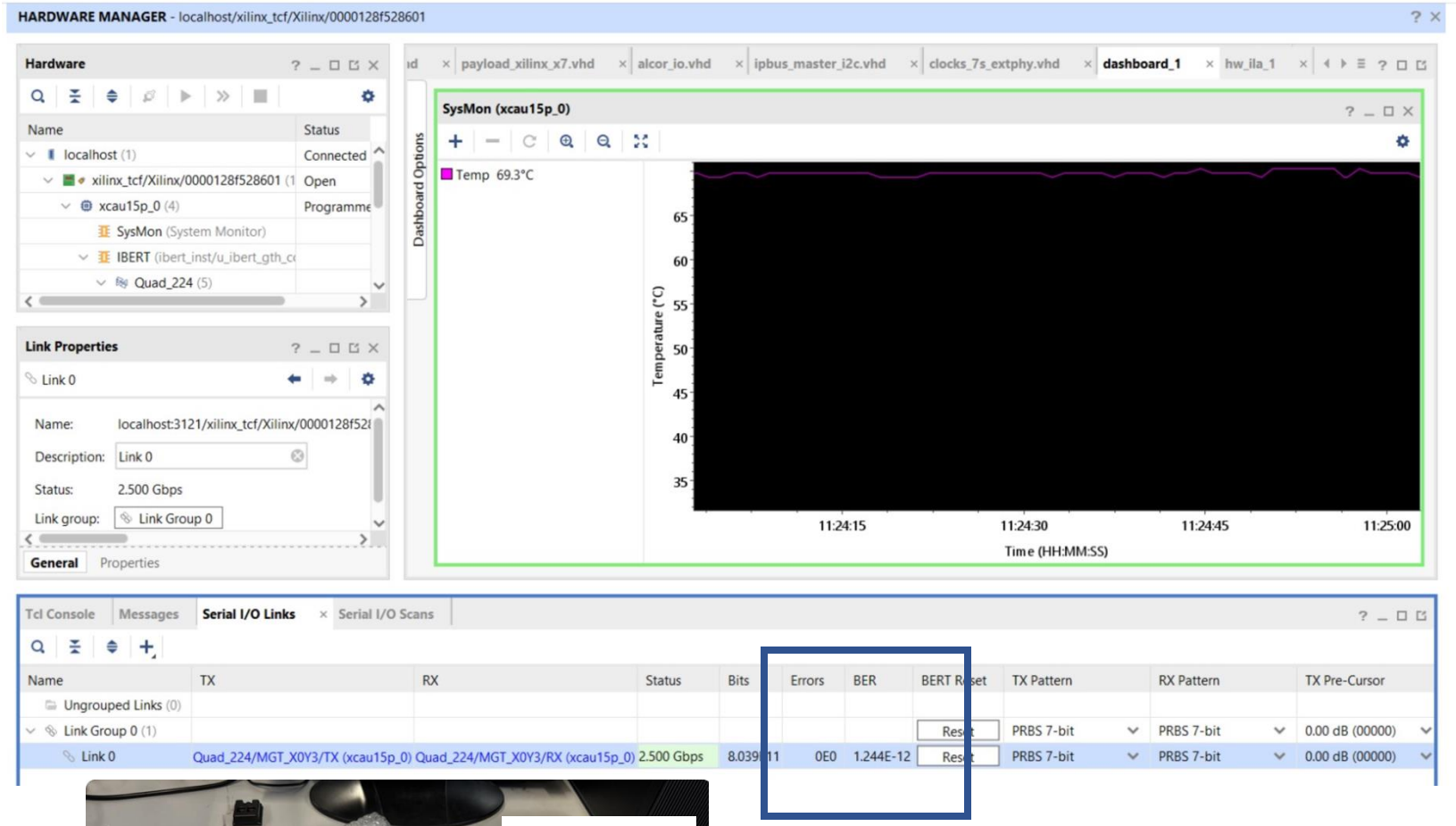
Bottom layer

R34 15K changed with 8.2K to set 1.2V Iout limit

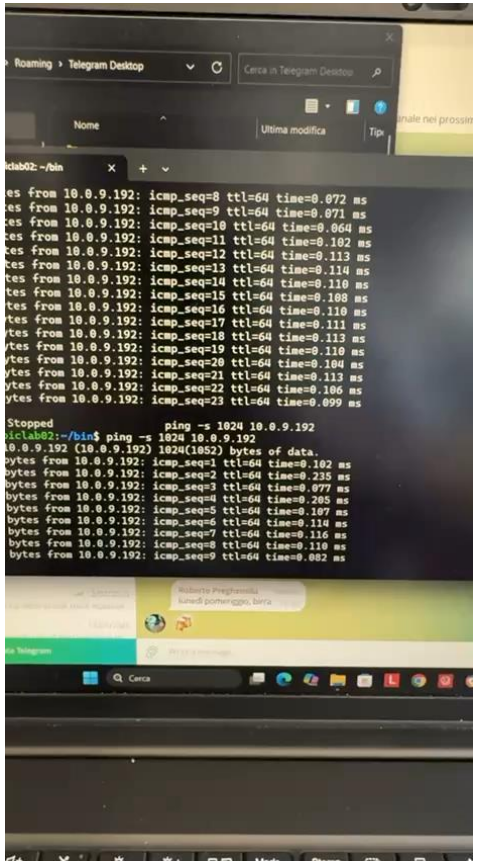




checking the optical link



first ping to dRICH RDO via VTRX+



which firmware flavour in ePIC ?

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

Table of available link “flavours” in FELIX cards and FPGA resources usage (courtesy by A. Lonardo)

FELIX FPGA resource usage

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

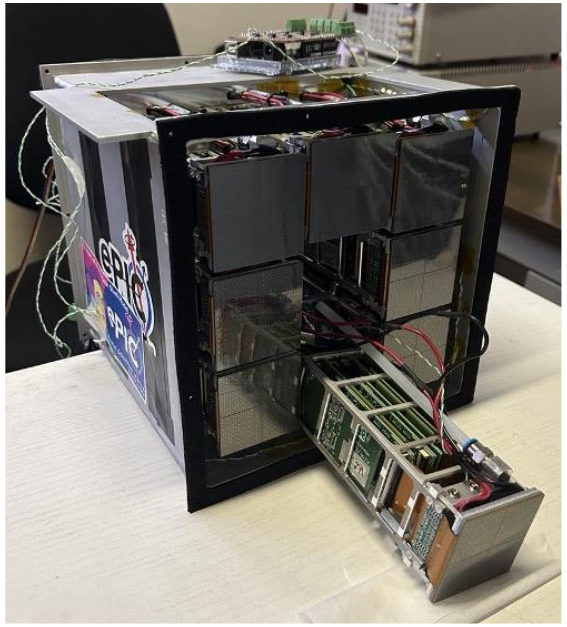
Note dRICH aims to use FLX-155 resources too for data reduction!

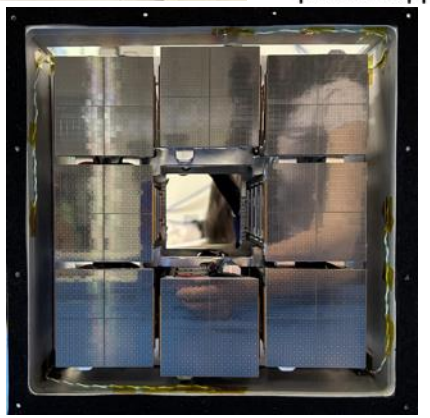
See A. Lonardo talk at ePIC Jan 2025 meeting

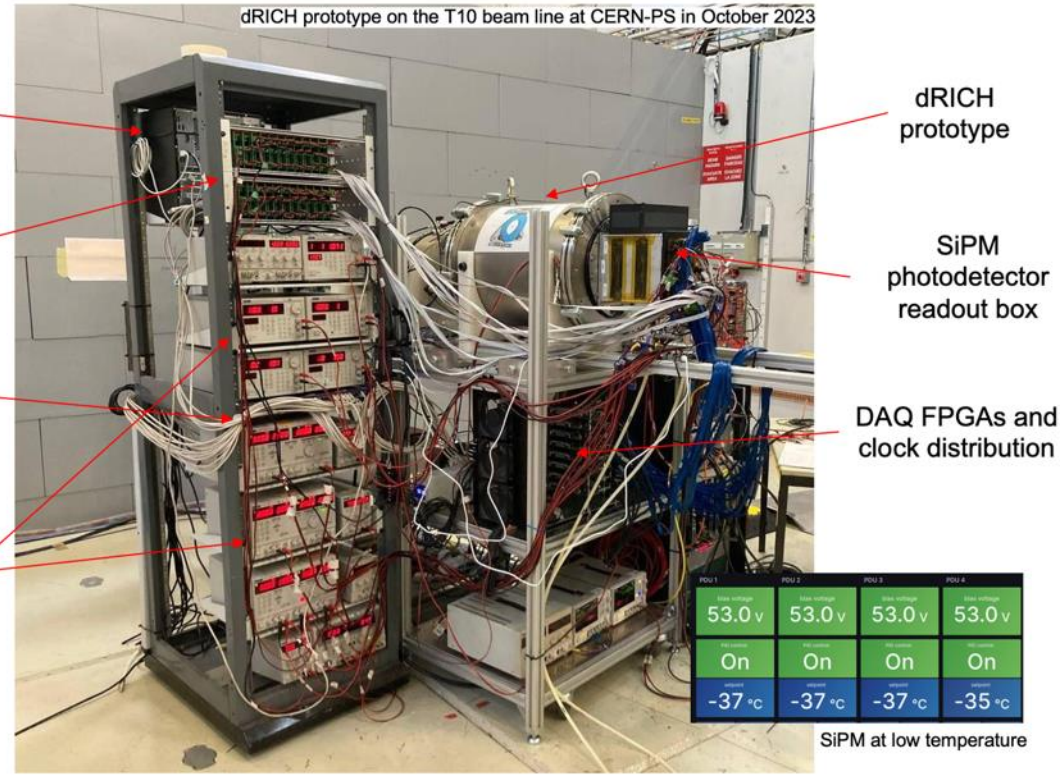
Update:
Rome1/2 has now the FLX-182 sent by BNL up and running!

- scale up to 48 lpGBT links might be a problem for FLX-155?
- as dRICH we use just the VTRX+ tranceiver not the lpGBT ASIC so lpGBT protocol not strictly needed but we would recommend to use anyway one of the existing flavour. FULL will be tested, agreement within ePIC

scale up to a test beam up to 2 kchannels





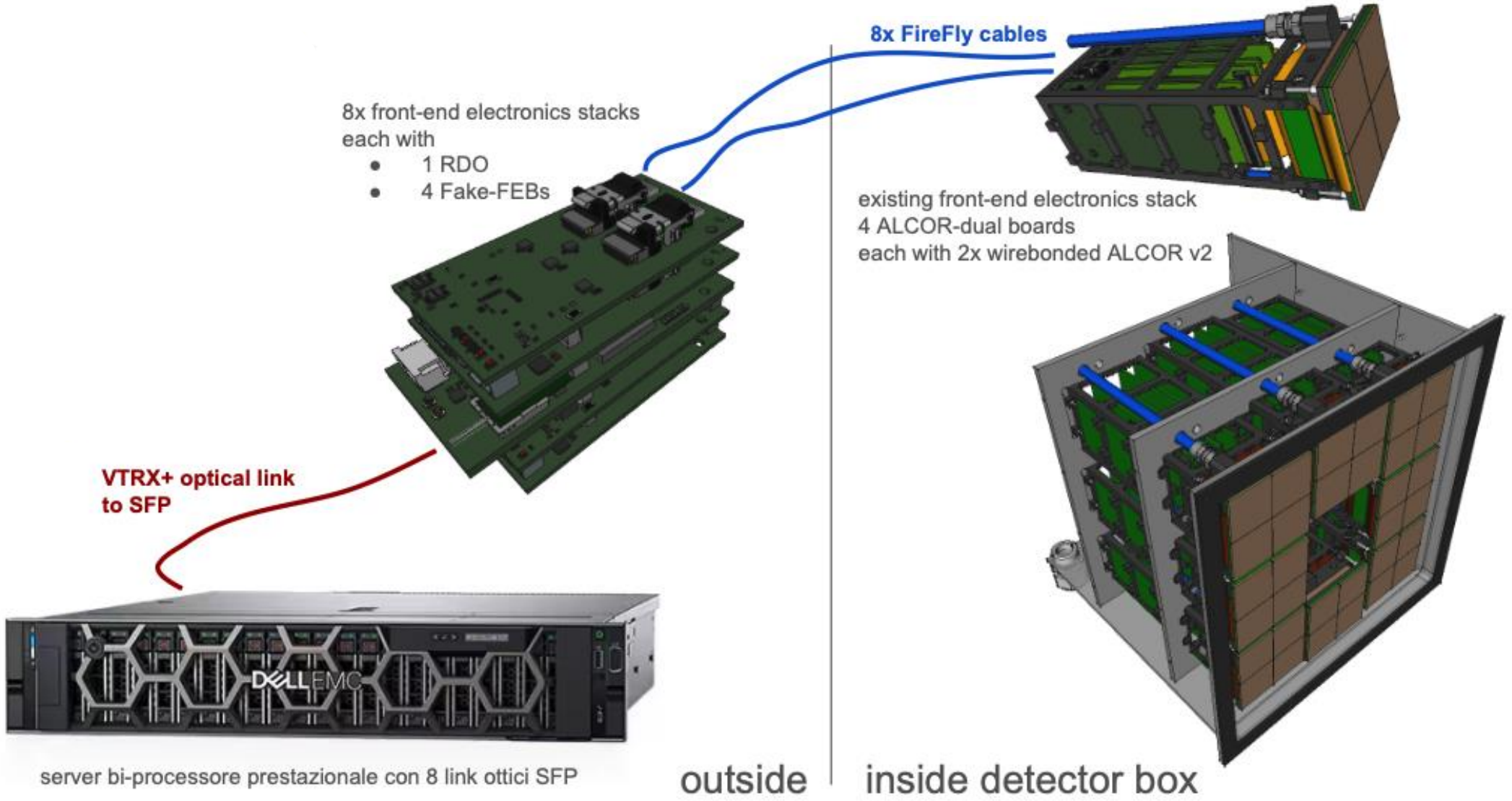


11 KC705 FPGA boards in parallel ➔ 64 AlCOR chips ➔2048 SiPMs

next step is bringing readout inside the PDU (RDO comes after)

RDO setup for 2025 test beam (Nov. 2025)

- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- ”fake-FEB” (ALCOR v2.1 adaptor) : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)

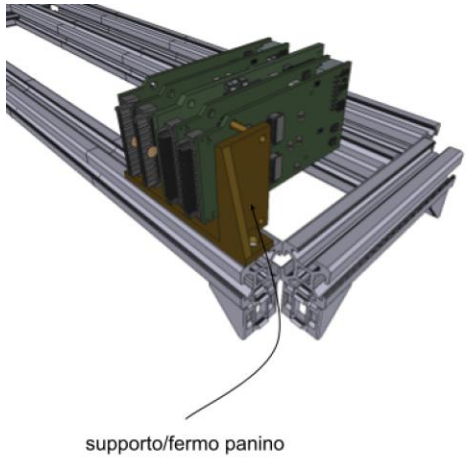


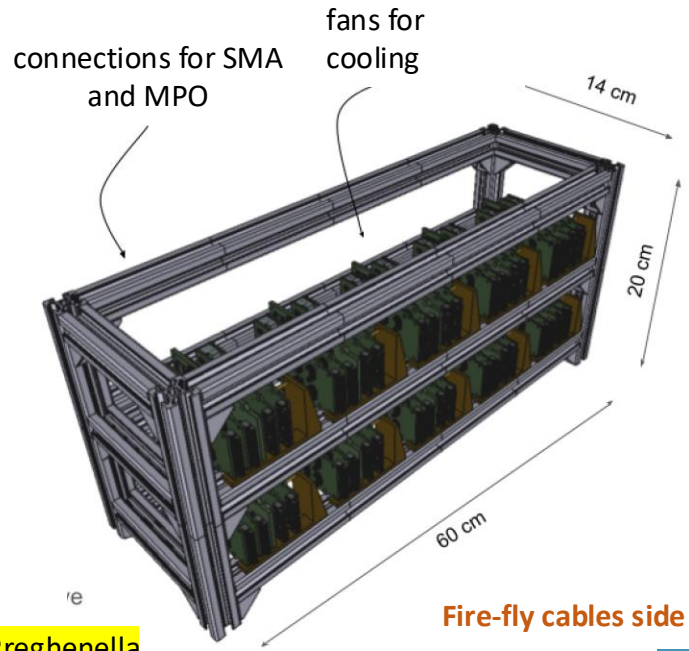
RDO next steps preparing for test beam 2025

1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I^2C sensors
3. I^2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling
6. A mini rack: 8 RDO + fake-FEB on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming





courtesy R. Preghenella

Fire-fly cables side

RDO next steps for test @TIFPA (December 2025)

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Communication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-FEB connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

RDO next steps towards full ePIC DAQ

- Check noise (if any) from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction
- Clock at 394 MHz/ ALCOR@394 MHz (only with ALCOR v3)
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link using AUX15P/ALINX + JLab card
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in magnetic field (PDU)
- PDU in detector box etc…

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- **testbed setup** for testing RDO production

RDO power consumption estimates

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0150	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

Device	Total Power (W)	Area (mm2)	W/mm2
AUX15P	2.455	361	6.80
MPF050T	0.438	121	3.62
LDOH	1.155	72	16.04
LDOL	1.034	72	14.36
SI5326	0.457	36	12.70
SI5319	0.457	36	12.70
VTRX+	0.193	100	1.93

FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**

Measured consumption with RDO prototypes = 4.3 W (not yet tested with ALCOR readout on + scrubbing)

RDO power consumption estimates

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
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		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
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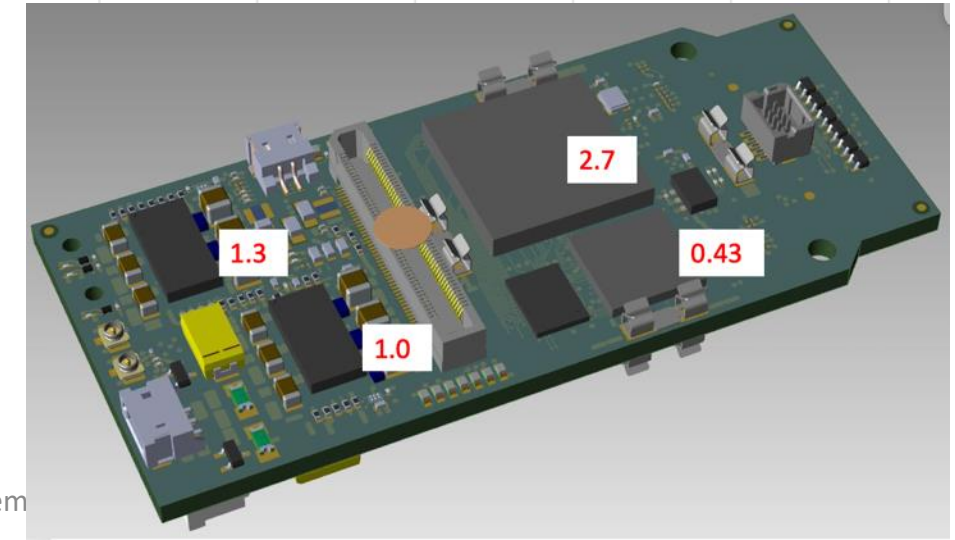
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

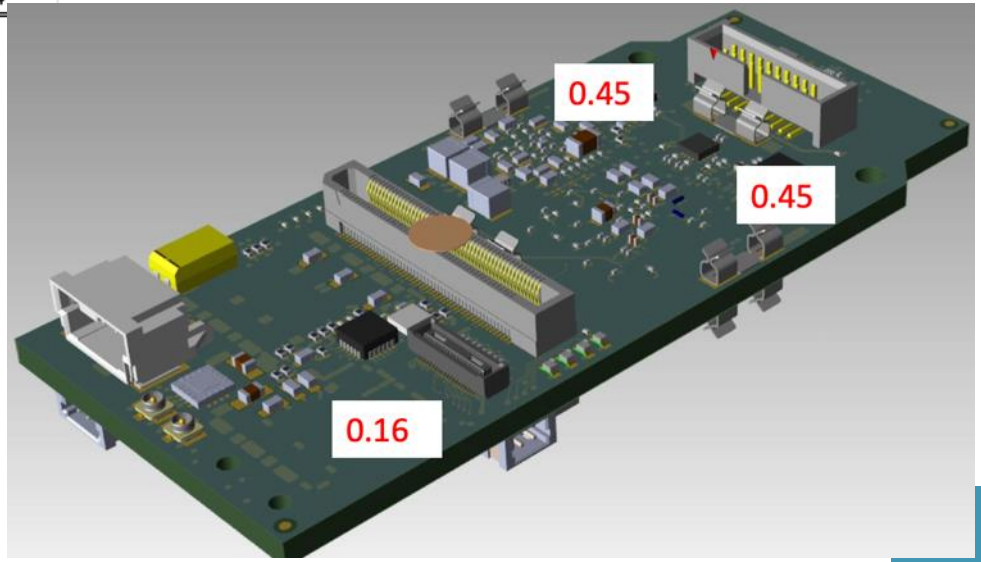
Actual FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**





Irradiations (for RDO, components, SiPM…)

Why we still need irradiation tests?

- first full RDO irradiation test (Dec. 2025) will be learning exercise: it is first scrubbing test
- with firmware more advanced we need to check behaviour of the card – link stability etc.
- 2026 is the year to test whole PDU: CHARM facility (CERN)
- [need to test ALCOR64]
- [need to irradiate a whole SiPM matrix to test then annealing in a true PDU]

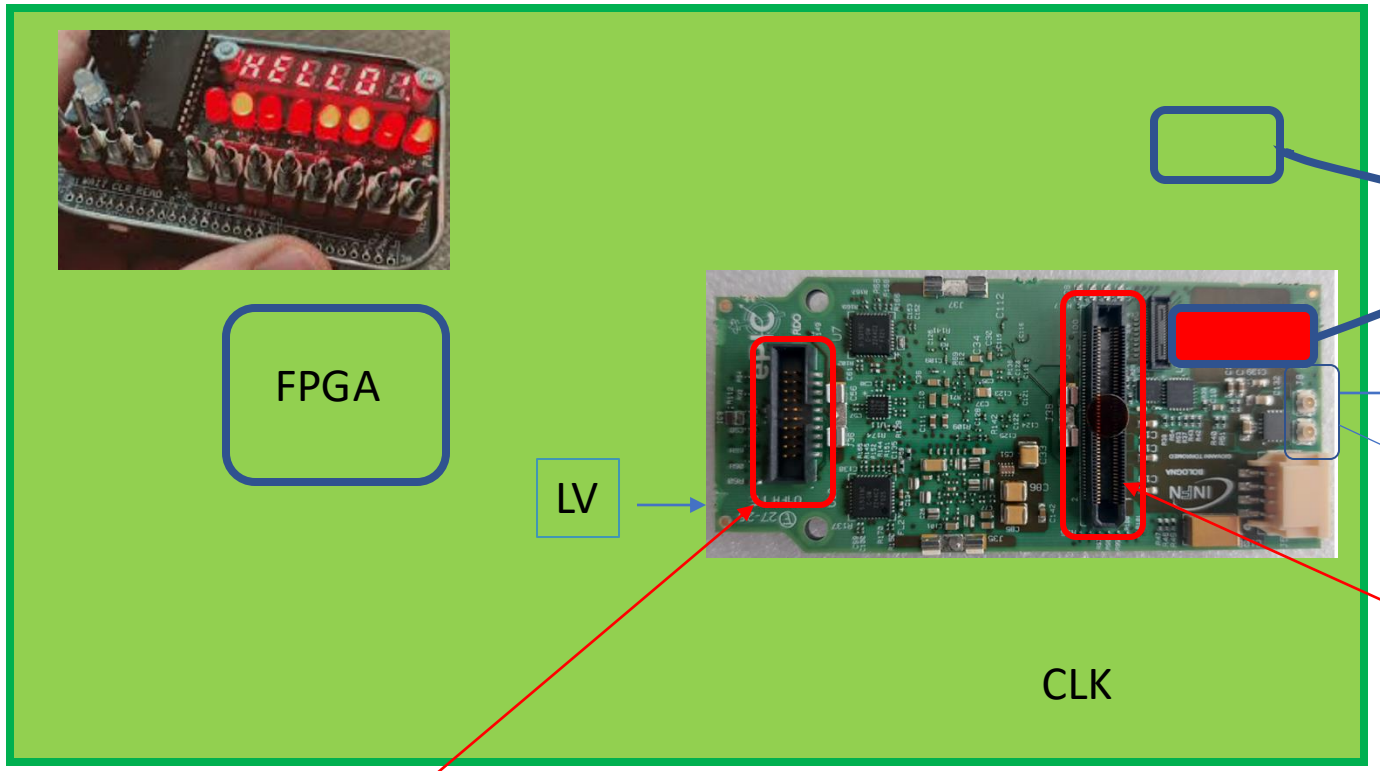
Applications for beam facilities for 2026

- INFN TIFPA c/o hadron therapy center (Trento) 3 sessions (or 2 but extending one to three days): RDO, ALCOR64 (FEB)
- CHARM (CERN), 1 session ("whole PDU). check "everything" plus we use a realistic mix of hadrons
  - whole PDU → we test all materials (glues, screws, connectors, etc.)

RDO production: a RDO testbed for 1500 cards

preparing for RDO production in 2027 we will invest time preparing carefully budgeting (currently cost foreseen 680 k€ + VAT) and a **RDO testbed card** to test thoroughly, quickly and effectively the 1500 boards (and load the firmware)

display + switches to run specific tests



Basic idea:
the TB FPGA FW verifies all RDO I/Os are ok before moving to
a) VTRX+ installation – link check
b) testing with FEB
c) testing in a PDU

RDO is plugged on TB using ALCOR BUS botttom connector

EXT CLK (UFL to SMA)

a flat cable connected to (ALCOR BUS top connection)

a flat cable connected for FPGAs/atTiny programming

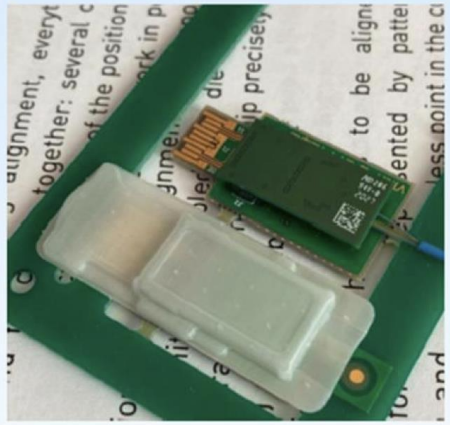
Updated RDO cost estimates

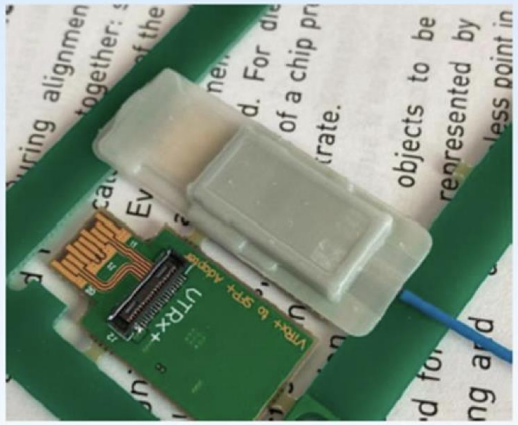
- Production cost : 267.1 k€ (1500 cards + all components not including FPGAs and VTRx+, mounting) [OFFER]
- FPGA: 256 k€ (ARTIX) + 187 k€ (PF) [simple estimate via Mouser/RS distributors with no reduction on cost/unit]
- Grand Total: 680 k€ + VAT = **829.6 k€** (not including VTRX+ costs, provided by EIC project)
  Part of VAT could be exempted (final destination not in Italy)
- To be defined which production tests to be outsourced to ext. company

VTRX+ light leakage (from CERN ESE-VL+ group) (I)

VTRx+ prototype cover

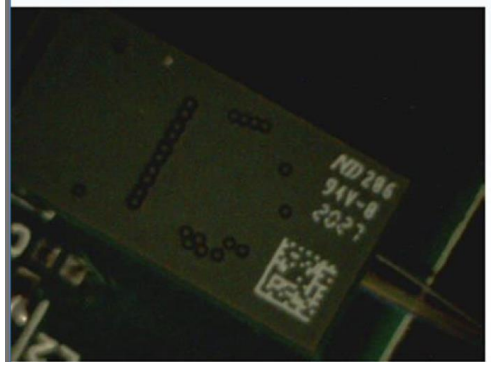
- 3D printed cover
- Mechanically good fit over VTRx+ module
- Material itself transparent to (infrared)light
- Painted with matte black paint at the polymer lab
- Greatly improved light shielding





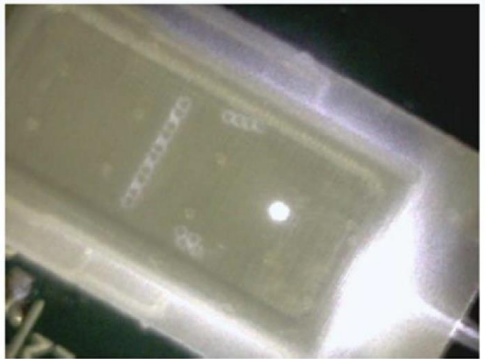
Photos with infrared sensitive camera:

VTRx OFF



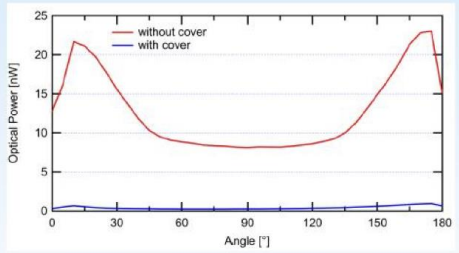
VTRx ON

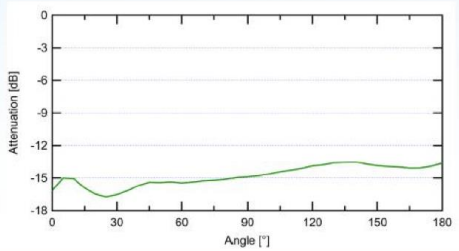
Cover without paint

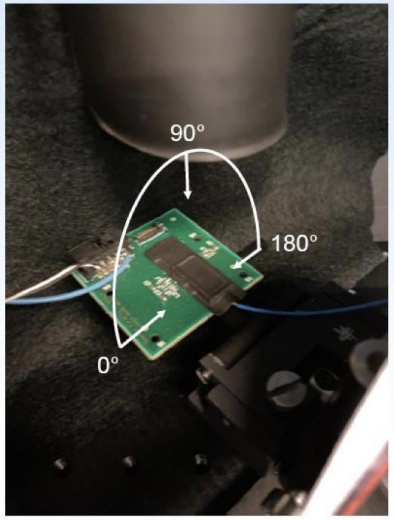


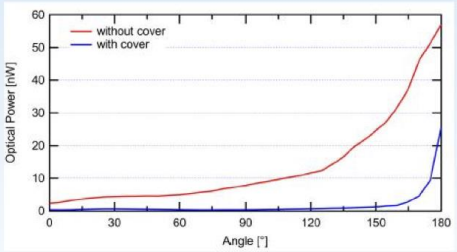
Painted cover

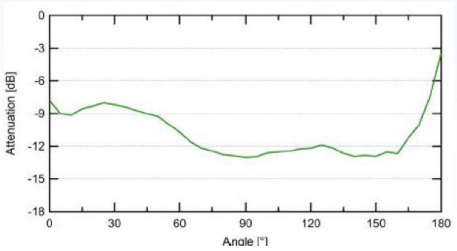
VTRX+ light leakage (from CERN ESE-VL+ group) (II)

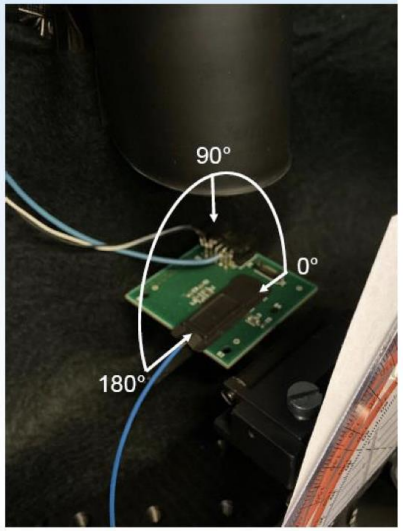












Conclusion of CERN ESE Versatile Link+ :

- Based on these first results the prototype cover significantly reduces VTRx+ stray light
- The directions to which the module mostly leaks light, except pigtail direction, are attenuated by 9-15 dB
- The worst stray light shielding is to the direction of the pigtail
  - Still halves the stray light
  - Never facing to sensors
  - Could be maybe further improved with small design changes if needed
    - Longer lip, cover around the pigtail more tightly…