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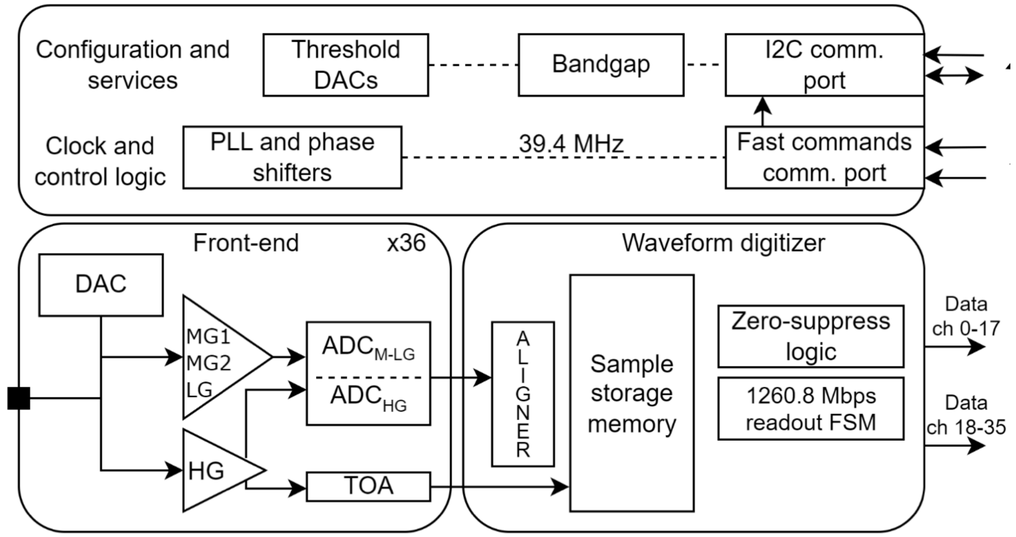
CALOROC 36 or 72 (32 or 64) channel configuration

Norbert Novitzky
(ORNL)

ORNL is managed by UT-Battelle LLC for the US Department of Energy

CALOROC1 A/B readout



1.26 Gbps

1.26 Gbps

The current ASIC design:

- 2x1.26 Gbps speed
- Covers 2x 18 channels (total 36 channels)
- Some I2C and fast command lines

Some readout capability calculation:

Data format:

- 1 sample
  - 32b header, 32b hitmap, (1-18)x32b channels, 32b trailer, 32b idle = 160b-704b

4 sample then 640b-2816b

Readout speed: 704b/1260Mbps = 0.558 µs (0.127 µs for 1 channel)

- Physics event with 4 samples - 2.232 µs —> 450 kHz readout
- Noise event (1 random channel) with 4 samples - 118 kHz
  - If all 18 channels are noisy at same time 450 kHz/18 = 25 kHz

This design also make it compatible with the LpGBT chip from CERN

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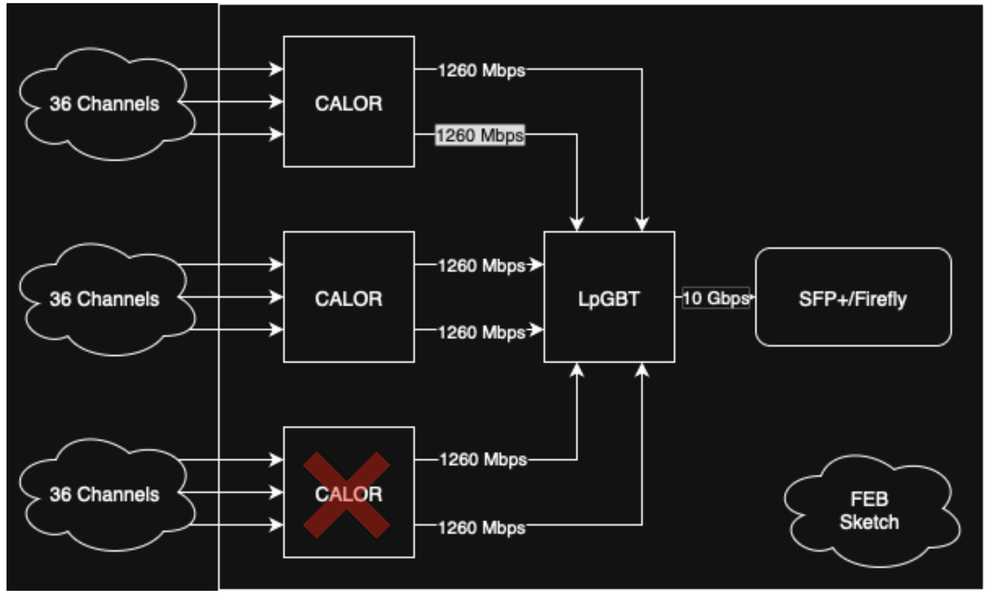
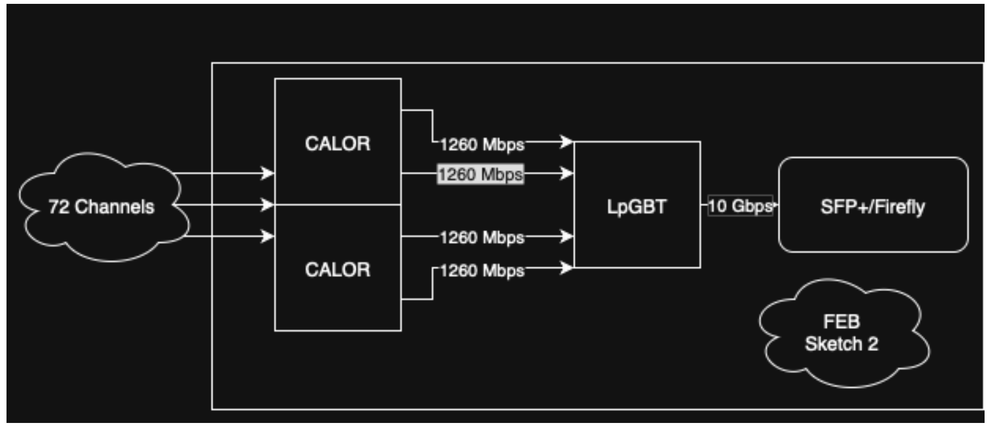
CALOROC towards final design



Option 1 (36 channel):

- 3:1 Caloroc:LpGBT
- Covers up to 108 channels:
  - Flexible design for 1, 2, 3 CALOROCs
- Exact same amount of services needed



Option 2 (72/64 channel):

- 1:1 Caloroc:LpGBT, 2x 1260Mbps lines are unused
- Covers 72 channels (or 64, if they would not fit in)
- Baseline with the services
- More compact (space-saving)

Some pros and cons

36 channel one	72 channel one
90%	81%
6700 pc	3700 pc
Additional space (but fits)	More compact
Less dense traces	More complex PCB
3:1 LpGBT ratio	1:1 LpGBT ratio
10 Gbps output from FEB	10 Gbps output from FEB
Services are the same	Services are the same
36, 72, 108 channel per FEB	72 (64) channel per FEB
0.7W, 1.4W, 2.1W	1.4W
Total cost: 250k$ mask + 4k$/wafer (6 wafer) + 36k$ (packages) [108%]	Total cost: 250k$ mask + 4k$/wafer (5 wafer) + 18k$ (packages) [100%]
Less iteration	Need additional engineering run (+250k$)
N/A	Probably need to shrink to 64 channels

Clearly, the 36 channel route is superior:

- ***We will have it sooner and for less money***
- ***More flexibility, versatility without increasing services***

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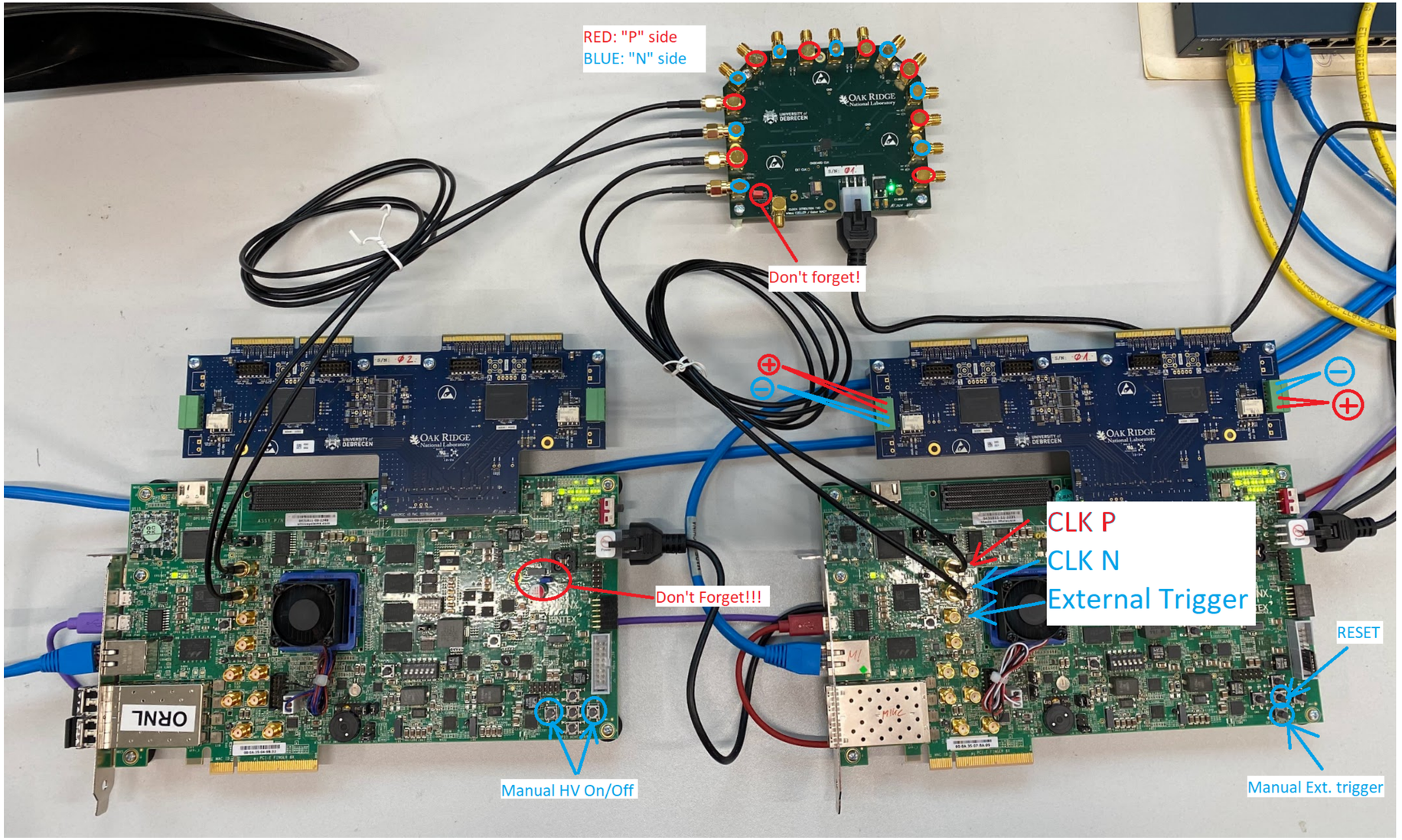
Present



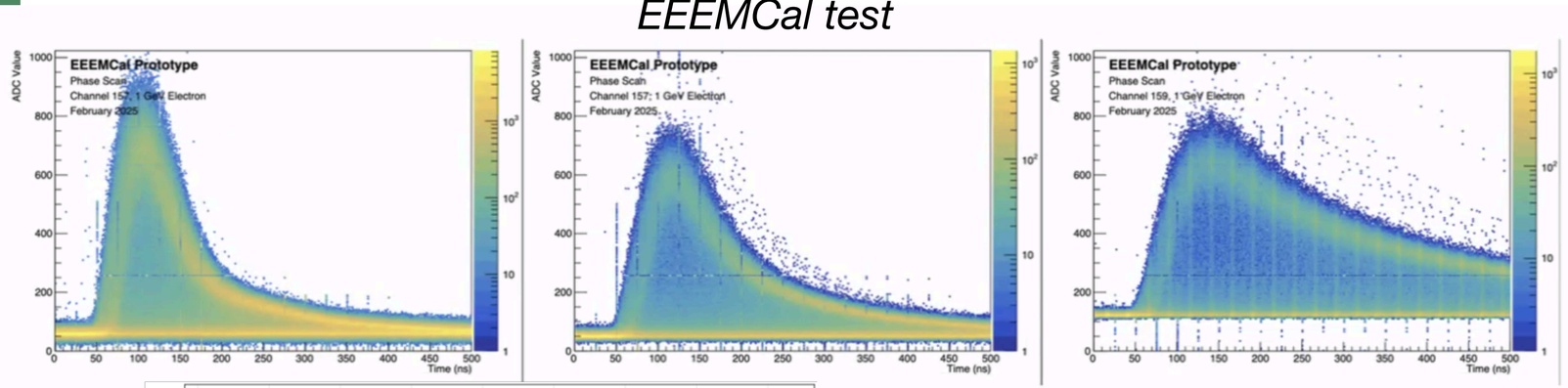
Veni, vidi, vici:

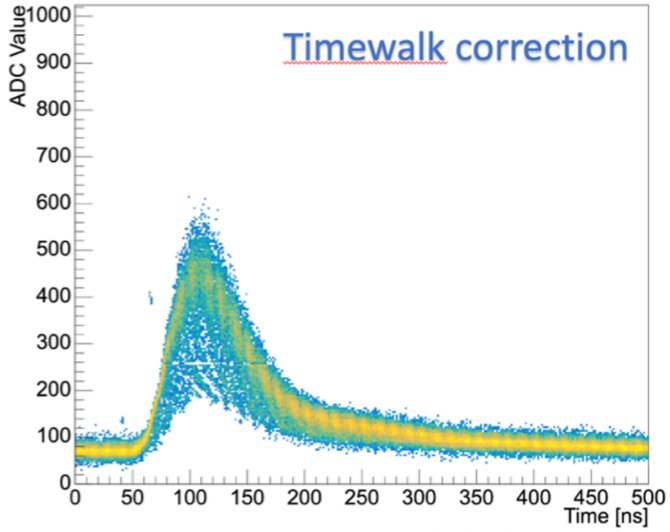
- Available already for years
- Many groups are using it, testing their detectors
- H2GCROC only
- Readout will be upgraded to 10Gbps

Was a good testing platform, let's move on

Present

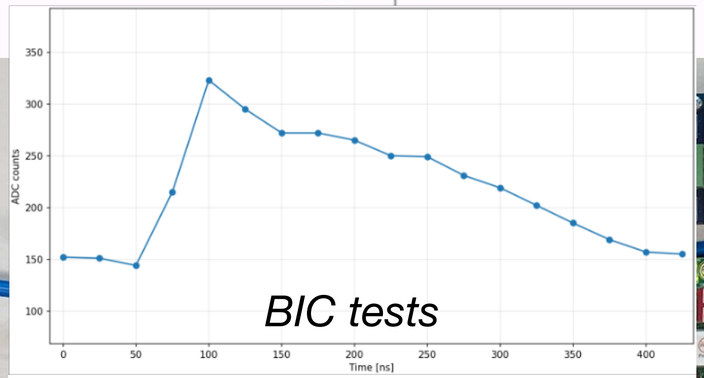
EEEMCal test



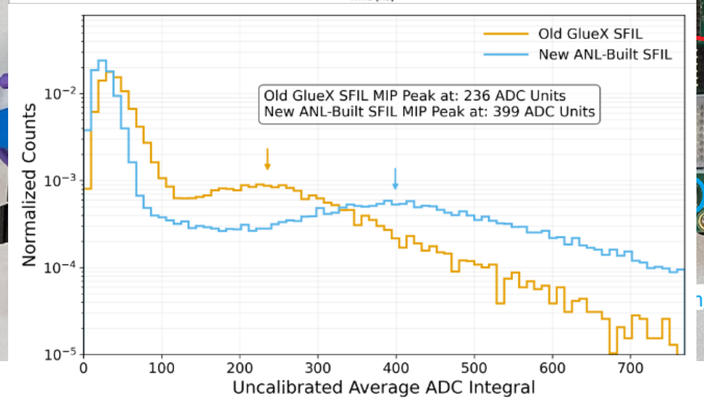


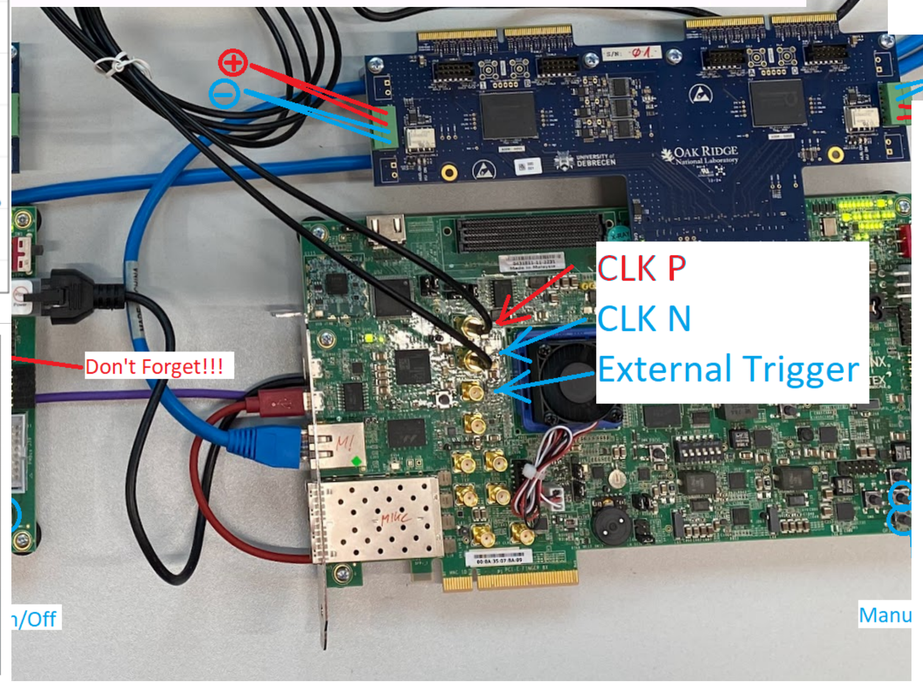
ars
it,

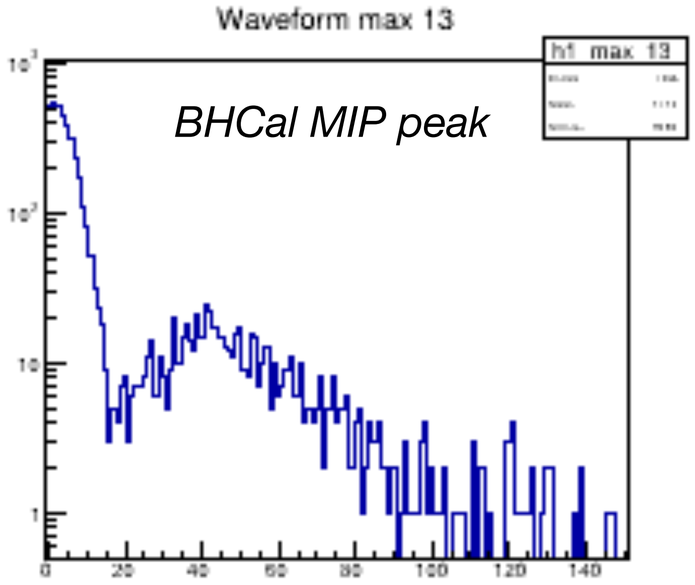
- Readout will be upgraded to



BIC tests







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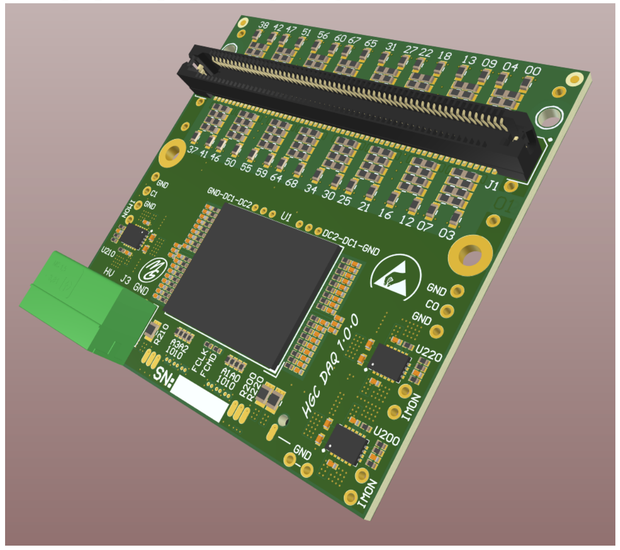
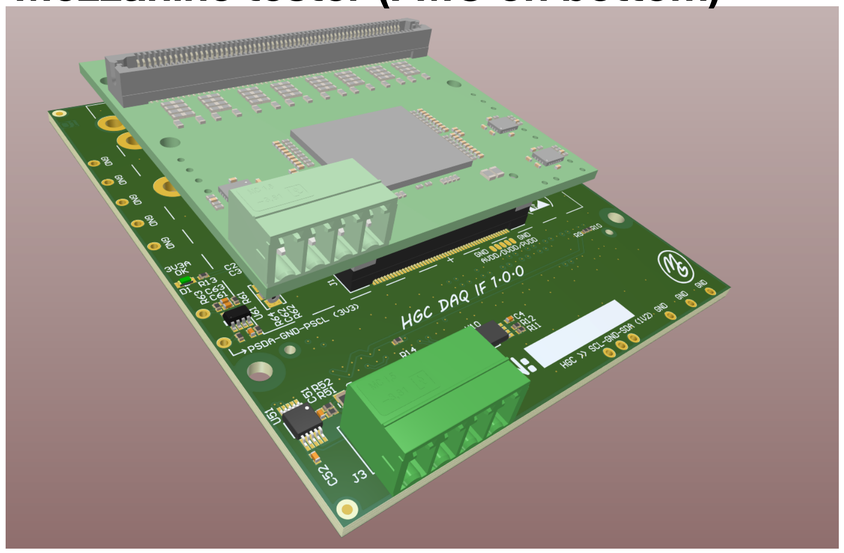
Way forward

H2GCROC mezzanine



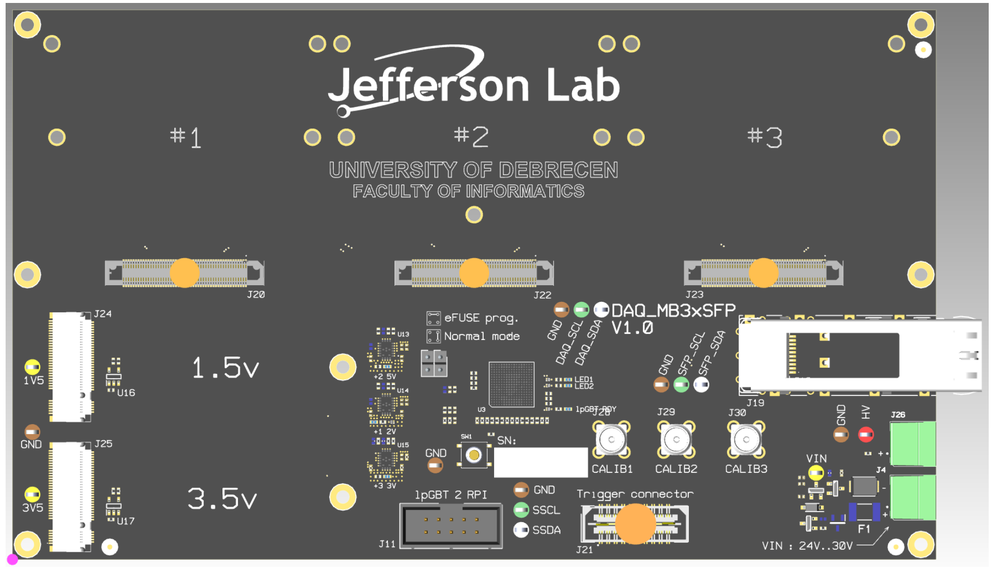
Mezzanine tester (FMC on bottom)



The mezzanine:

- 10 H2GCROC mezzanines will be produced
- One mezzanine == 64 channels
- Once CALOROC is available:
  - Make mezzanines with CALOROC
- Mezzanine Tester:
  - Connect to an FPGA FMC connector (e.g. KCU105, RDO, etc)
  - Individually testable setup
  - Can be used for small setup as is

Baseboard for 3 mezzanines



Step forward:

- Can take 3 mezzanines:
  - Does not matter H2GCROC or CALOROC mezzanine
  - Both has 2x1.28 Gbps data lines
- First test article for all FEB
  - 1 LpGBT can take 3 ROCs
  - 1 SPF+ —> 10 Gbps output
  - 2 DC/DC bPOL48 converters
  - All radiation tolerant (SPF+?)

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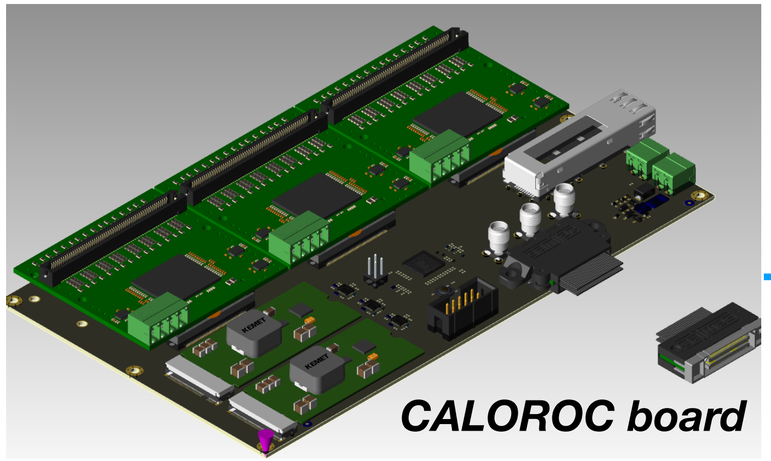
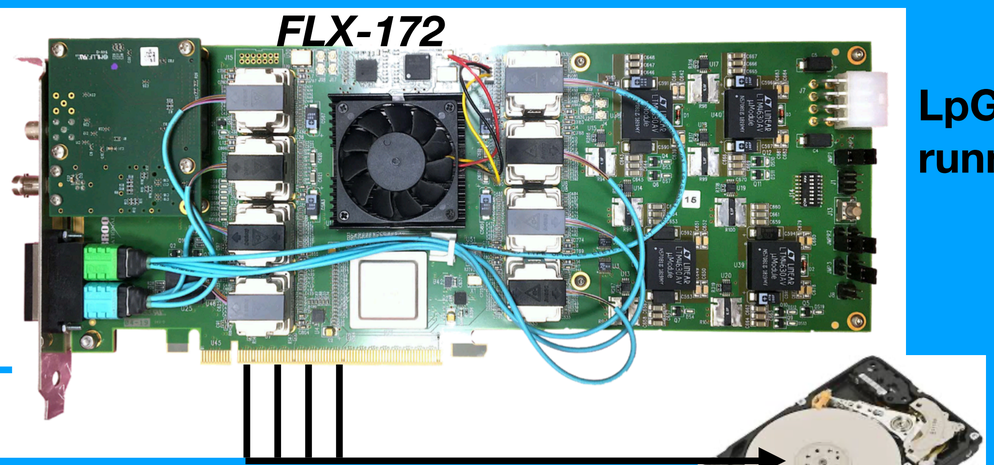
Full DAQ testing

Step 1 (end of September):



10Gbps fiber

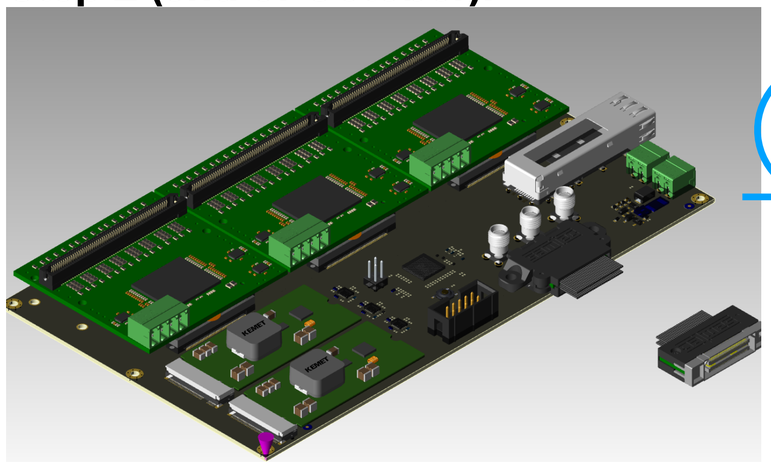
PC

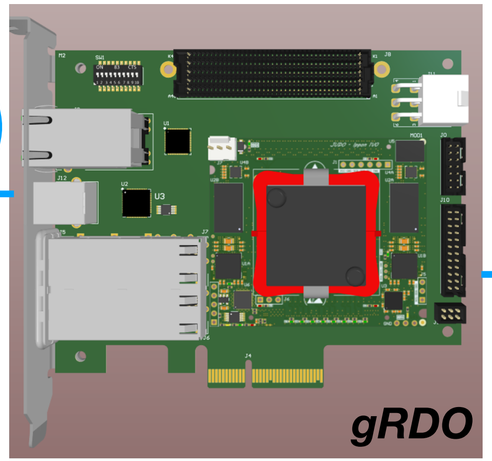


LpGBT fw running

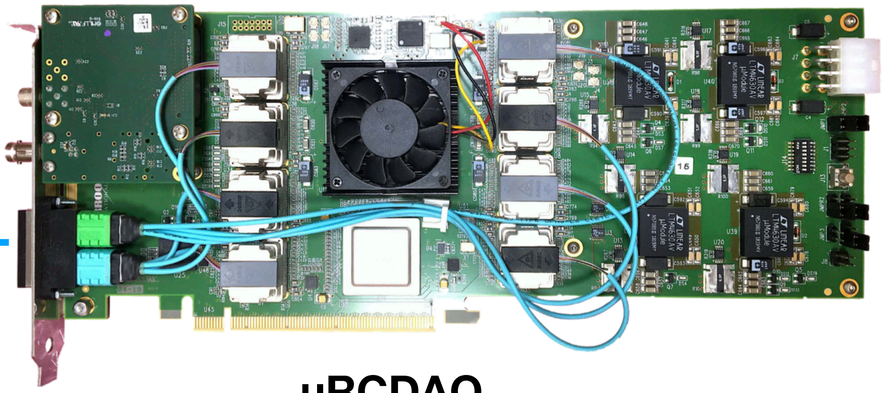
RCDAQ

Step 2 (end of October):





LpGBT fw + aggregator

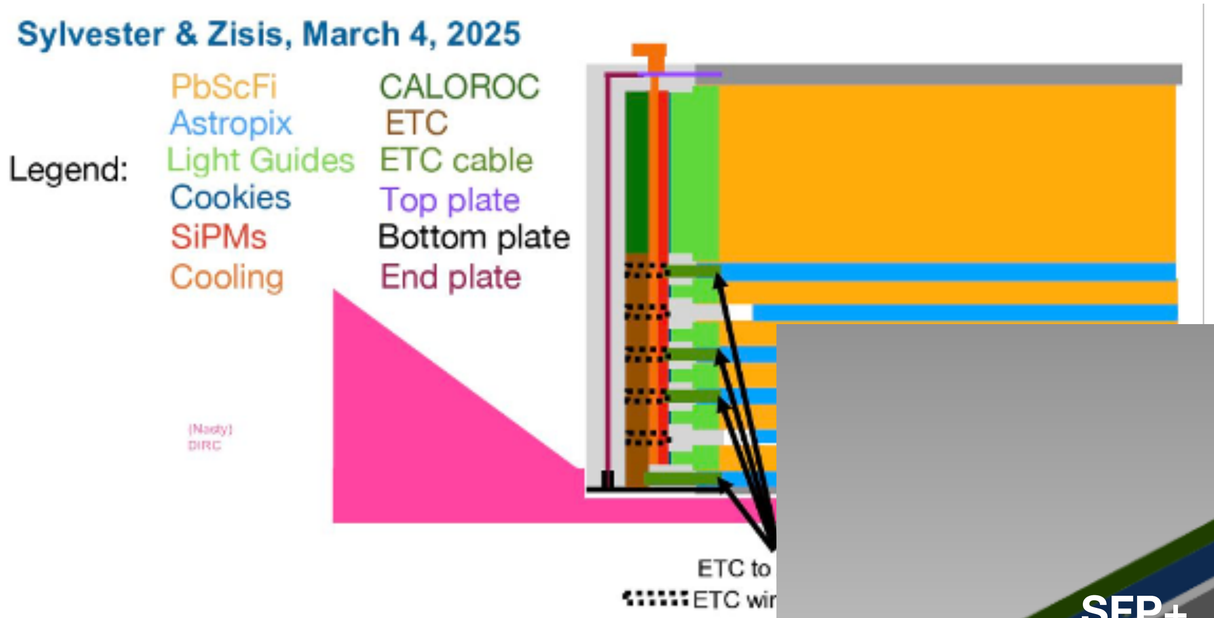


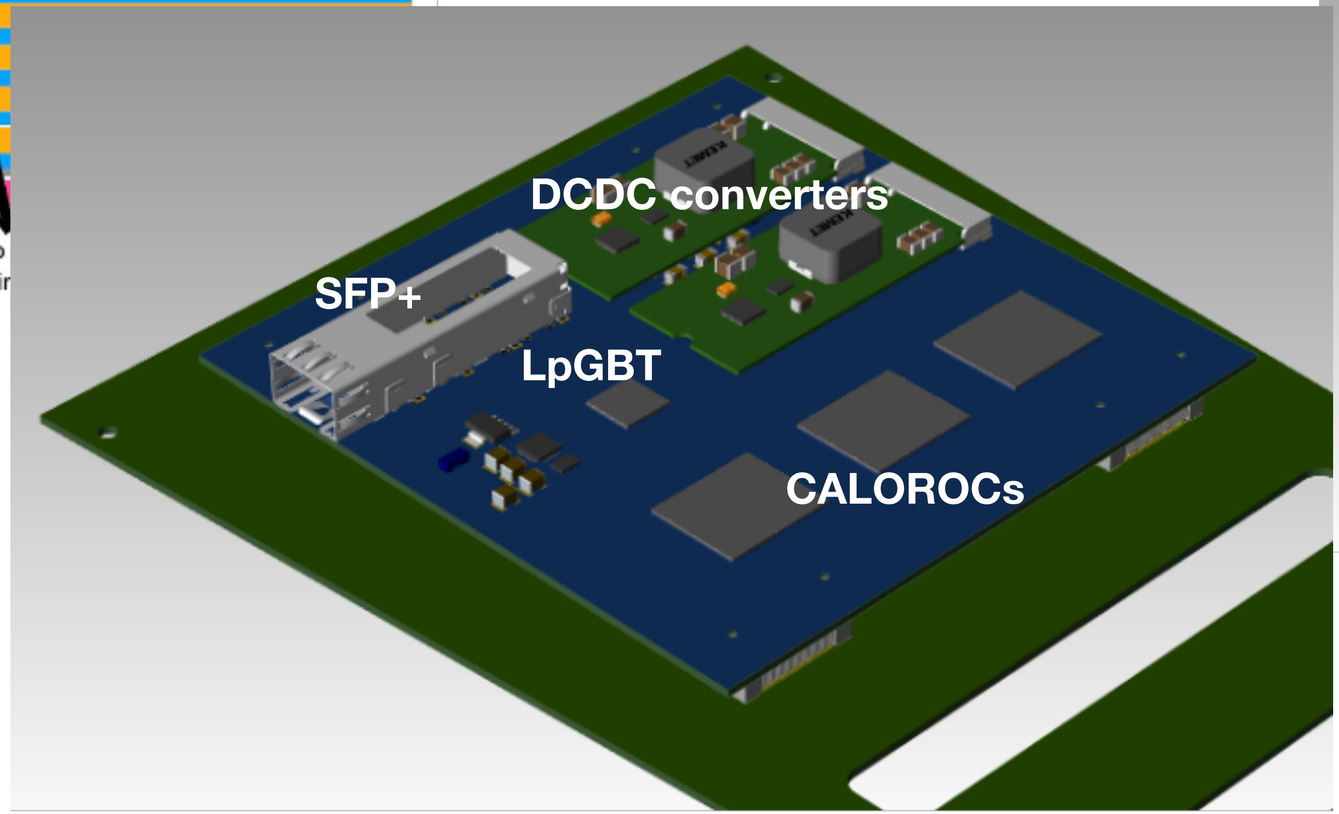
µRCDAQ

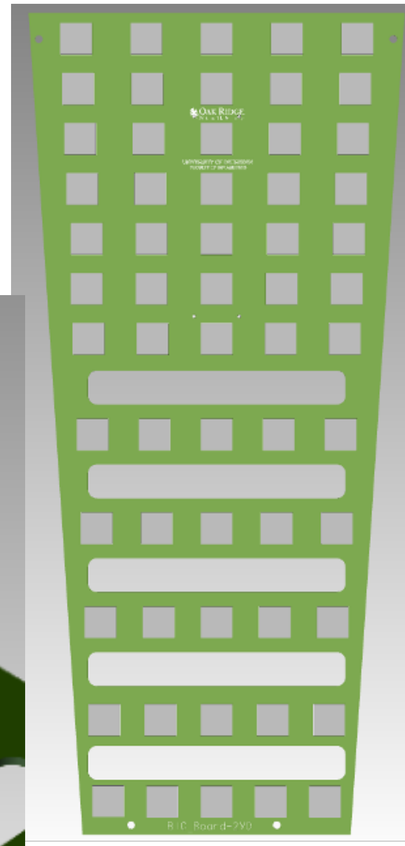
The ‘NO summary’ slide

- **CALOROC channel count 36 vs 72:**
  - Less risk by implementing less channels - better yield by individual chips
  - More space, but this does not look to be a problem in calorimeters
  - Cost increase is minimal, more versatility with the lpGBT
- **Rapid progression in integration to µDAQ system:**
  - In ORNL we have 1xFLX-172, 1x Versal evaluation board
  - End of September:
    - 10x H2GCROC mezzanines
    - 5x FPGA mezzanine tester
    - 3x Baseboard
  - End of October:
    - 16 gRDO’s
  - End of year:
    - Everything should start to work, reading out H2GCROCs
  - January:
    - 150 CALOROC1A production (5400 channels)
    - 150 CALOROC1B production (5400 channels)
  - February:
    - CALOROC mezzanines
    - Extra baseboard
  - April:
    - sPHENIX would ‘release’ 30-40 FLX-172?

Backup







The FEB for the BIC is the most space constraint, yet it can accommodate 3 chips with the lpGBT + services