ePIC MPGD readout

Power dissipation oriented Intro

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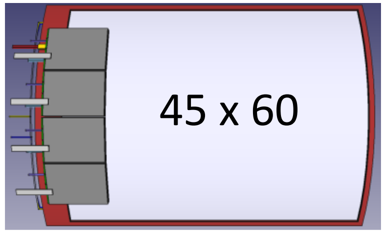
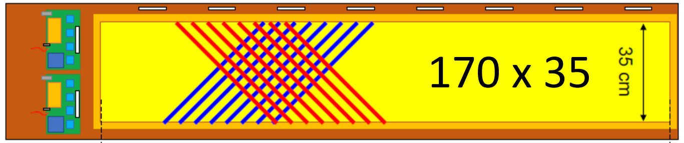
Reminder on MPGD sub-systems and channel counts

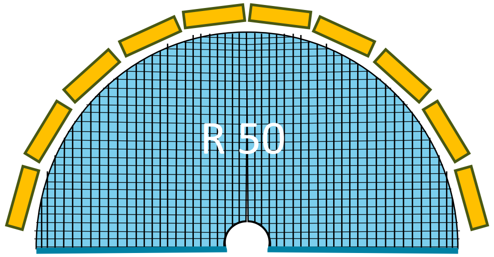
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~50k channels
  - → 48 tiles of 1024 channels each



- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  - → 24 modules of 4 096 U-V strips each

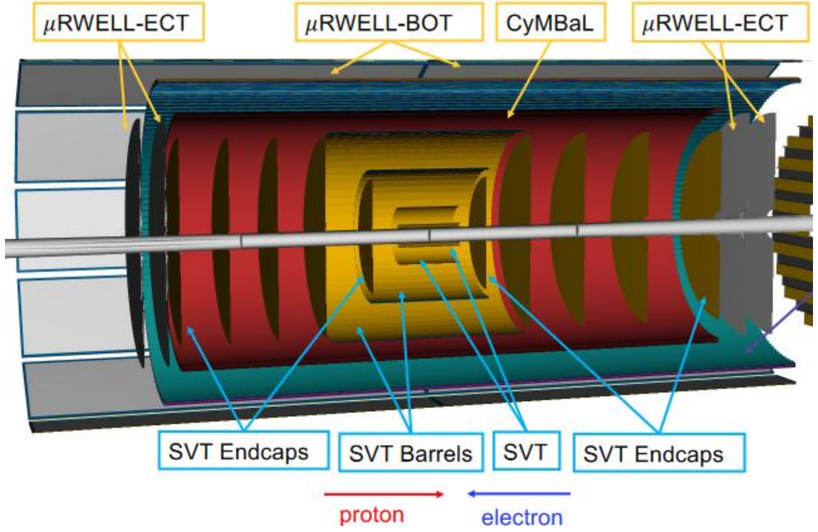


- µRWell End Cap Tracker : µRWell-ECT : ~30k channels
  - → 8 half-disks of 4 000 X-Y strips each



- ~180k-channel heterogeneous system
  - → Micromegas, µRWell, barrel, endcap, curved, planar, circular

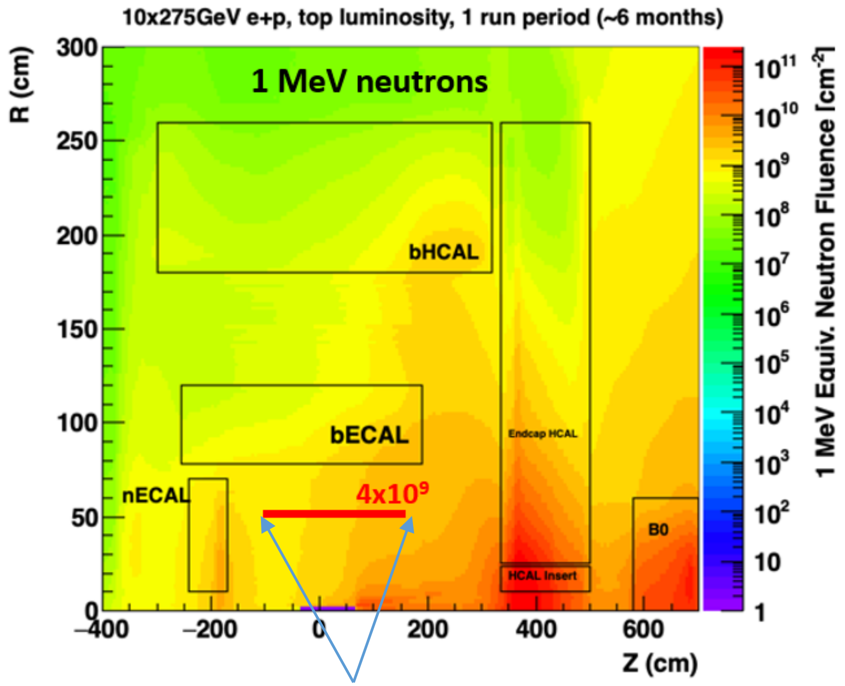
- Common approach to acquire data from different types of ePIC MPGDs
  - → Use same frontend ASIC
    - Salsa – under development
  - → Share frontend design between groups
    - Adapt form factor if needed



Inner detector fronted environment

- Stringent space
- Restricted material budget including for cooling
- Magnetic field
- Radiation

- Example of CyMBaL tracker environment
  - → TID after 10 years : 10 krad
  - → Neutron fluence after 10 years: 10^{11} n_{eq} / cm^2
  - → 20 MeV proton flux: 100 particle / cm^2 / s
  - → Magnetic field: 1.9 T

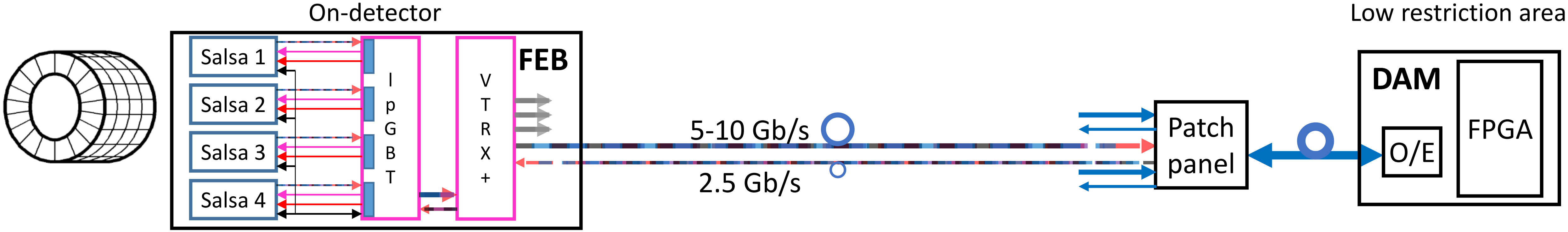


CyMBaL is here

- Similar radiation and magnetic field environment for other MPGD detector frontends

- Note : radiation environment changes "every week"
  - → Mainly due to ups and downs in estimations of synchrotron radiation

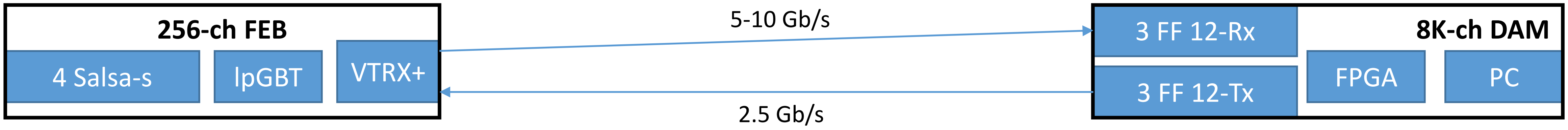
MPGD readout architecture based on lpGBT / VTRX+



- 256-channel FEB with 4 Salsa-s per board

- Direct FEB-DAM connection avoiding intermediate RDO stage
  - → Downstream
    - ■ Clock | Synchronous run-control commands | Async slow control and monitoring requests
  - → Upstream
    - ■ | Physics and calibration data | Slow control and monitoring responses

176K-ch MPGD readout component count



- Operational quantities

	CyMBaL	µRWell-BOT	µRWell-ECT	Total
Channels	48K	96K	32K	**176K**
Salsa	768	1 536	512	**2 816**
FEB	192	384	128	**704**
DAM	6	12	4	**22**

- Production quantities
  - Including prototyping, test-bench and quality assurance needs

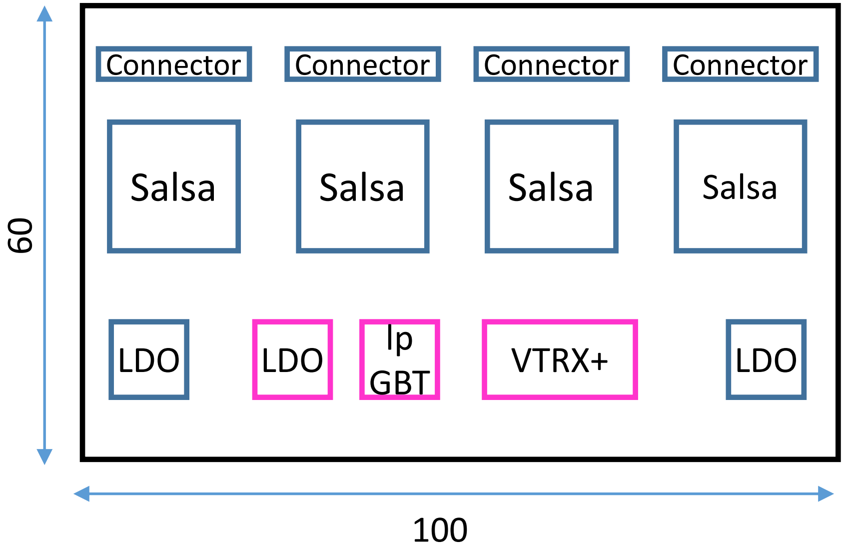
→ 4 000 Salsa-s

→ 770 FEBs
  - 770 VTRX+
  - 770 lpGBT

→ 25 DAMs
  - 100 12-Rx and 12-Tx FireFly modules

256-channel FEB power consumption

Component illustration for CyMBaL FEB



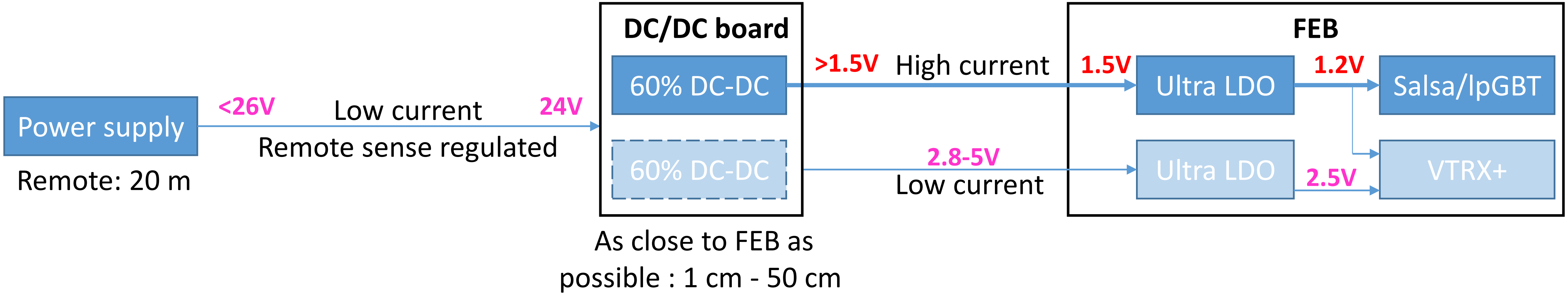
- Raw power budget with minimal margin : ~6.8 W
  - → 27 mW / ch
- Assume 8.5 W for safety : 25% extra
  - → 33 mW / ch
  - → 1.5 V – 5.6 A
  - → 2.8 V – 90 mA
- Cooling to be studied

FEB components and their power consumption

Component	Vin V	Current mA	Power mW	Comment
Salsa 1	1.2	1 000	1 200	15 mW/ch
Salsa 2				
Salsa 3				
Salsa 4				
lpGBT	1.2	420	500	Overestimated
VTRX+	1.2	20	25	
	2.5	70	175	
LDO Salsa 1-2	1.5	2 000	600	LDO / Salsa to avoid hotspots ?
LDO Salsa 3-4				
LDO lpGBT/VTRX+	1.5	440	130	
LDO VTRX+	2.8	70	20	

FEB powering in ~1.8 T magnetic field

- DC/DC-based LV distribution: to be magnetic field tolerant
  - → Remote power supply distributes 12-24V with a low voltage drop over ~20 m cables
  - → Low cross-section power cables

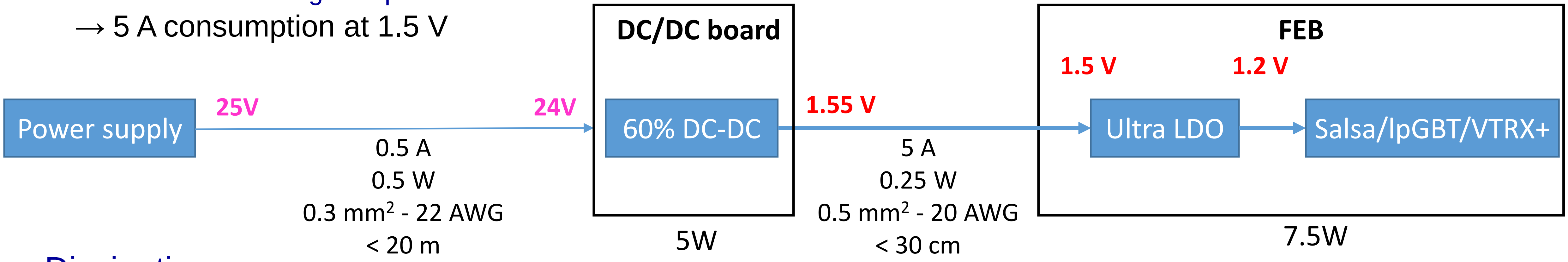


- DC/DC regulator board
  - → Might be bulky and a source of EMI
    - Space + extra material for shielding
  - → Delivers high current for 1.2V
    - Should be close to FEBs
      - Avoid significant power drop and power dissipation in cables
      - Avoid pickup noise and ground-loops

- Studies within the ePIC collaboration to have common approach to power the frontends
  - → Adapt proposed solution to MPGDs

Expected power dissipation

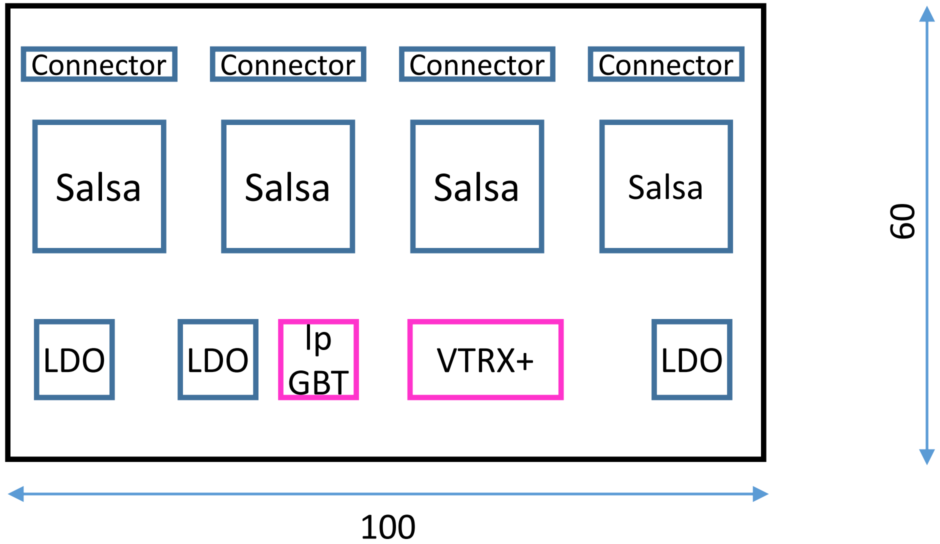
- Assume
  - → 20 m cable between remote power supply and DC-DC convertor
    - Less than 1 V voltage drop
  - → 60% DC-DC efficiency
  - → DC-DC not far from FEB
    - In 30cm vicinity
    - 0.05V voltage drop
  - → 5 A consumption at 1.5 V



- Dissipation
  - → 0.5 W over PS – DC-DC cables : 22 AWG
  - → 5 W on DC-DC board
    - Requires cooling
  - → 0.25 W over DC-DC – FEB interconnect : 20 AWG
  - → 7.5 W on FEB
    - Requires cooling

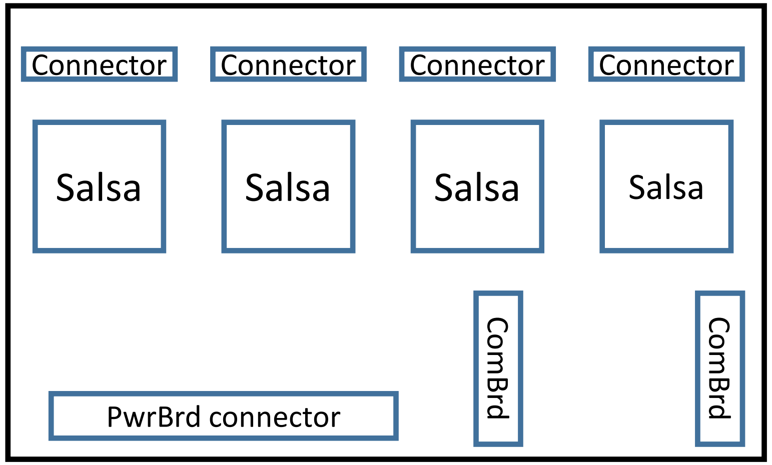
Illustration of CyMBaL lpGBT-based FEB organization options

- Single board

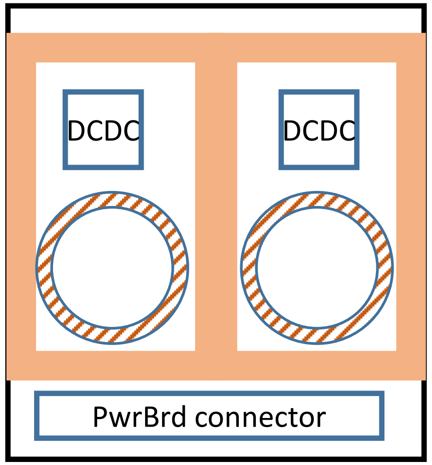


→ Complex high density high speed
→ MPGD-specific form factor

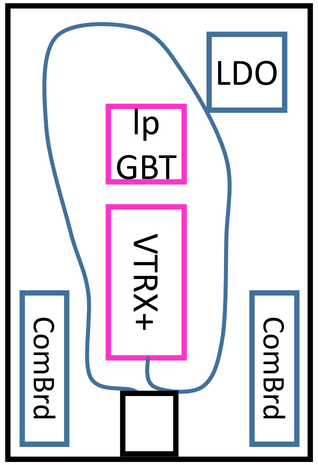
Mezzanine approach



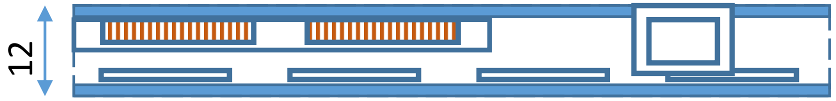
→ FEB mother-board
→ Low density low speed
→ MPGD-specific form factor



→ DC/DC mezzanine
→ 2 T tolerant low EMI
→ Common to all MPGDs ?



→ Communication mezzanine
→ high density high speed
→ Common to all MPGDs ?



Summary

- Design is in early stage
- Specific form-factors for frontend electronics boards depending on MPGD type
  → FEB, optical module, DC-DC converter
- Not enough knowledge on component placement and space constraints

- Cooling will be required for all frontend components

- Targeted operation temperature should be within 25-35°C.
  → With current knowledge, temperature stability less than 3°C peak to peak can be acceptable