ePIC MPGD readout

Rectification after eDAQ PDR on September 3-4

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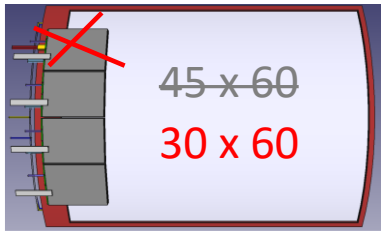
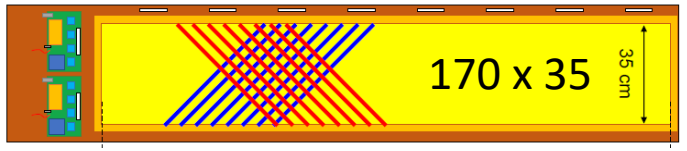
Quick update on MPGD channel counts

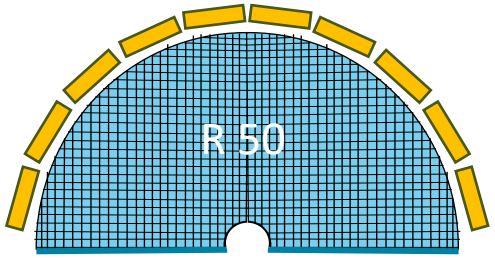
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~50k channels
  - → 48 tiles of 1024 channels each



- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  - → 24 modules of 4 096 U-V strips each

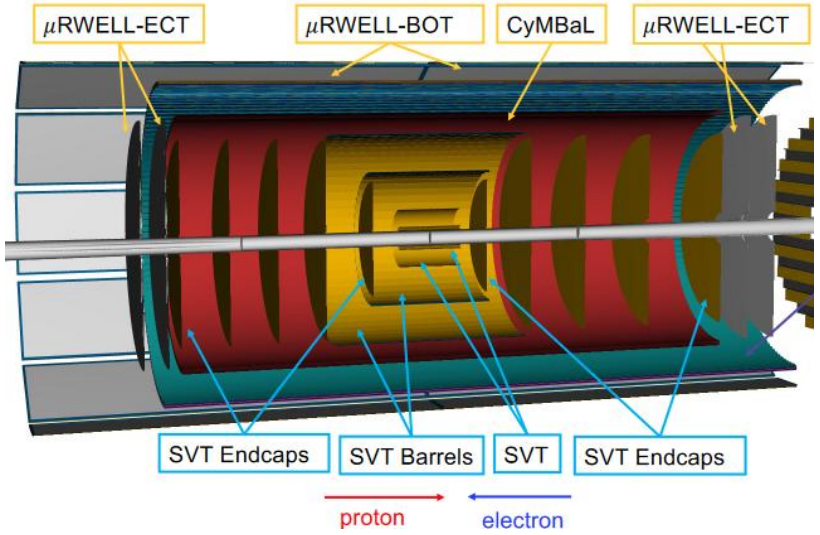


- µRWell End Cap Tracker : µRWell-ECT : ~30k channels
  - → 8 half-disks of 4 000 X-Y strips each



- ~180k-channel heterogeneous system
  - → Micromegas, µRWell, barrel, endcap, curved, planar, circular

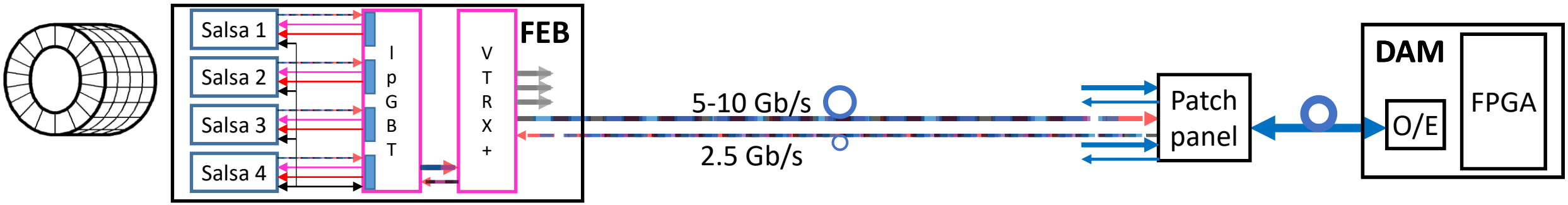
- Common approach to acquire data from different types of ePIC MPGDs
  - → Use same frontend ASIC
    - Salsa – under development
  - → Share frontend design between groups
    - Adapt form factor if needed



Baseline architecture for MPGD readout

On-detector

Low restriction area

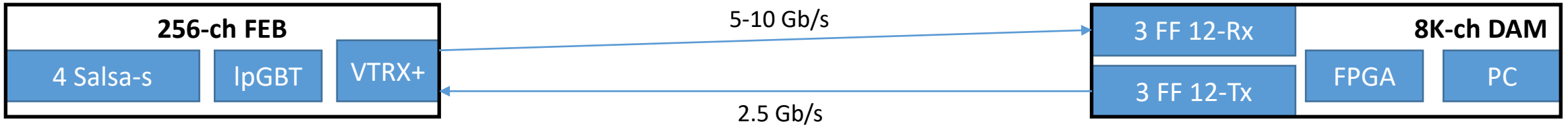


- 256-channel FEB with 4 Salsa-s per board

- Direct FEB-DAM connection avoiding intermediate RDO stage
  - → Downstream
    - Clock — Synchronous run-control commands — Async slow control and monitoring requests
  - → Upstream
    - — Physics and calibration data — Slow control and monitoring responses

  → Presented at collaboration meeting in Frascati, January 2025
  https://agenda.infn.it/event/43344/contributions/253075/attachments/130667/194487/250124_IM_MpgdRo_Update.pdf
  → For detailed discussion on lpGBT use in MPGD readout see
  https://indico.bnl.gov/event/25106/contributions/97861/attachments/57983/99568/241017_IM_lpGbt2Salsa.pdf

176K-ch MPGD readout component count



- Operational quantities

	CyMBaL	µRWell-BOT	µRWell-ECT	Total
Channels	48K	96K	32K	**176K**
Salsa	768	1 536	512	**2 816**
FEB	192	384	128	**704**
DAM	6	12	4	↑ **22**

- Production quantities
  - Including prototyping, test-bench and quality assurance needs

→ 4 000 Salsa-s

→ 770 FEBs
  - 770 VTRX+
  - 770 lpGBT

} A common pool of spare components expected

→ 25 DAMs
  - 75 12-Rx and 12-Tx FireFly modules

Summary

- Reminder : RDO subsystem is complex and has non negligible size
  - → O(100) RDO boards to be housed, powered, cooled, controlled and monitored
  - → Effort to develop, validate, produce, install and commission
    - Hardware, firmware, software
  - → A group to be identified responsible for RDO subsystem

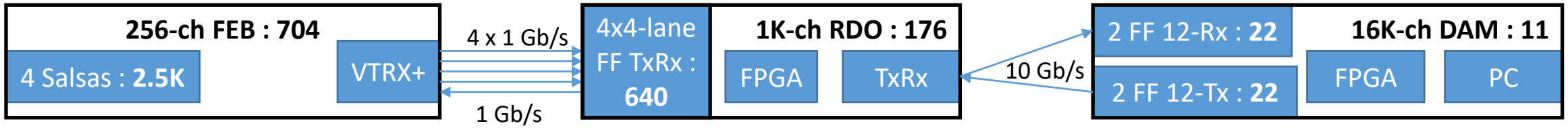
- Pros and cons of presented architecture
  - → Pros : Avoids RDO complexity and related effort
    - Inline with several other subsystems – developments can be shared
  - → Cons : increases number of DAMs
    - Basically doubles
      - 1.5 increase with higher channel count DAMs : Fully populated with FireFly components
    - GTU has to accommodate the extra DAMs

- Are there strong arguments for not to adopting this architecture for MPGDs ?

Backup

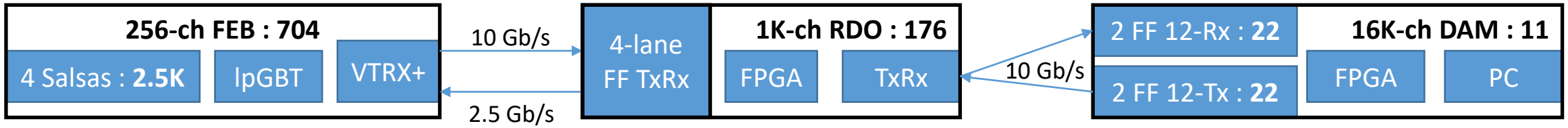
160K-ch MPGD readout configurations and component count

- FEB with direct Salsa-VTRX+ interface



Low density 1 Gb/s grade

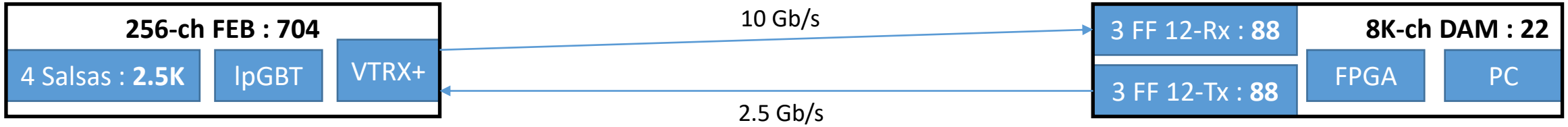
- FEB with lpGBT-VTRX+ interface



High density 10 Gb/s grade

4 times less 4-lane FF

- FEB with direct DAM interface



High density 10 Gb/s grade

No RDOs to design, produce, install, debug and maintain

3 times more 12-lane FF pairs
2 times more DAMs