LARZIC ASIC Documentation

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LARZIC ASIC Documentation

Top Drift Electronics (TDE) Consortium V1.2 30 March 2023

1. LARZIC Design

1.1. Introduction

The LARZIC ASIC is the outcome of an R&D process carried on at IP2I Lyon [1, 2, 3, 4] which went through progressively sophisticated versions of a cryogenic ASIC preamplifier based on the CMOS 0.35 μm technology, for the readout of Liquid Argon (LAr) Time Projection Chambers (TPC). Nine versions of the ASIC, incorporating in each next generation more elements and readout channels, were designed and tested in between 2007 and 2016; some first versions of the chip are shown in Fig 1.

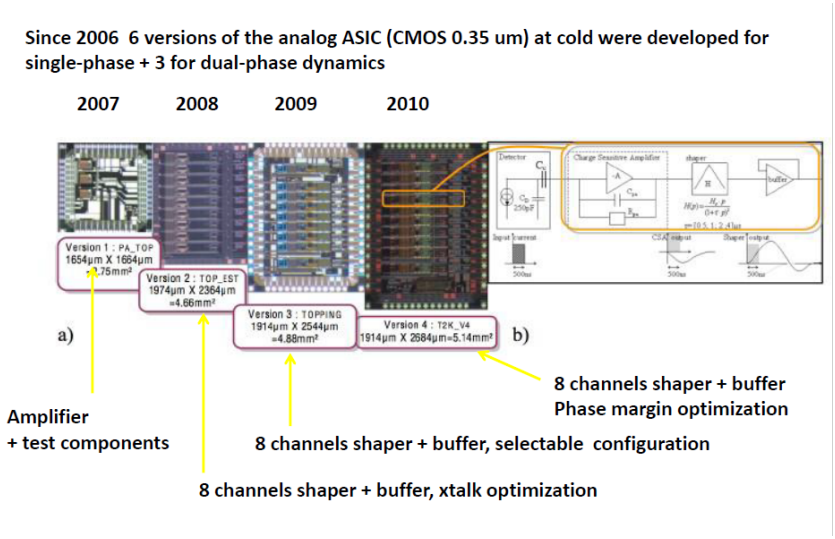

Figure 1: Development process for LARZIC 2006-2016

The current version of LARZIC ($LARZIC\_2015$, see Figure 2), exploited by the dual-phase electronics and by the Vertical Drift Top-Drift Electronics (TDE), was produced in 2016 for 700 chips in order to equip the $3 \times 1 \times 1m^3$ dual-phase TPC demonstrator and the NP02 ProtoDUNE dual-phase detector, where it successfully operated in 2019-2020 and it was exploited in dual-phase demonstration of the readout of tracks over 6m drift length.

Additional 300 chips were produced in 2020 with completely equivalent characteristics of the 2016 production. These chips are also used to equip the cryogenic Front End Boards (FEB) deployed to readout the prototypes top-drift Charge Readout Planes (CRP) for the second DUNE Far Detector Module based on the Vertical Drift Design (DUNE FD2-VD). The top-drift

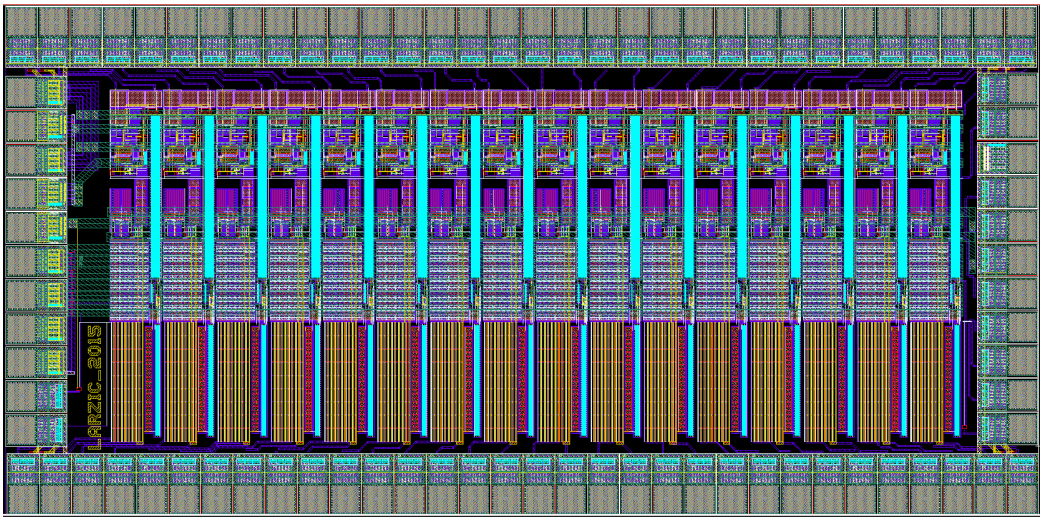

Figure 2: *LARZIC*_2015 layout

CRP prototypes and the associated TDE electronics, including the FEBs with the LARZIC chips, were extensively tested in 2021 and 2022 in the cold-box TCP cryostat, setup at in the EHN1 hall by the CERN Neutrino Platform.

1.2. Design development, requirements and specifications

The *LARZIC*_2015 ASIC satisfies the DUNE requirements, its main specifications are listed in Table 1.

The LARZIC was originally developed as an integrated circuit for the readout of large LAr TPC neutrino detectors. These detectors employ LAr simultaneously as massive neutrino target and detection medium of the secondary charged particles. The detection of secondary particles produced in neutrino interactions is achieved by collecting, on a system of segmented anodes at the top of the detector, the electrons from their ionization losses. In the Vertical Drift design three planar coordinates are measured by the perforated anodes segmentation (the first views on perforated anodes act as induction views, the third implemented view collects the electrons), the fourth, orthogonal, coordinate is obtained by measuring the drift time. In order to limit input cable capacitance and therefore the noise, the front-end electronics is designed to be installed as close as possible to the anodes in the ullage volume of the cryostat.

Parameter	Value
Technology	CMOS 0.35 um
Number of channels per ASIC	16
Integrated components per channel	CSA + Differential Buffer
Peaking time	1 μs
Operation temperature	Typically around 110 K at the bottom of the SFT chimneys, the LARZIC/FEB can operate as well at LN2 temperature
Power consumption	11 mW/channel
ENC	$\approx$ 600 electrons at cold for 250pF detector capacitance
Conversion factor	11 mV/fC (including all the entire TDE analog chain ASIC + ADC buffer)
Calibration	Integrated charge injection system with embedded capacitors and the possibility of activating single channels or groups of channels
Integrated charge injection capacitors	1 pF
Crosstalk	$< 1\%$
Unipolar dynamics (ASIC)	Linear up to 400 fC, max signals up to 1200fC with dual-slope regime (used in dual-phase)
Bipolar dynamics (ASIC)	Linear up to +-200 fC
Bipolar dynamics (ASIC coupled to ADC buffer)	Linear up to +-80 fC

Table 1: $LARZIC\_2015$ main characteristics and specifications

The LARZIC ASICs will be installed for the readout of the top-drift volume of the second DUNE Far Detector module above the liquid argon level and will be operating at the temperatures of the argon vapours contained in the upper part of the cryostat. Four LARZIC ASIC chips are integrated on each cryogenic Front End Board (FEB). The FEBs are mounted on sliding blades and plugged on cold flanges at the bottom of the signal feedthrough (SFT) chimneys. This configuration allows keeping the FEBs very close to the anodes, operating around 110K temperature and accessible at any time from outside by opening the chimneys and extracting the blades. This access

operation to the FEBs can be performed in "hot-plugging" without risks of contamination of the LAr volume neither having to stop the operation of the other top-drift front-end electronics components.

Depending on the height above the liquid level, the cryostat geometry and insulation and other environmental and installation aspects the location of the electronic boards in the gas phase may correspond to temperatures ranging between 100K and 150K. In case of the DUNE design adopted in the $3 \times 1 \times 1$, in NP02, in FD2-VD and deployed in all tests operated so far, the operation of the FEBs happens at a temperature of 110k achievable at the bottom of the SFT chimneys integrated in the roof of the DUNE cryostats. The ASICs and the FEBs should dissipate as little heat as possible,in order to represent a minor contribution to the heath flow going through the SFTs, preventing so additional warming of the detector and of the gas inside the chimneys.

For the ASIC design it was selected a low-cost standard $0.35\mu m$ CMOS technology (C35B4C3) from AMS (Austria-MicroSystems) for its high performance in analog design. Such CMOS process also works well at cryogenic temperatures. The LARZIC can operate as well at the LAr or LN2 temperatures. An aspect of the CMOS technology, which was investigated in the R&D phase, with direct measurements and characterizations of single components in dedicated versions of the ASIC (transistors, resistors, capacitors) [1], is that the process is usually well characterized down to $-40°C$ while for these applications its functionality is extended to the LAr temperature.

The Charge Sensitive Amplifier (CSA) has to integrate a minimal amount of charge equivalent to about 30k electrons for a charged particle at the ionization minimum. This charge is typically collected over 500 ns and with a detector capacitance of the order of 200 pF. The input referred noise has to typically be as of the order of 1000 electrons or less.

A differential buffer is exploited to drive the lines bringing the signals outside the cryostat. A readout digitization system, developed following the μTCA standard, is used in conjunction with the analog front-end based on the LARZIC ASIC, in order to acquire and process the signal and transmit the data to the DAQ.

1.3. ASIC design

The $LARZIC\_2015$ ASIC was designed by using Cadence virtuoso (version IC6.1.6.64b.500.14) and the Physical Design Kit by the AMS foundry (PDK version AMS-410, October 2012).

The $LARZIC\_2015$ ASIC includes 16 readout channels. Each channel is composed by a Charge Sensitive Amplifier (CSA) followed by a differential output buffer stage, acting as low pass filter.

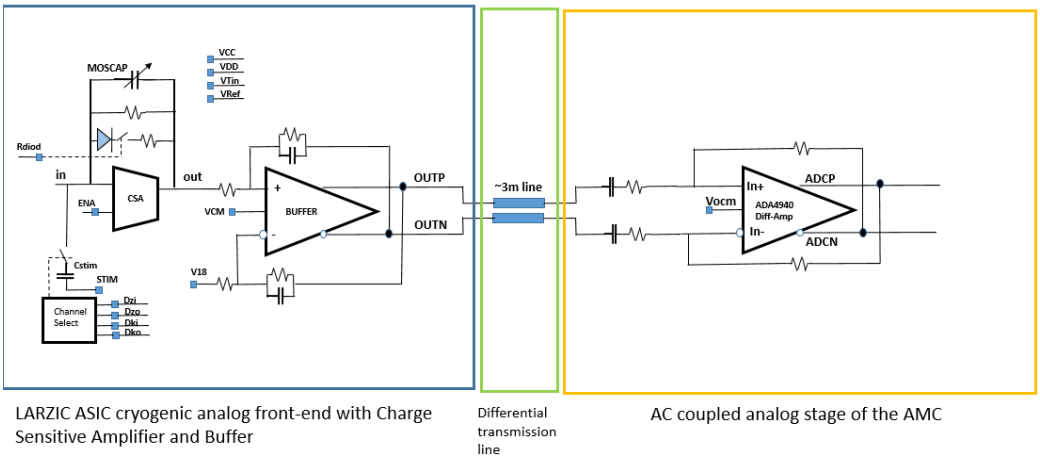

Figure 3: Synopsis of the TDE analog chain including the LARZIC ASIC and the analog stage (ADC buffer) present in the AMC digitization boards

A zoomed picture of the physical implementation of a single channel in the ASIC is shown in Figure 4. A single readout channel occupies a surface of about $1100\mu m \times 170\mu m$. The physical layout specifications of the chip are reported in table 2.

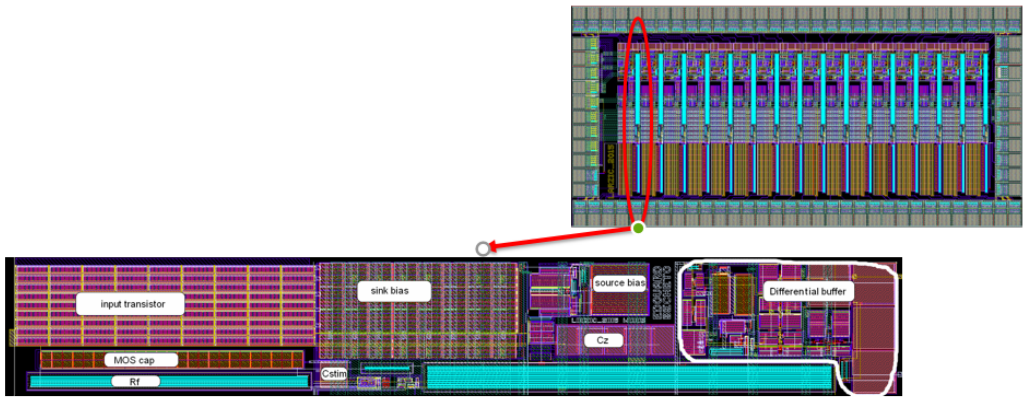

Figure 4: Zoomed picture of a single channel layout ($1100\mu m \times 170\mu m$) of $LARZIC\_2015$

Parameter	Value
Core size	x: 1160 μm, y: 2786 μm
Die size including pads	x: 1657 μm, y: 3368 μm
Pad area (passivation opening)	85 $\mu m \times 85 \mu m$
Pads spacing	x direction: 25 μm, y direction: 20 μm
Package type	PQFP 100
Jedec type	MS_022
Package body size	14mm × 20mm
Thickness	3.4mm

Table 2: $LARZIC\_2015$ physical layout characteristics

The differential buffer drives the signals up to the analog input stage of the AMC digitization cards. A scheme of the overall chain is shown in Figure 3.

The LARZIC output signals are transmitted on differential lines on flat cables with 120 Ohm impedance, up to the AMC analog input stage. The buffer integrated in the ASIC produces positive and negative differential signals (Figure 5) separated by an adjustable positive offset (V18) defining the common mode DC voltage. These signals are then treated by the differential amplifiers in the AMC analog input stage which are AC coupled at the end of the transmission lines and have a gain of 4. This gain is introduced in order to fully match the dynamic range of the ADCs and it adds on top of the gain of the ASIC amplifier.

The resistor (44 kOhm) in parallel with the capacitor (5 pF), present on each feedback branch of the differential output buffer, introduce a high frequency cutoff at 724 kHz (see Figure 6).

The peaking time of the LARZIC is $1 \mu s$.

1.3.1. CSA

The CSA consists of a folded cascode [5] amplifier (see Figure 7).

The closed loop stability is obtained with the feedforward technique detailed in [6]. The feedforward technique is implemented by adding passive components R_z and C_z. The values of R_z and C_z are chosen to satisfy the stability condition, as described in [6].

The charge collection deficit for the charges transferred from the detector capacitance C_d into the feedback capacitor C_f is determined by the compar-

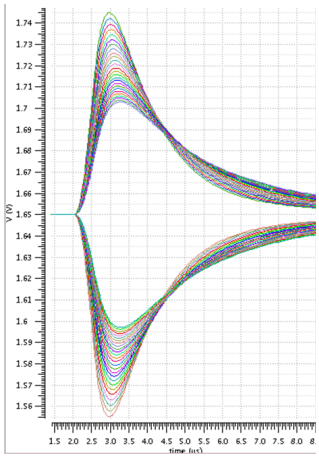

Figure 5: Examples of differential output signals of the LARZIC ASIC

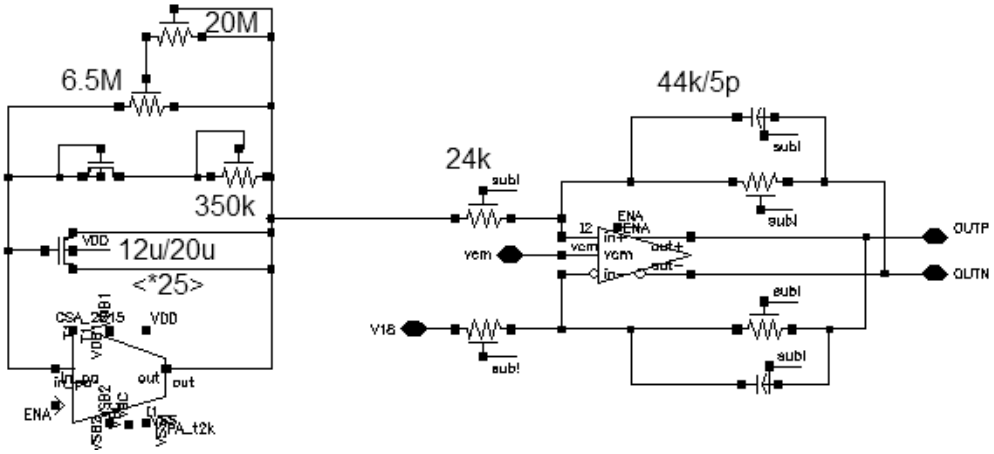

Figure 6: Schematics of the CSA plus the buffer

ison of C_d to the product of the DC gain of the amplifier (AO) times C_f (see Table 3 and Figure 8). This yields, with the current parameters, about 80% of the charges transferred for $C_d = 250pF$.

Higher values of A0 (for instance 100 dB in order to to transfer 97% of the charges) would imply much higher input transistor bias currents. The chosen configuration represents a reasonable compromise between power consumption and charge transfer efficiency.

As the detector strips, to be coupled to the CSA, have large capacitance,

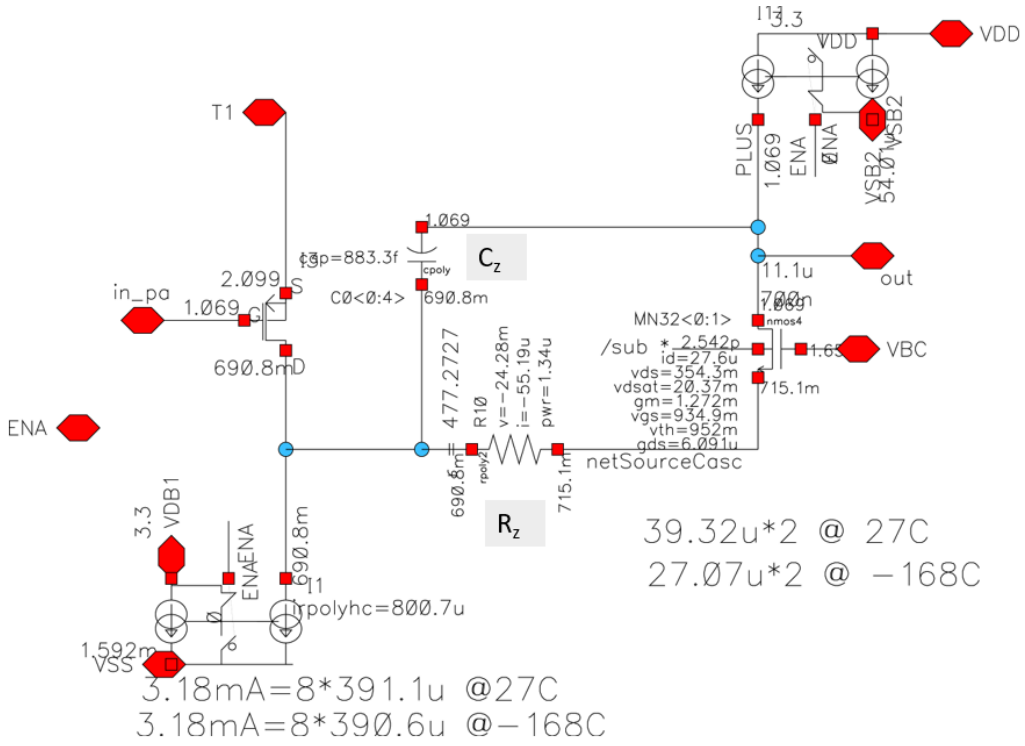

Figure 7: Schematics of the gain stage of the CSA

Parameter	Value (at 110 K)
Input transistor bias current (I_d)	3.2 mA
Cascode transistor bias current	54 μA
Open loop gain A0	78.39 dB
Bandwidth	177 kHz
Gain-Bandwidth Product GBW	1GHz
Pole-zero cancellation: R_z, C_z	477.3 Ohm, 883 fF

Table 3: CSA main characteristics

large size MOSFET are employed, especially for the input transistor (W/L = 8100 μm/0.35μm) in order to reduce the channel thermal noise. The input transistor was implemented with large gate width W (8100 μm) and minimal gate length L (0.35 μm) in order to achieve a high W/L ratio (and so a large g_m helping to reduce the input referred noise) while optimizing the $W \times L$ product in order to optimize the CSA input capacitance.

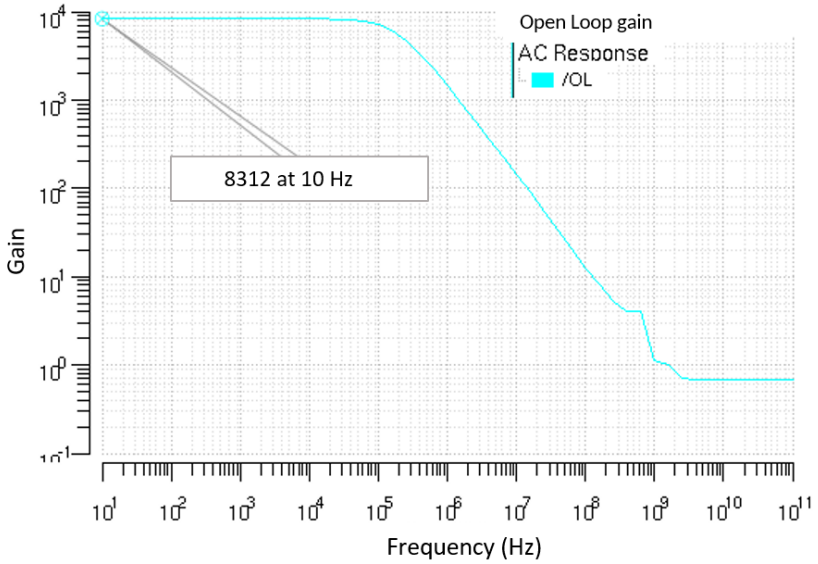

Figure 8: Open Loop gain of the CSA gain stage

1.3.2. Noise considerations

The noise evolves with the temperature. A major noise parameter is the input drain current transistor noise $S_I = \frac{8}{3}kTg_m$. The voltage power spectral density S_V referred to the CSA input is then related to S_I by: $S_V = \frac{S_I}{(g_m)^2}$. Since g_m increases by decreasing the temperature, S_V decreases.

The noise is then dominated by the value of g_m and thus (see equation 1) is determined by: the bias current I_D, the geometry ratio W/L of the transistor, the inversion coefficient n, $\beta = \mu C_{ox} W/L$, depending on the mobility μ of the electrons in the transistor channel and C_{ox} the gate oxide capacitance.

$$g_m = \sqrt{\frac{2\beta I_d}{n}} \tag{1}$$

The mobility is a strong function of the temperature $\mu \approx T^{-\alpha}$ and dependent on the doping level. A standard value of α for low doping levels is 1.5. At a given bias current of the input transistor, g_m will increase as the temperature decreases, which is the case in cryogenic applications. For a temperature variation from room temperature to 110K, the mobility can increase by a factor 4. As a result, g_m increases by a factor two improving the noise performance. Another reduction factor comes from the linear tem-

perature term explicitly present in S_I. Since the ENC depends on the square root of S_V in a first instance a ENC reduction of $\approx \frac{1}{\sqrt{6}}$, slightly larger than a factor two, can be naively expected from these simple qualitative arguments when reducing the temperature from 300K to 100K.

1.3.3. Feedback network

The main characteristics of the feedback network (see Figure 7) are listed in Table 4.

Parameter	Value (at 110 K)
Feedback resistor (R_f)	6.5 MOhm
Feedback resistor on diode branch	350 kOhm
MOSCAP capacitance	115 fF

Table 4: CSA feedback network elements

1.3.4. Dynamic range

The CSA has a linear gain for input charges of up to 400 fC and a logarithmic response in the 400–1200 fC range, corresponding to very high charge levels. This double-slope behaviour was developed for the dual-phase TPC, having in principle stronger signals due to a potentially high gain in the gas phase, and of a single polarity due to the use of only collection views. The double-slope behaviour is obtained by using a MOSCAP capacitor in the feedback network of the amplifier. The MOSCAP changes its capacitance above a certain signal threshold (see Figure 9. The MOSCAP capacitance value in the linear gain regime, of interest for the Vertical Drift application, is 115fF, corresponding to a g_{conv} value of 3.5 mV/fC. The MOSCAP then yields a lower gain for input charges larger 400 fC, corresponding to a MOSCAP capacitance of 25 pF.

The feedback network includes also a branch, which can be externally configured, (R_{diod}) with a resistor of 350 kOhm in series to a diode (which has a threshold of $\approx 0.7V$), acting on the discharge time for high charge values accumulated on C_f. The enabling of this branch in the feedback circuit guarantees, in the dual-slope regime, similar discharge times for signals which are which are exceeding the 400fC or which are smaller than this threshold. The discharge time would be longer for charges larger than 400fC by into account the higher capacitance value taken by the MOSCAP for large charges in the dual-slope regime.

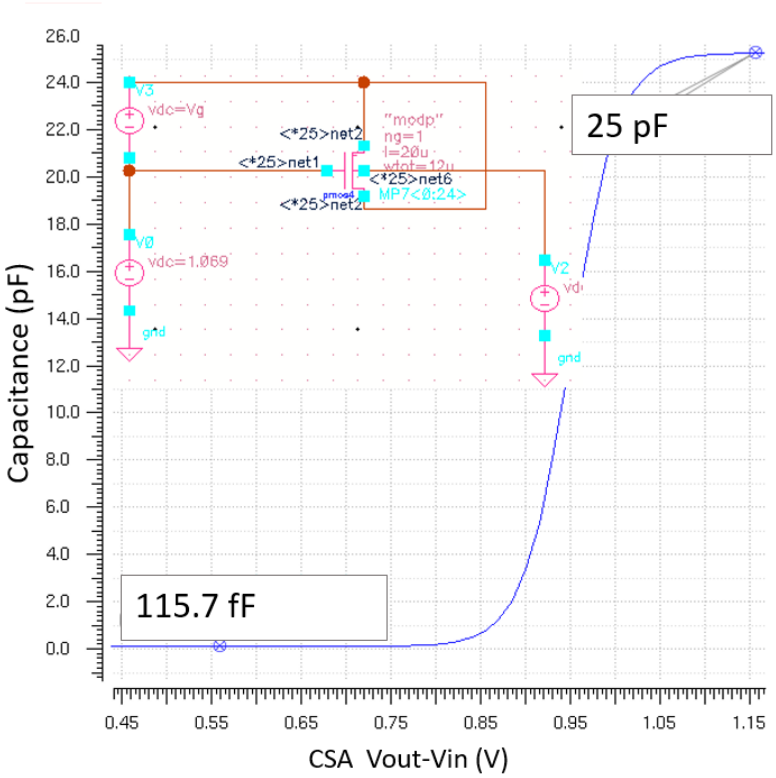

Figure 9: MOSCAP capacitance as a function of the output signal amplitude

The introduction of the diode branch reduces by about a factor 20 the discharge time while the integrated charge on the MOSCAP exceeds 400fC. In this regime the discharge time considering just R_f would be longer due to the change of the MOSCAP capacitance from 115fF to 25pF. This R_{diod} feedback branch allows keeping the total discharge time of the CSA similar in the two regimes: when charges exceeding are 400fC or are smaller than that value. For charges smaller than 400fC the discharge time is instead just determined by the RC constant of the standard feedback branch (R_f=6.5 MOhm and C_f= 115 fF for the MOSCAP).

The possibility for this larger dynamics, beyond 400fC in unipolar mode, was developed for the dual-phase application (with LEM gain of at least 20) and is of little interest for the Vertical Drift, where the dynamics of the entire analog chain has been re-optimized to work in bipolar mode. In this configuration the dual-slope is not activated and the ASIC features a linear

regime up to +-200fC exploited for the Vertical Drift. The signals dynamics is then limited to +-80 fC by the ADC dynamics after accounting also the AMC analog stage. In these conditions the ASIC amplifier works always on the first linear slope.

1.4. Supply voltages

Five independent DC supply voltages are supplied to the FEB for the operation of the ASICs: VCC (supply voltage of the differential buffer), VDD (supply voltage for the output stage of the CSA), VRef (reference voltage used by cascode stage of the CSA with no current drawn), V18 (bias voltage applied to the buffer circuit to separate the signal branches) and V_{Tin} (supply voltage for the input transistor of the CSA). The typical values of these voltages are reported in Table 5

The ASIC can be completely disabled (switched off) with an external control level (ENA). Similarly a control level set on the R_{diod} input allows deselecting the second resistance branch in the feedback network.

Parameter	Value
VCC	3.3 V
VDD	3.3 V
VRef	1.4 V
VTin	2.2 V
V18	1.8 V

Table 5: LARZIC supply voltages

1.5. Charge injection and slow controls

The LARZIC integrates a charge injection system with embedded capacitors (C_{STIM} 1 pF) and a slow control system to select the channels seeing the charge injection from an external signal injection source, connected to the STIM line (Figure 10). The system allows selecting single channels or a desired configuration of channels. This configuration is defined with a SPI bus connected to the ASIC, including input and output data and clock lines (Dzi, Dzo, Dki, Dko).

The possibility of activating the injection on single channels, by the internal charge injection system but also by exploiting dedicated injection boards which can be connected to the input connectors of the FEB, also allows measuring that the cross-talk is negligible (smaller than 1%).

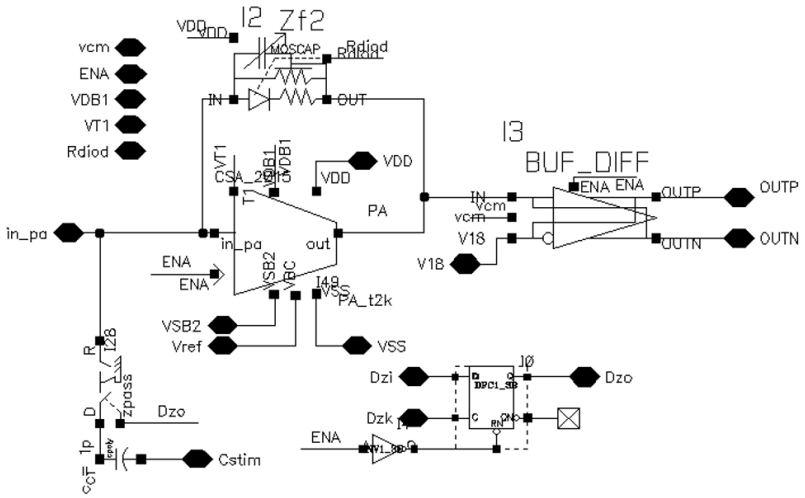

Figure 10: Details of the charge injection system and channels selections

Multiple ASIC devices on the same FEB are daisy chained on the SPI bus using the input and output clock and data connections of each chip (Figure 11).

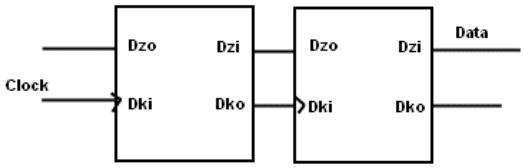

Figure 11: Daisy-chaining of multiple LARZIC devices

1.6. Bonding diagram

The ASIC bonding diagram is presented in the Figures (12, 13). The chip die is bonded in a PQFP-100 package.

The pinout table of the PQFP100 package used for the LARZIC ASIC is shown in Figure 14. The pin numbering refers to the package pins numbering. The names are those of the LARZIC chip pads.

A picture of the ASIC is shown in Figure 15

1.7. Specifications and simulated performance

The LARZIC specifications are summarized by the following set of curves which have been obtained by full simulations taking also into account par-

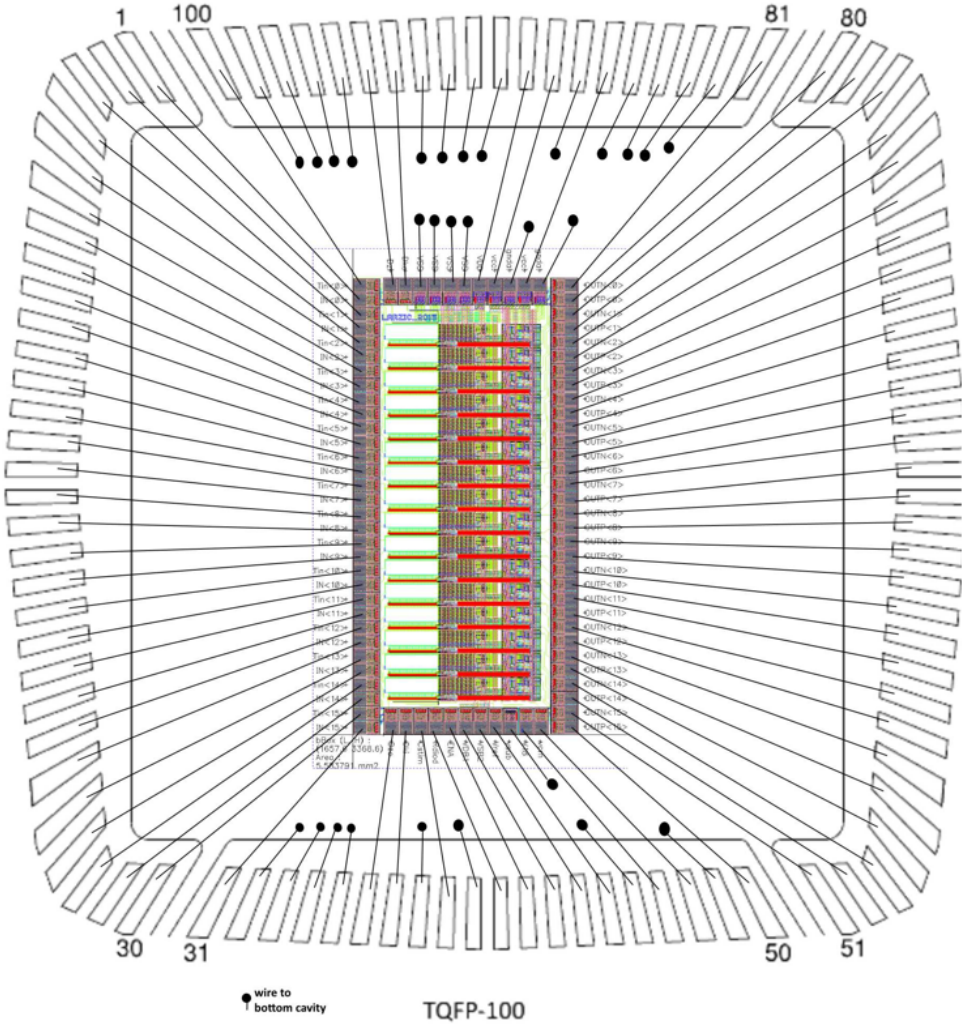

Figure 12: LARZIC_2015 bonding diagram

asitic effects on the chip. Two sets of simulations were performed with extracted parasitic components (R and C). The files provided by the AMS foundry allowed for the extraction of the parasitic components.

One set of simulations was considering the capacitances decoupled from ground. The second set included the coupling of the capacitances to ground. The results showed that dominant parasitic effects are not related to the coupling to ground but to net-to-net coupling inside the chip (decoupled

set). All the results shown in the following are related to this decoupled set of simulations, which were performed with with the CADENCE framework (IC6.1.8).

Figure 16 shows a simulated pulse, as seen at the input of the analog stage of the AMC card after having made the difference between the differential signals produced by the buffer. The amplitude does not include the gain of the ADC buffer. The signal corresponds to an operation temperature of 110K, a detector capacitance of 250pF and to 30fC injected charge.

This capacitance value of 250pF is arbitrarily taken as a typical benchmark point for the noise in the LARZIC specifications. The typical detector capacitance is actually lower than this value.

For instance, capacitance of the final Vertical Drift CRP strips layout is 135pF for the collection strips. In addition to the strips capacitance one has to consider also the capacitance of the flat cables used to connect the CRPs to the SFT chimneys (capacitance per unit of length: 36pF/m). For the maximal flat cable length foreseen in the DUNE FD2-VD CDR for FD2-VD (2.2m) the total cable capacitance corresponds to 79.4 pF. This cable length may be reduced, given the new installation process of the top-drift CRPs discussed at the CRP FDR.

By taking into account the strips capacitance and 2.2m connection cables length, the total capacitance seen by the amplifiers is 135+79.4=214.4 pF. The induction strips have variable length with a maximal length of 1.4m and a corresponding capacitance of 177pF. For the induction views then the capacitance corresponding to the case of the strips of maximal length, associated to 2.2m long flat cables, corresponds to 177+79.4=256.4 pF.

The linearity of the response as a function of the input charge is shown in Figure 17 for an operation temperature of 110K and a detector capacitance of 250 pF. The points are precisely fitted (with deviations from linearity smaller than $\pm 0.1\%$,as shown in 18) by a straight line corresponding to a proportional law with a slope of **2.6 mV/fC**. This curve corresponds to the output of the buffer of the ASIC (input of the AMC analog stage) and it does not include the additional gain achieved at the level of the AMC analog stage which is used in order to fully exploit the ADC dynamics.

In Figure 19 the ENC noise is reported as a function of the detector capacitance (C_{det}) at room temperature (RT) and at 110K. The behaviour with the detector capacitance at cold can be described by the functional form shown in 2 which corresponds to about 630 electrons at 110K for 250 pF. The noise is reduced by about a factor two when going from room temperature to

cold operation conditions. The ENC at 110K is 50.9% of the ENC at room temperature.

$$ENC = 212 + 1.684 \times C_{det}(pF) \tag{2}$$

The ENC behaviour as a function of temperature, shown for a detector capacitance of 250 pF, is presented in Figure 20. If simply approximated by a linear interpolation (superimposed dashed line which allows appreciating the deviations at low and high temperature with respect to the real curve), the ENC as a function of the temperature corresponds to 3 which still represents a decrease by about a factor two in the noise when going from room temperature to 110K.

$$ENC = 242 + 3.251 \times T(K) \tag{3}$$

1.8. Applications performance and operational experience

1.8.1. Reliability

The LARZIC ASIC was successfully operating in 2016-2017 in the $3\times3\times1$ dual-phase demonstrator and in 2019-2022 in NP02 ProtoDUNE dual-phase. In NP02 ProtoDUNE dual-phase the FEBs hosting the ASICS where exposed for long periods to a very intensive sparking activity from the LEMs (tens of thousands of sparks per LEM at about 3 kV) which they successfully withstand without consequences.

The LARZIC front-end boards were then exploited in 2022, at the end of ProtoDUNE dual-phase run for the operation of the detector at 300KV with 6 m drift. 6m long tracks, going though the entire drift length, were cleanly acquired and reconstructed in a dual-phase CRP without LEMs but just with anodes installed (see Figure 21). This was possible despite the fact that the signal levels per readout channel, were lower by a factor 4 with respect to what could be yielded by a Vertical Drift CRP operating in the same detector.

The signal reduction by a factor 4 is just due to the dual-phase CRP anodes configuration. This reduction was independent and added to possible attenuation of the charges along the 6m drift due to the LAR purity. The factor 4 is accounted by the finer pitch of the strips (3mm) on the dual-phase anodes compared to Vertical Drift, by the fact that the dual-phase anodes have no induction views but two Collection views, each one seeing only 50%

of the collected charge and by some extraction efficiency of the electrons from LAr, due to the fact that the anodes where operating in the gas phase.

In the normal dual-phase operation this overall penalty factor is more than compensated by the LEM gain (achieved gain of about 6). However the dual-phase CRP (CRP4) operated for the 6m drift data-taking campaign had no LEMs installed on it but it had just the dual-phase anodes located in the gas phase. Despite the handicap on the signal levels by a factor 4, related to the CRP configuration, and despite the very long drift of 6m, which was totally unprecedented, the front-end electronics based on the LARZIC read out a very clean sample of 6m long tracks with good S/N performance.

The LARZIC ASIC front-end boards were then operated in all the Vertical Drift CRP tests since the very first one in Fall 2021. Two cold-box tests were performed in Fall 2021 with CRP1 and a cold-box test was repeated in June 2022 with a modified version of CRP1 (CRP1b). Then in the second half of 2022 two cold-box tests of CRP2 (the first full size Vertical Drift CRP with the final strips orientation) and one cold-box test of CRP3 were performed as well.

During these 6 cold-box tests the TDE electronics and the LARZIC performed in a very reliable way, promptly operating since the very beginning of each test and without showing any issues. All channels kept active. No channels were lost or damaged during the tests, which overall showed very good stability records, as documented in the next section.

The TDE front-end boards hosting the LARZIC have very good reliability records in operation and robust ESD protections. As the extended experience of about ten years shows, they can be manipulated bare hands without having to worry about possible ESD damages.

1.8.2. Calibration and stability

The calibrations, systematically performed at the QC qualification level, of the front-end boards hosting the LARZIC ASICs showed a remarkable channels response uniformity at 1% level. It was a challenge to develop a calibration system simulating the CRPs and capable of injecting charges with 1% accuracy. Various versions were developed since 2018. First using mechanically tuned and calibrated varycaps and then with embedded PCB capacitors for more practical implementation. These external circuits demonstrated to be able to deliver to the FEB inputs charge calibration signals with 1% channel-to-channel accuracy.

This first calibration method emulates in the QC tests by using external

boards the CRP connection. However the ASIC has also an internal charge injection system with injection capacitors embedded in the ASIC. This second system is slightly less complete than the first one since the charge is injected inside the ASIC and it does not go through the input connector of the FEB. The comparison of the two charge injection methods showed in the laboratory tests equivalent performance. Both systems, by addressing single channels on each ASIC allowed proving that the cross-talks levels on nearby channels are negligible and lower than 1%.

The charge injection system implemented in the ASIC allows performing in situ calibrations at warm and at cold of the electronics when this is fully installed in the cold-box and connected for the CRP readout. This capability has been systematically exploited in order to check the stability and reproducibility of the readout system during the CRP tests. The procedures for the determination of the calibration constants imply the injection of different charge levels and the measurement of the linearity slopes channel-by-channel, as shown in the example in Figure 22 where the curves at cold and at room temperature are shown. The definition of the gain constants follows the standard DUNE techniques described in the ProtoDUNE single-phase performance paper ([7]). It can be appreciated from the picture that the gain at cold is about 13% larger than the one at room temperature.

Figure 23 shows the systematic application of this calibration procedure. The measured gain values at cold, in occasion of the two cold-box tests of CRP2 and the cold-box test of CRP3, are superimposed for all channels. One can notice that the averages of the two sets of calibration constants corresponding to the two runs of CRP2 are within 1% and they also correspond to the set of CRP3. The other information is that the spread of the calibration constants over all channels is represented by a gaussian distribution with a an RMS of 2.5%.

These values, which are generally inclusive of the entire TDE chain and not just the LARZIC response, show that even without taking into account the measured gains the response is intrinsically quite uniform and reproducible over the entire CRP readout system.

Similar considerations on the response stability can be drawn by reconstructing tracks and measuring physics quantities as the dE/dx from cosmic ray muons. In this case the distributions show the overall stability of the detector response including the CRP and the readout electronics.

Figure 24 shows the dE/dx distributions for samples of cosmic ray tracks collected by the top-drift electronics in two runs of CRP1 respectively per-

formed in November 2021 (CRP1) and in June 2022 (CRP1b). The Landau distributions (in red and black) perfectly overlap and they are barely distinguishable.

1.8.3. Noise levels

Noise levels have been systematically measured before and after the application of the Coherent Noise Removal (CNR), since the very first cold-box test of CRP1 in Fall 2021. The presence of coherent noise in the cold-box setup has been largely improving since the installation in 2022 of an isolation transformer with little coherent noise remaining before the application of the CNR.

Noise levels are represented by using the DUNE standard "sample noise" definition, as adopted since the ProtoDUNE single-phase performance paper section 4.3 ([7]). The calculation of the channels gain calibration constants, described in the previous section is also performed following the same analysis technique.

Since the very first test of CRP1 it was noticed that the noise levels, following the standard DUNE noise analysis technique, are equivalent as those measured in NP04 ProtoDUNE single-phase and similar for the top-drift and bottom-drift readout electronics. Figure 25, shows the noise levels at cold for all channels measured in the cold-box tests of CRP2 and CRP3, before and after the application of CNR. The two CRPs were cabled with flat cables of 2.2 m length, after removal of some small coherent noise features they show equivalent performance.

Figure 26, contains the measured FFT spectra of the noise in CRP3 after residual coherent noise removal. The integral of the noise power spectrum is reduced by a factor two when going from room temperature to operation temperature at cold.

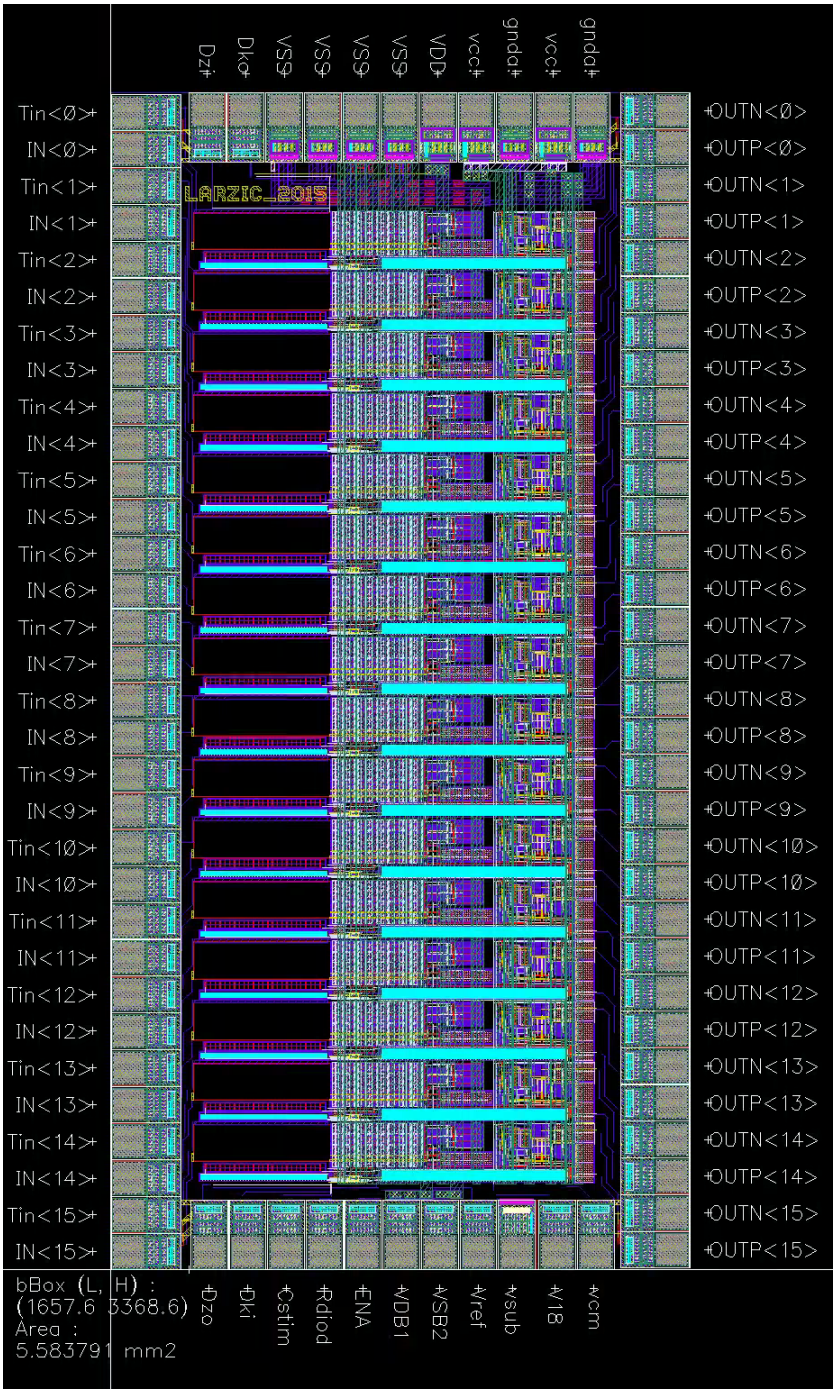

Figure 13: LARZIC layout with I/O pads names

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	In 0	31	In 15	51	OUTN 15	81	OUTN 0
2	Tin 1	32	GND	52	OUTP 14	82	GND
3	In 1	33	GND	53	OUTN 14	83	GND
4	Tin 2	34	GND	54	OUTP 13	84	GND
5	In 2	35	GND	55	OUTN 13	85	GND
6	Tin 3	36	Dzo	56	OUTP 12	86	VCC
7	In 3	37	Dki	57	OUTN 12	87	GND
8	Tin 4	38	GND	58	OUTP 11	88	VCC
9	In 4	39	Stim	59	OUTN 11	89	VDD
10	Tin 5	40	GND	60	OUTP 10	90	GND
11	In 5	41	Rdiod	61	OUTN 10	91	GND
12	Tin 6	42	ENA	62	OUTP 9	92	GND
13	In 6	43	VDB1	63	OUTN 9	93	GND
14	Tin 7	44	VSB2	64	OUTP 8	94	Dko
15	In 7	45	Vref	65	OUTN 8	95	Dzi
16	Tin 8	46	GND	66	OUTP 7	96	GND
17	In 8	47	V18	67	OUTN 7	97	GND
18	Tin 9	48	VCM	68	OUTP 6	98	GND
19	In 9	49	GND	69	OUTN 6	99	GND
20	Tin 10	50	OUTP 15	70	OUTP 5	100	Tin 0
21	In 10			71	OUTN 5		
22	Tin 11			72	OUTP 4		
23	In 11			73	OUTN 4		
24	Tin 12			74	OUTP 3		
25	In 12			75	OUTN 3		
26	Tin 13			76	OUTP 2		
27	In 13			77	OUTN 2		
28	Tin 14			78	OUTP 1		
29	In 14			79	OUTN 1		
30	Tin 15			80	OUTP 0		

Functions:
Signal Inputs
Signal Outputs
Supply voltages
Controls

Figure 14: Pinout table of the PQFP100 packaging

Figure 15: Picture of LARZIC_2015

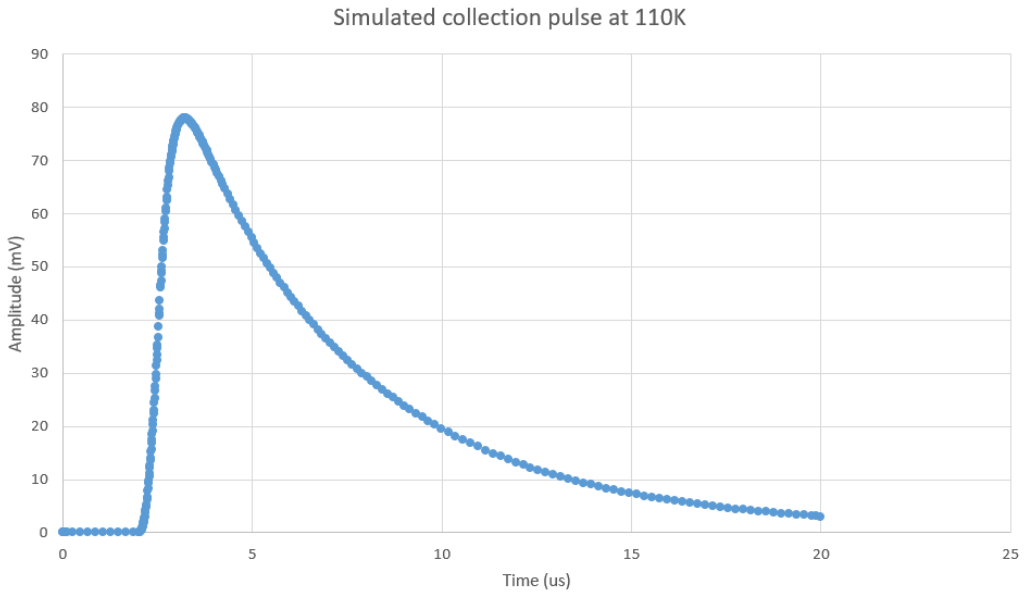

Figure 16: Simulated pulse at cold for 30fC injected charge and 250pF detector capacitance

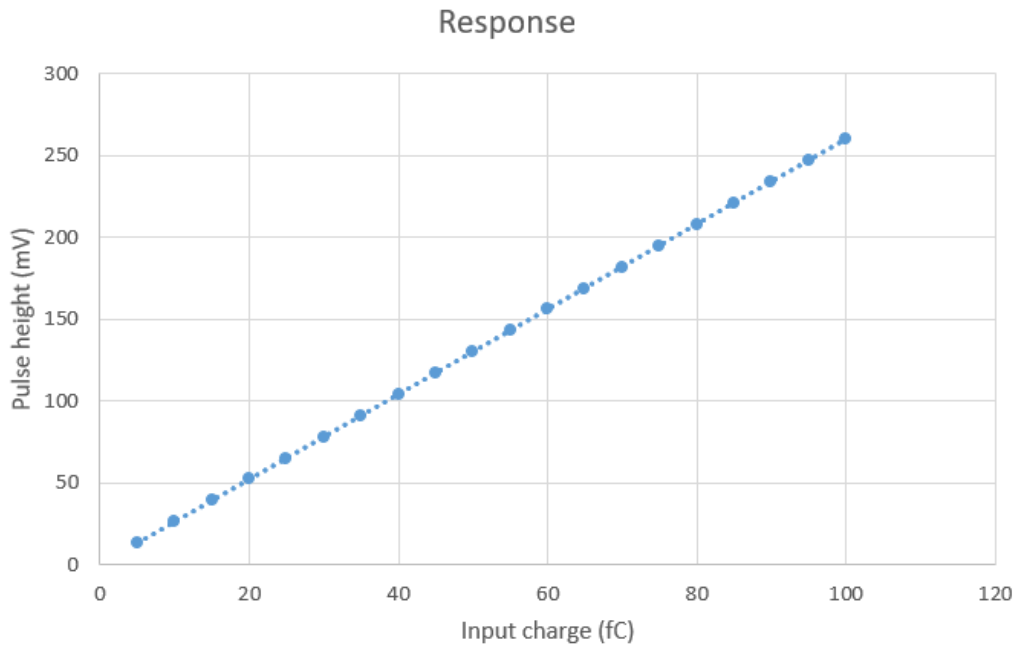

Figure 17: Linearity curve of the LARZIC response at 110K

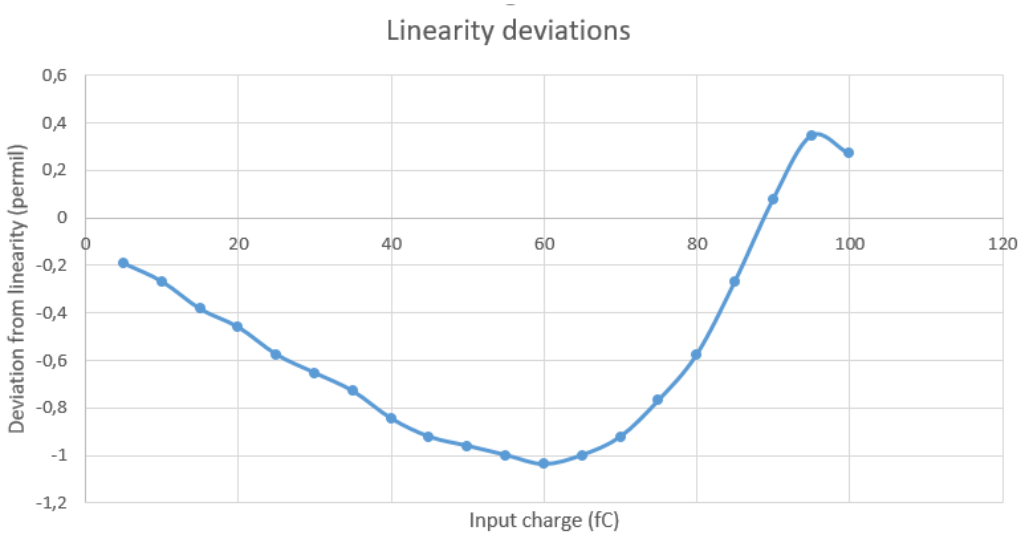

Figure 18: Linearity deviations of the LARZIC response at 110K, the vertical axis is in per mil

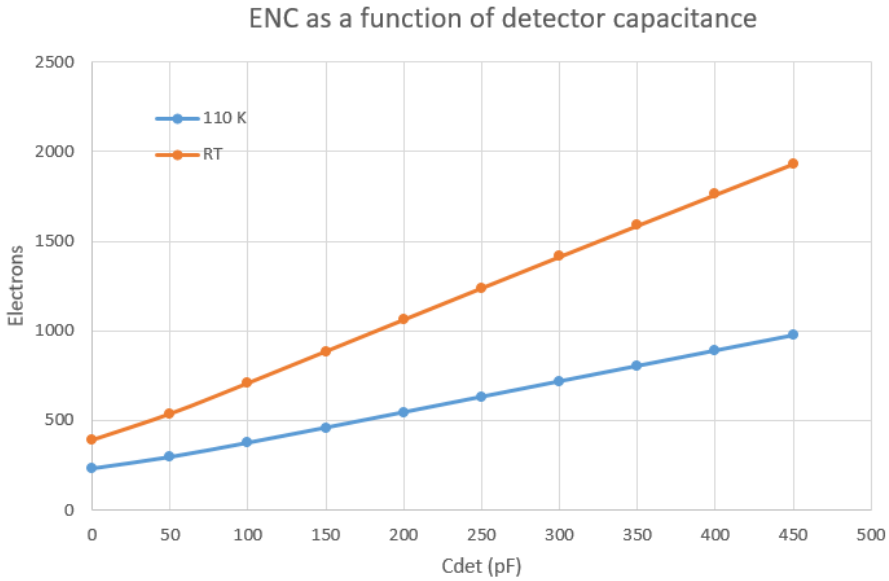

Figure 19: ENC dependency on the detector capacitance

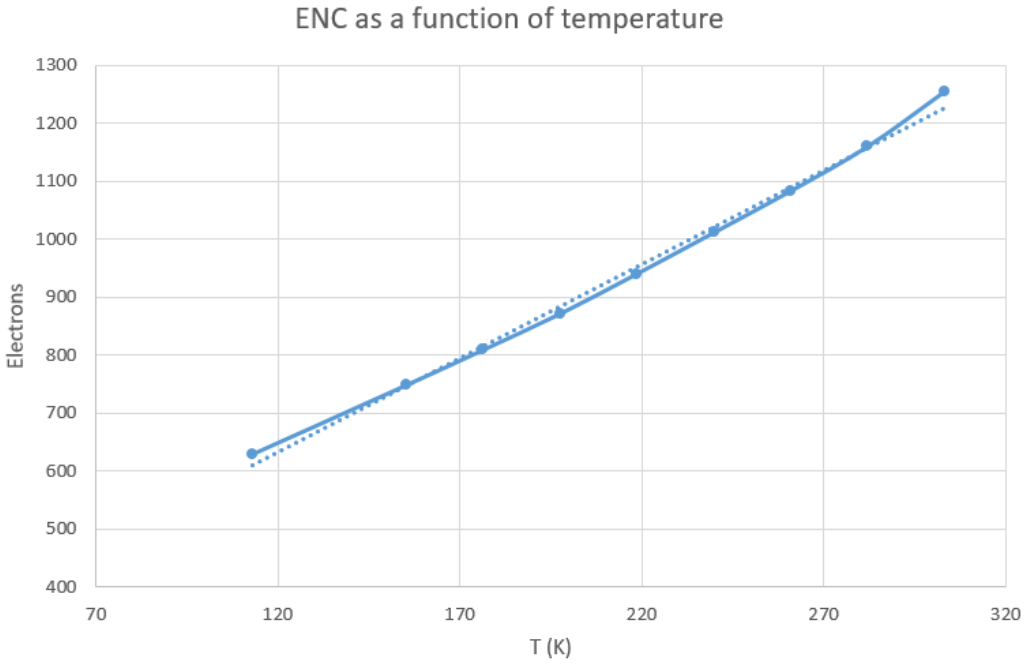

Figure 20: ENC dependency on the temperature, calculated for 250 pF detector capacitance

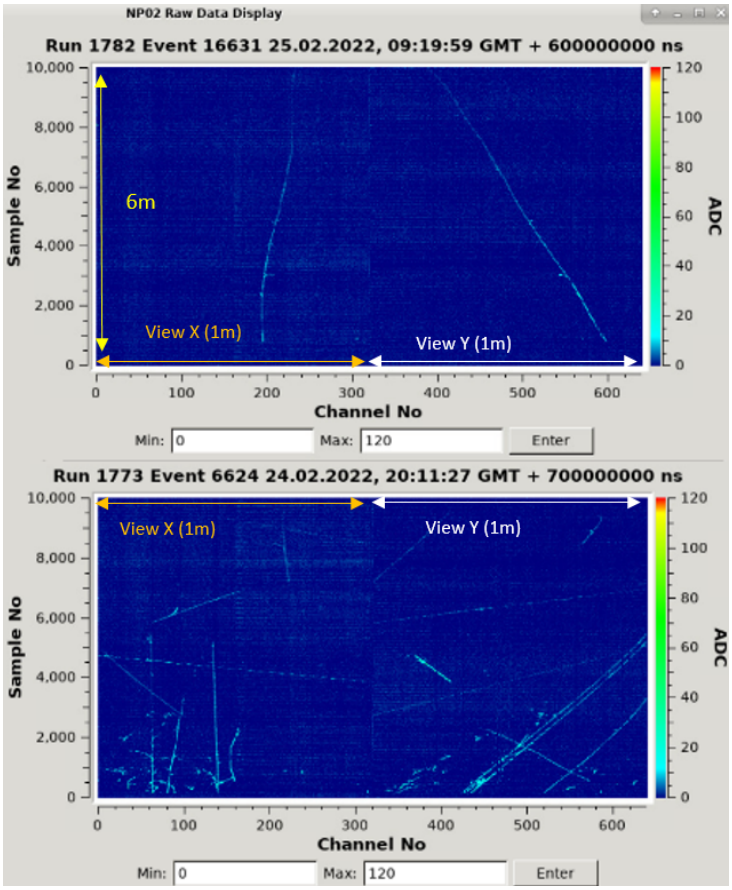

Figure 21: Cosmic ray tracks acquired with with the top-drift electronics operated in ProtoDUNE dual-phase demonstrating 6m drift

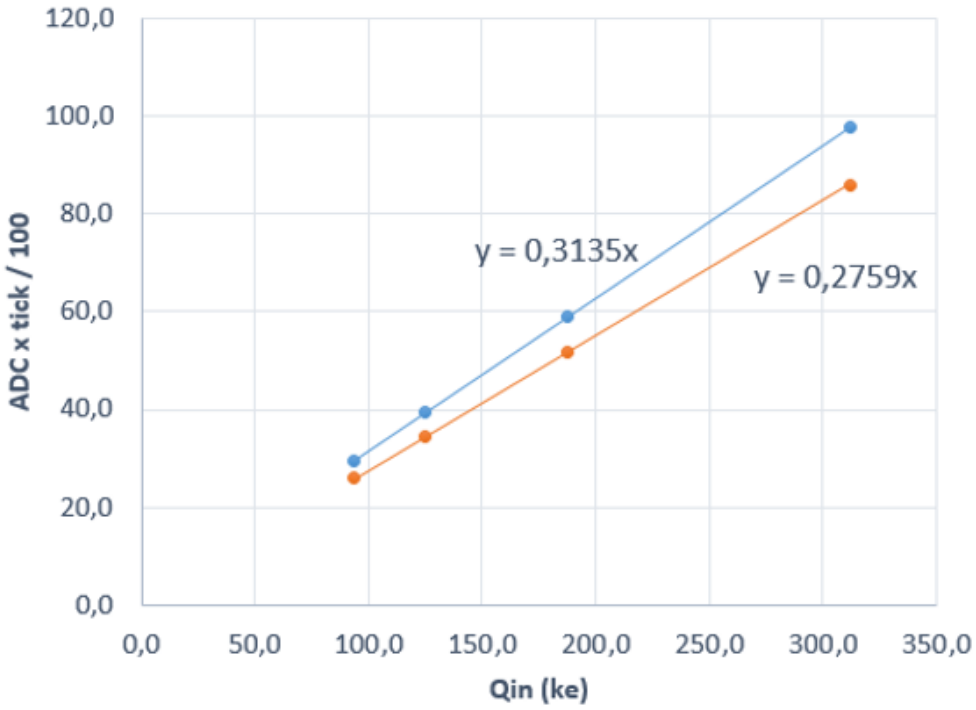

Figure 22: Example of in situ gain calibration at cold and warm by exploiting the LARZIC charge injection system

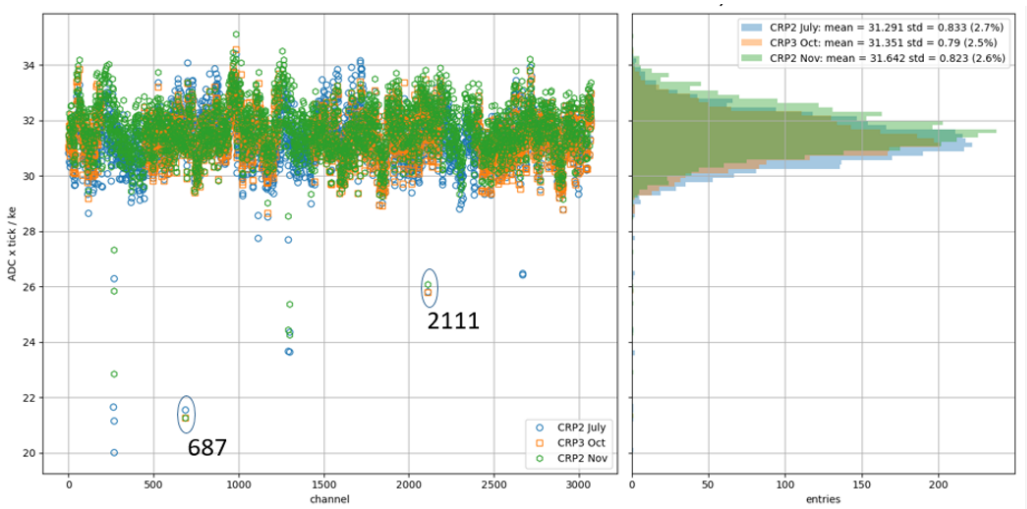

Figure 23: Reproducibility of the measured gain values for different cold-box runs of CRP2 and CRP2

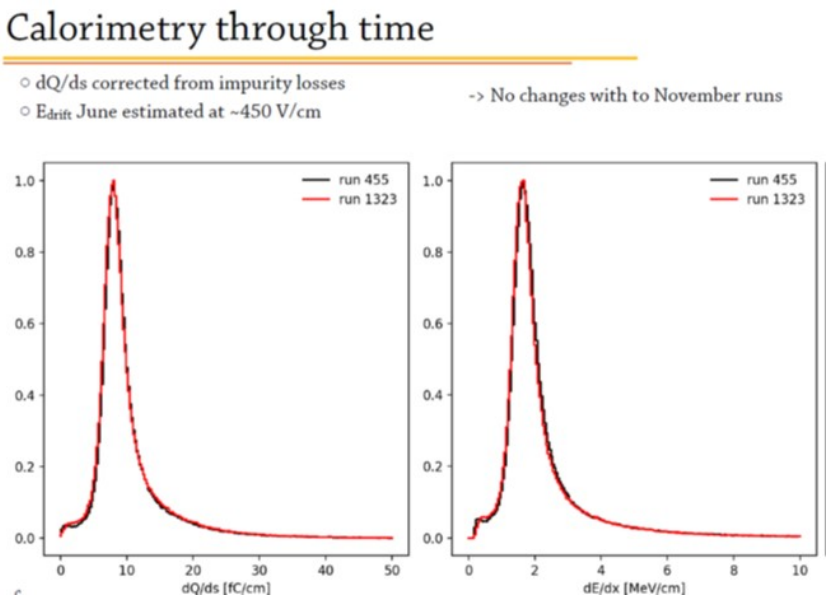

Figure 24: Reproducibility of dE/dx for the TDE readout of CRP1 in two different runs taken at 6 months time

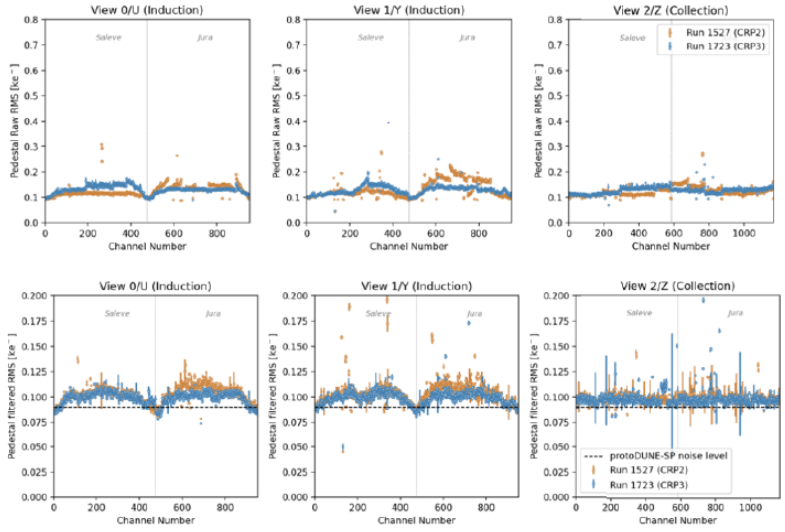

Figure 25: Noise levels measured at cold on CRP2 and CRP3 and compared to the ProtoDUNE-SP noise levels (dashed line)

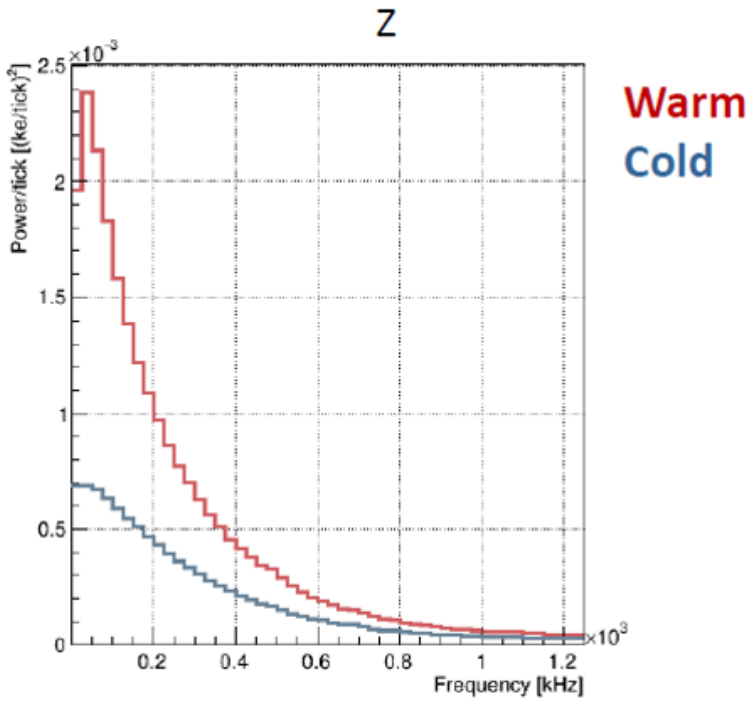

Figure 26: FFT analysis and measured noise reduction when going from room temperature to operation temperature with the cold-box test of CRP3

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