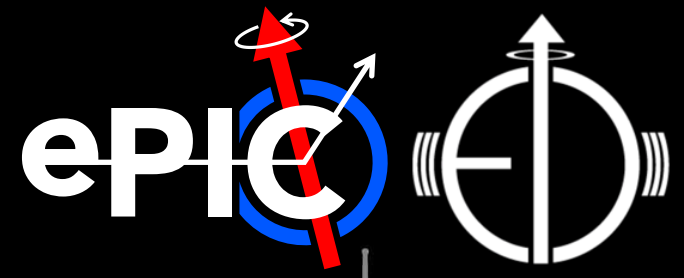




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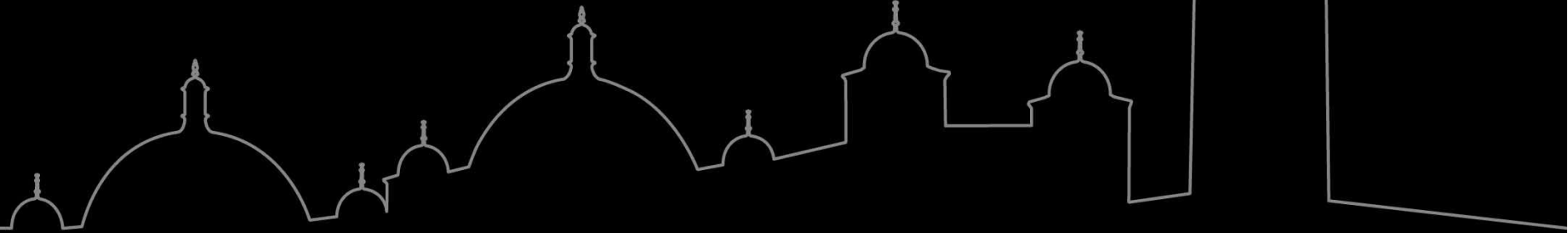


# UK readout plans

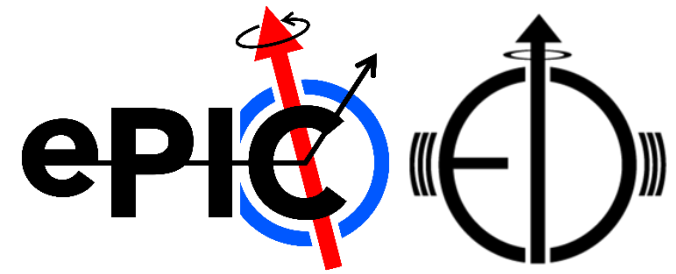
James Glover

EIC-UK WP1 meeting

Wed, 24<sup>th</sup> Sep 2025



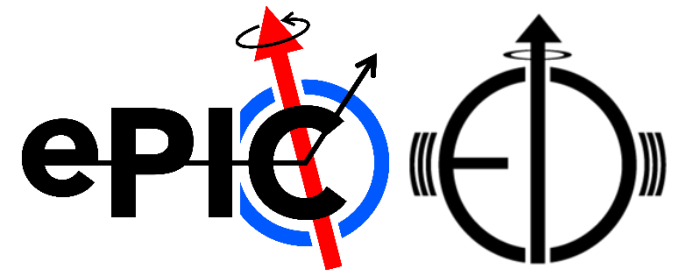
# Main testing hub @ RAL



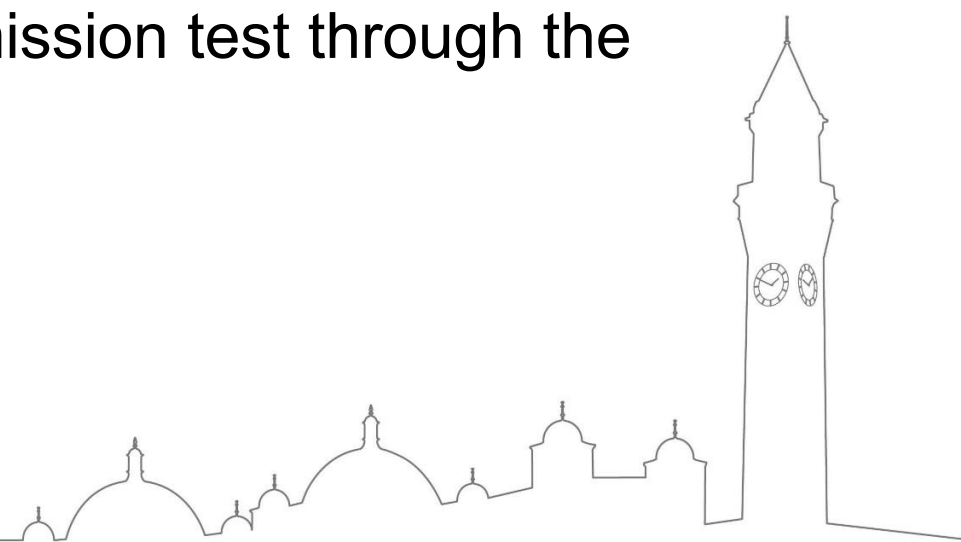
- Readout testing is (so far) being done by B'ham, Oxf + RAL.
  - PCB design and assistance also coming from Daresbury.
- RAL is to be the main location for the readout testing.
- Most equipment needed is already @ RAL.
  - FPGA dev kits (both KCU105 and ZCU102 available).
  - VTRx+ and IpGBT interconnection boards (VLDB+ and ORNL's "MOSAIX mockup board") – populated with VTRx+ & IpGBT.
  - Oscilloscopes – permanent access to 8/10GHz scopes, with occasional access to a 33GHz scope (incl. optical probes on the latter).
- 2<sup>nd</sup> VLDB+ set-up available @ B'ham
  - Confirm transmission settings prior to running tests @ RAL.



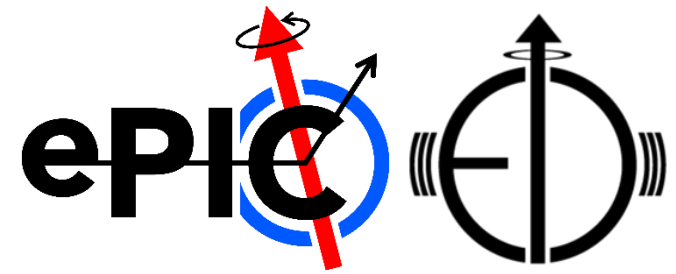
# Limited time/man-power



- Fergus, Todd and James have set-up what we have so far.
- Atanu @ RAL has been a great asset to get us this far.
- Roy is (soon) to have more time for ePIC-related tasks.
  - Come October will start to look at data transmission test through the FPC differential transmission lines.



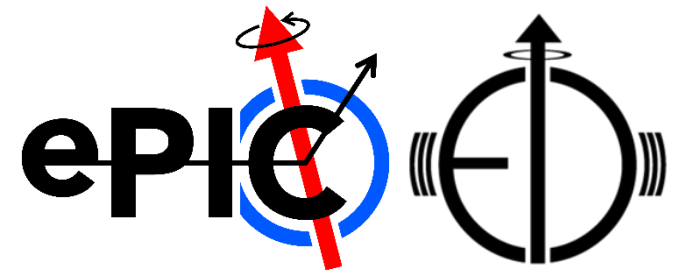
# Optical readout



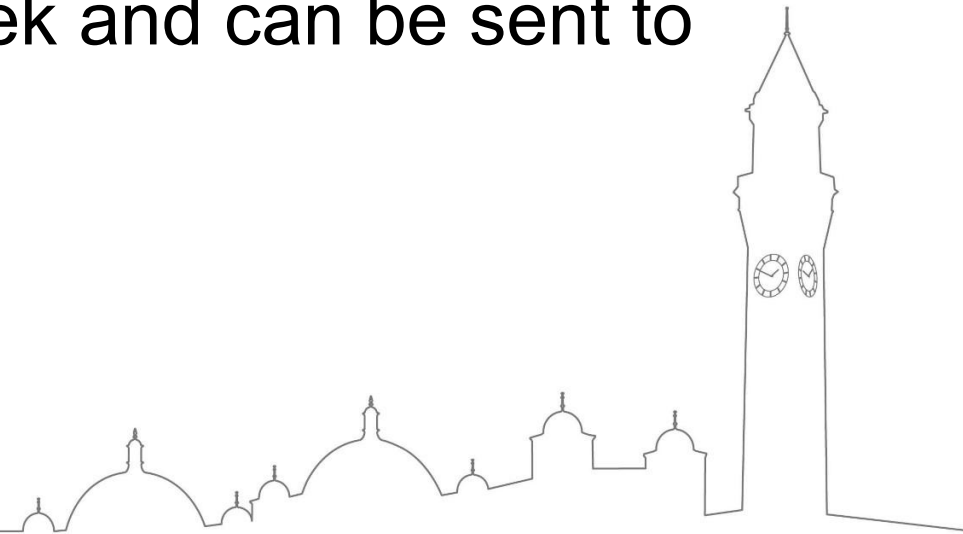
- Equipment in hand to replicate Jo Schambach's MOSAIX mockup set-up.
  - FPGA board to emulate MOSAIX (utilising the ITS3 MOSAIX emulator).
  - ORNL design PCB for VTRx+ interface (all the fibres of an SIB; 8DataUp, 1S/Cup, 1S/Cdown, on 3 VTRx+).
  - 2<sup>nd</sup> FPGA board to process optical signals back to electrical.
  - Repository of information in [1<sup>st</sup> SVT WP5-UK meeting](#).
- Firmware to now being populated in the [EIC GitHub](#).
  - Joining instructions can be found at: [github.com/eic/.../README.md](https://github.com/eic/.../README.md)
  - Specific team set up: [github.com/orgs/eic/teams/epic-svt-readout](https://github.com/orgs/eic/teams/epic-svt-readout)



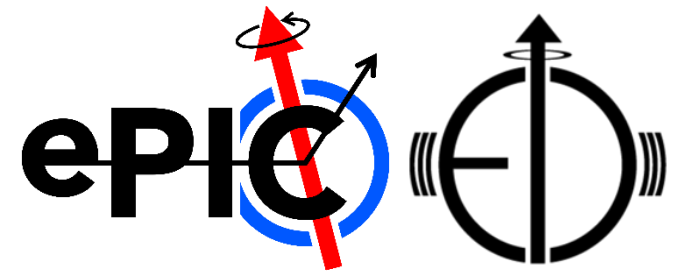
# Electrical data transmission



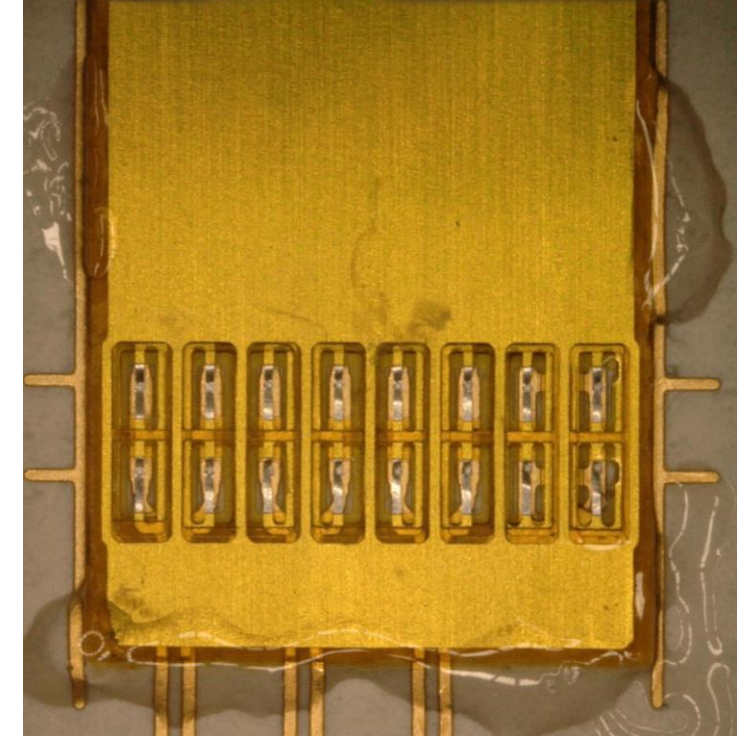
- Roy to start testing the prototype FPCs for transmission integrity over the full trace length with spTAB connections to PCBs.
- Testing to happen @ RAL.
- 2<sup>nd</sup> FPC prototype has been bond this week and can be sent to RAL ready for Roy's testing.



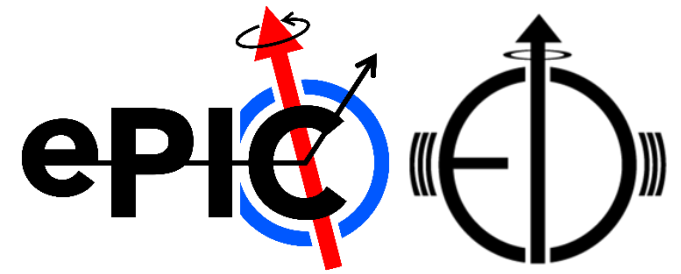
# M-FPC prototype 2



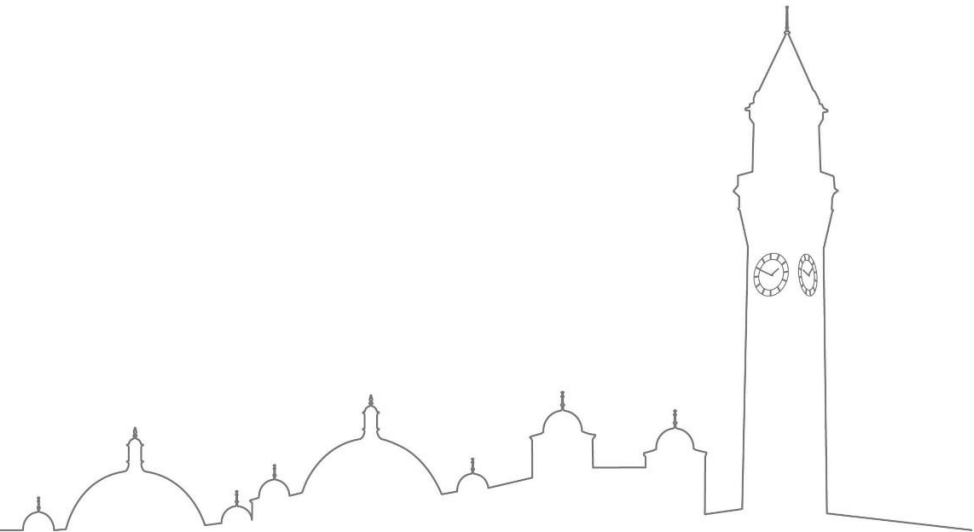
- New FPC installed using an update jig from Oxford.
- Nylon stand-offs used as weights to aid alignment of FPC.
- UV-cure glue-dots used to hold FPC flat and aligned during bonding.
- Additional glue added to FPC edges post-bonding.



# Summary



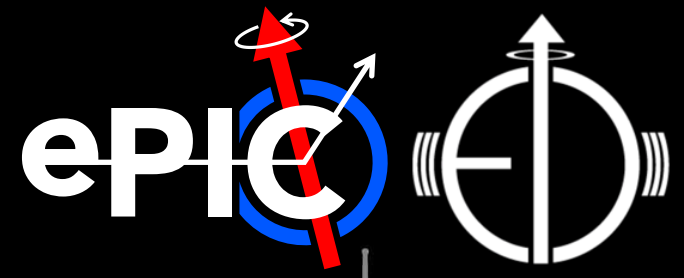
- RAL is to be a testing hub for most readout tasks.
- Optical readout systems are being prepared.
- Transmission line testing to commence soon.
- Latest FPC prototype ready for testing.





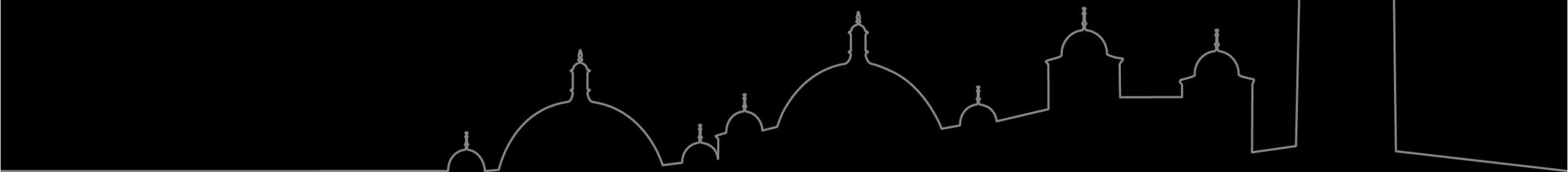


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# Thank you very much!

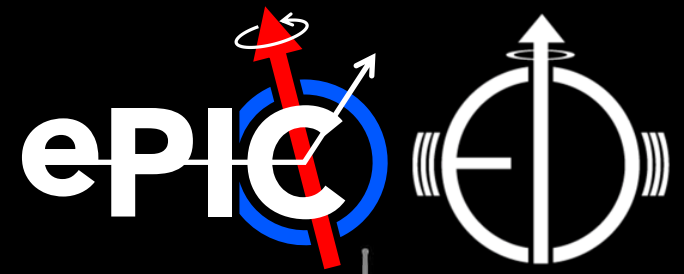
Any questions?



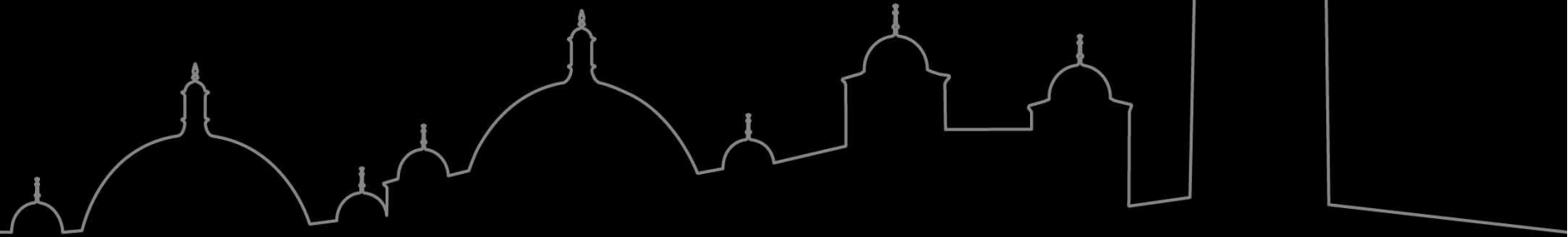




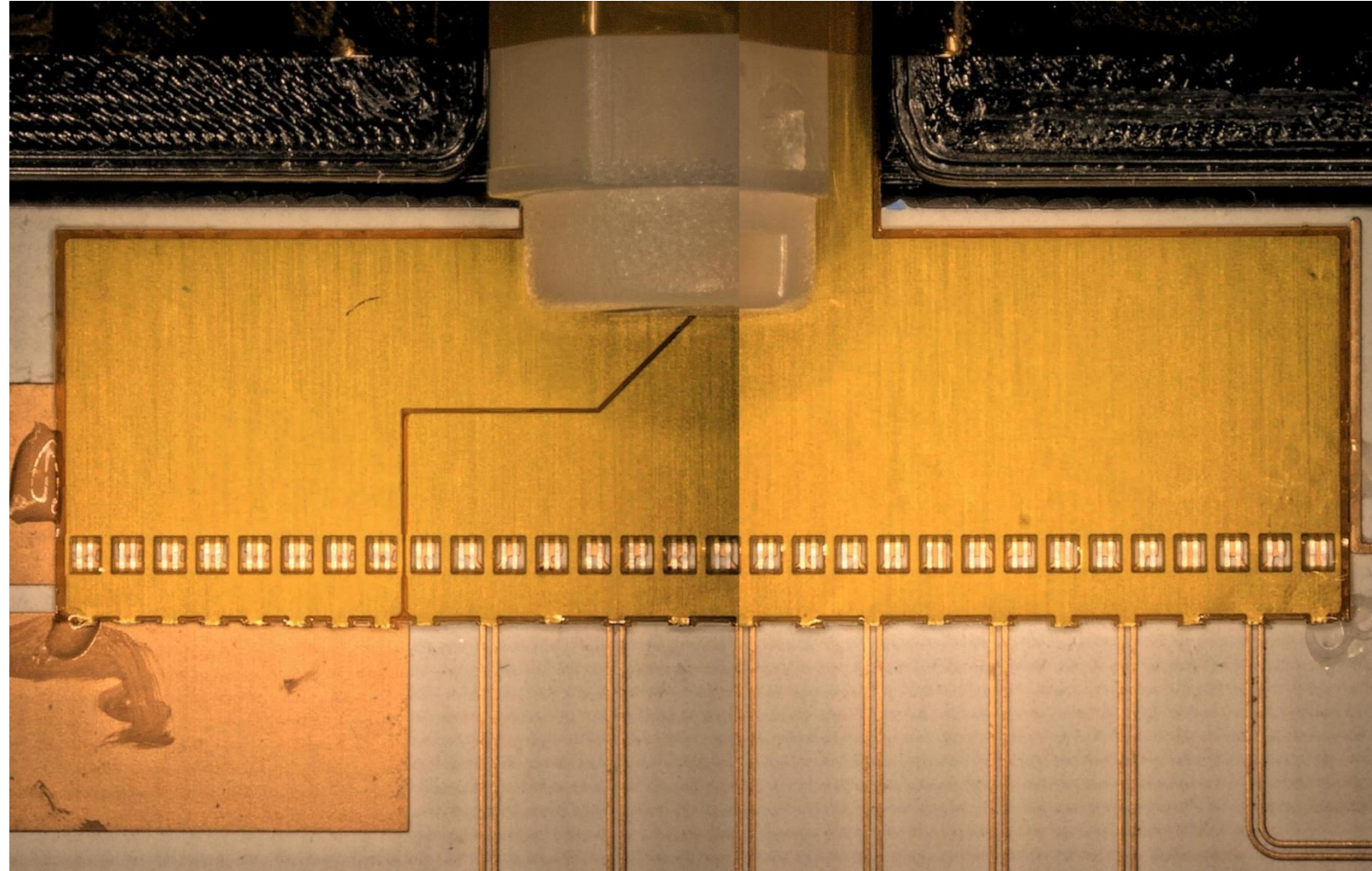
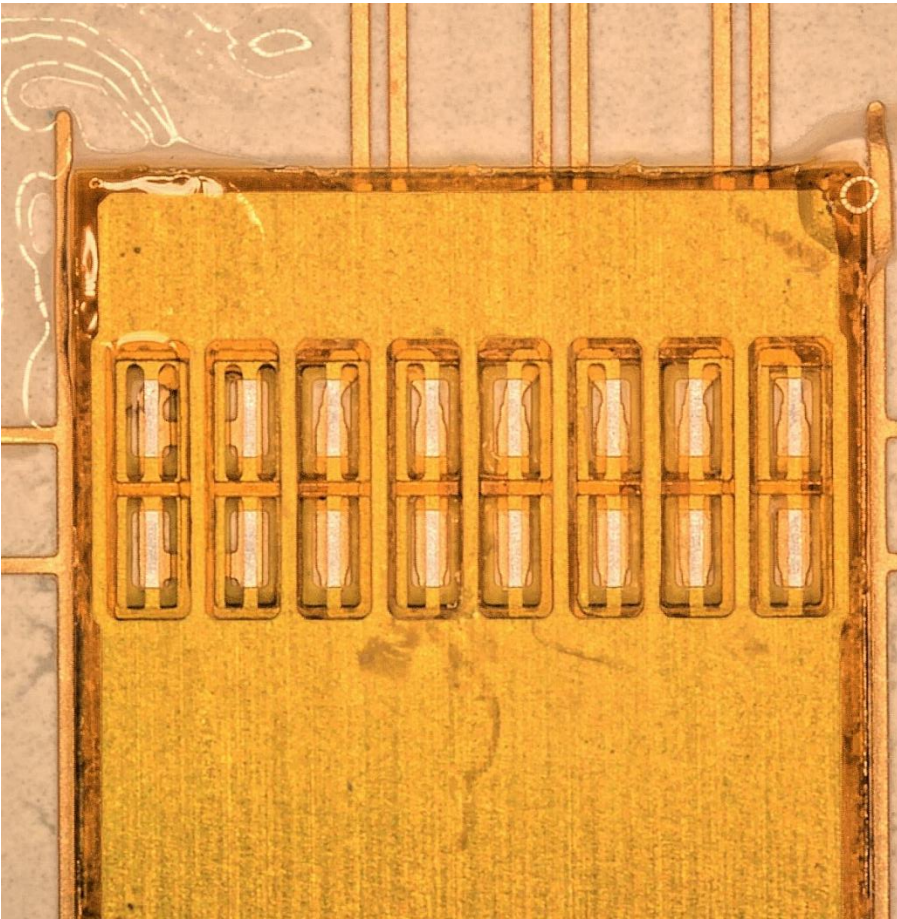
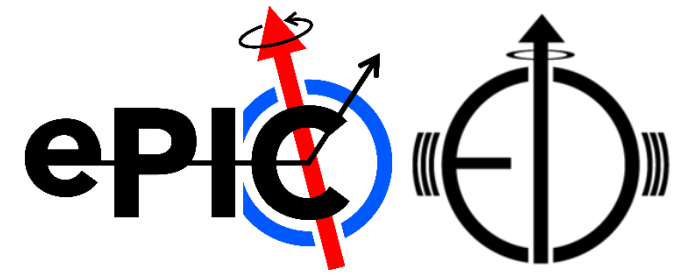
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# Additional (support) slides



# Glued



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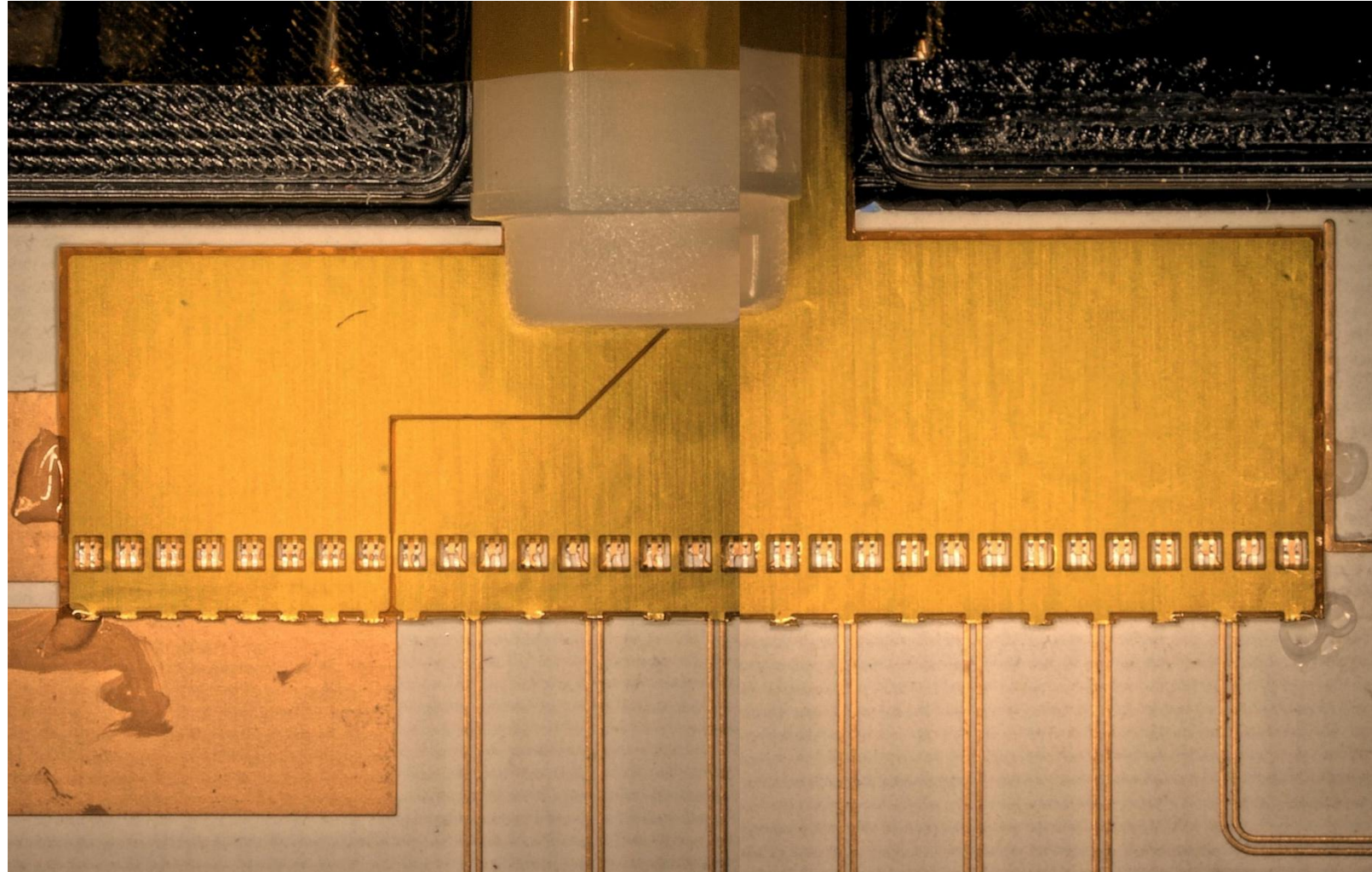
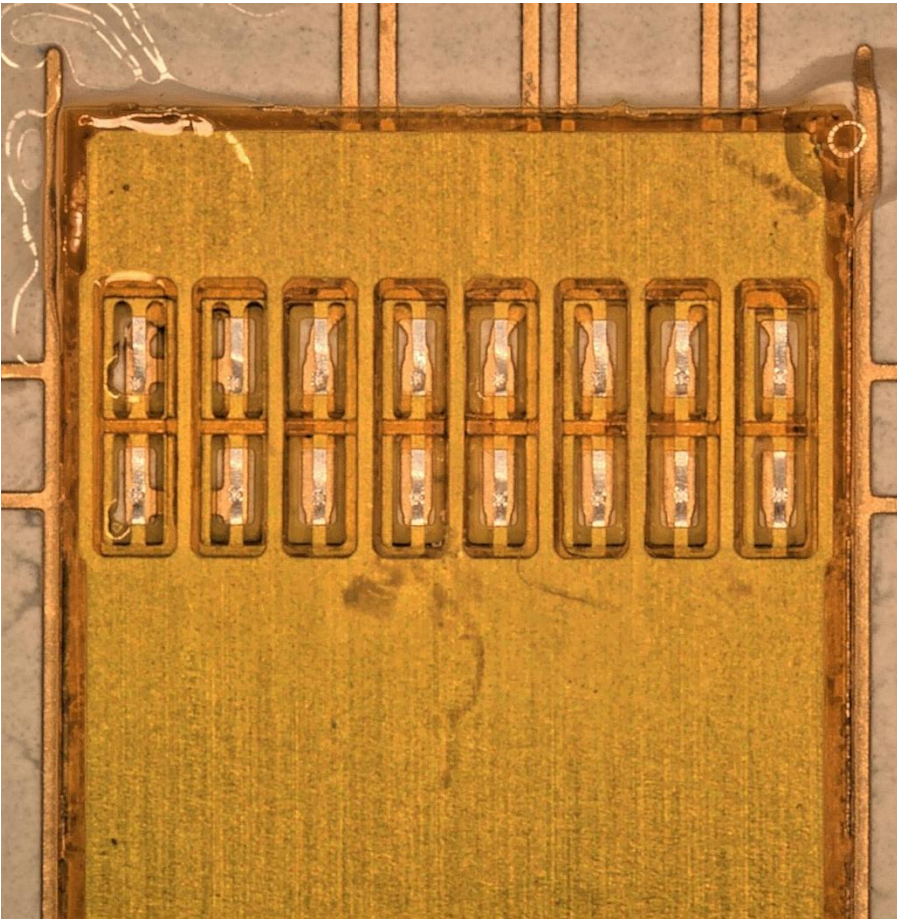
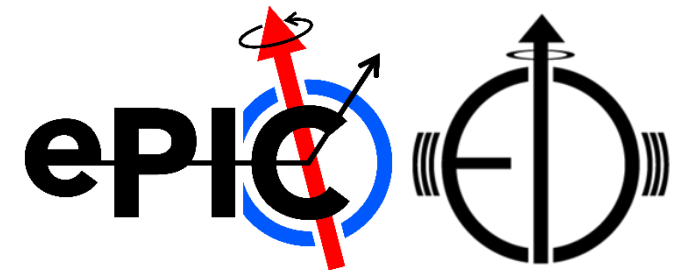
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# Bonded



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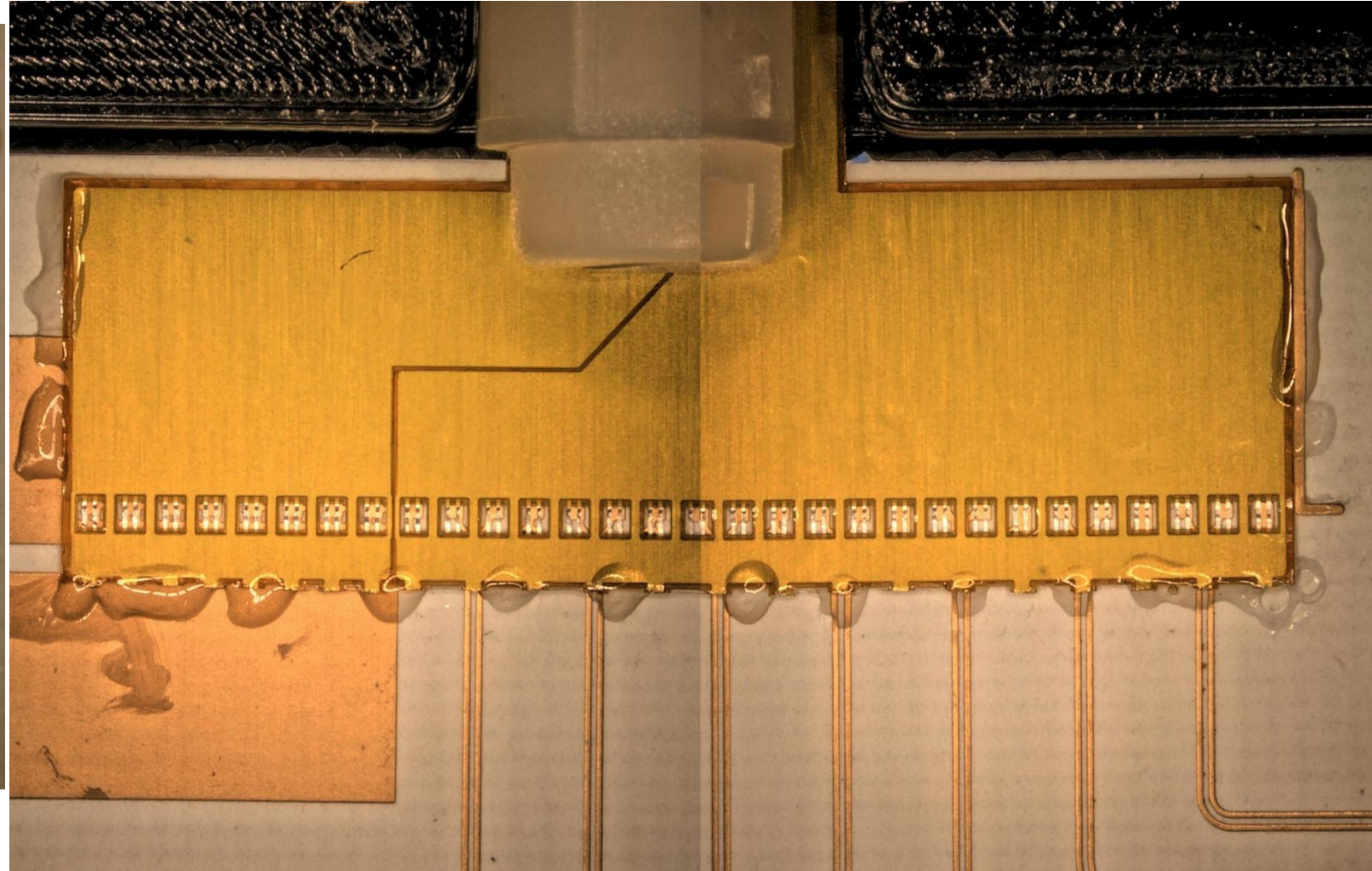
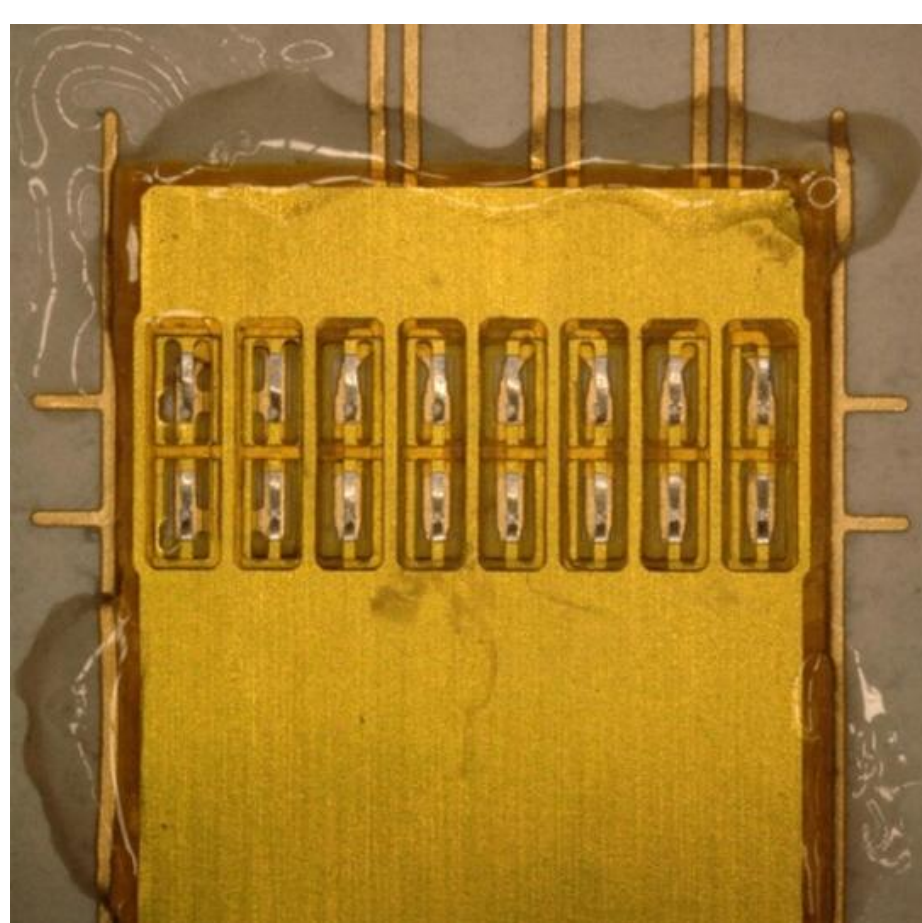
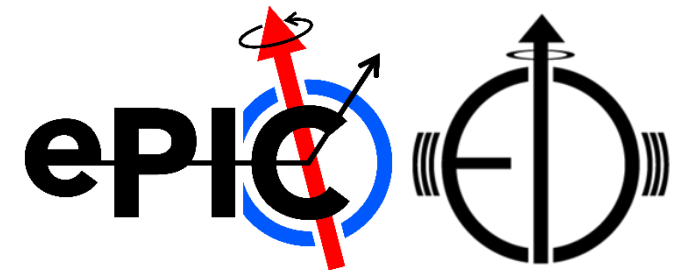
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# Secured



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