

eRD109 update: dRICH RDO

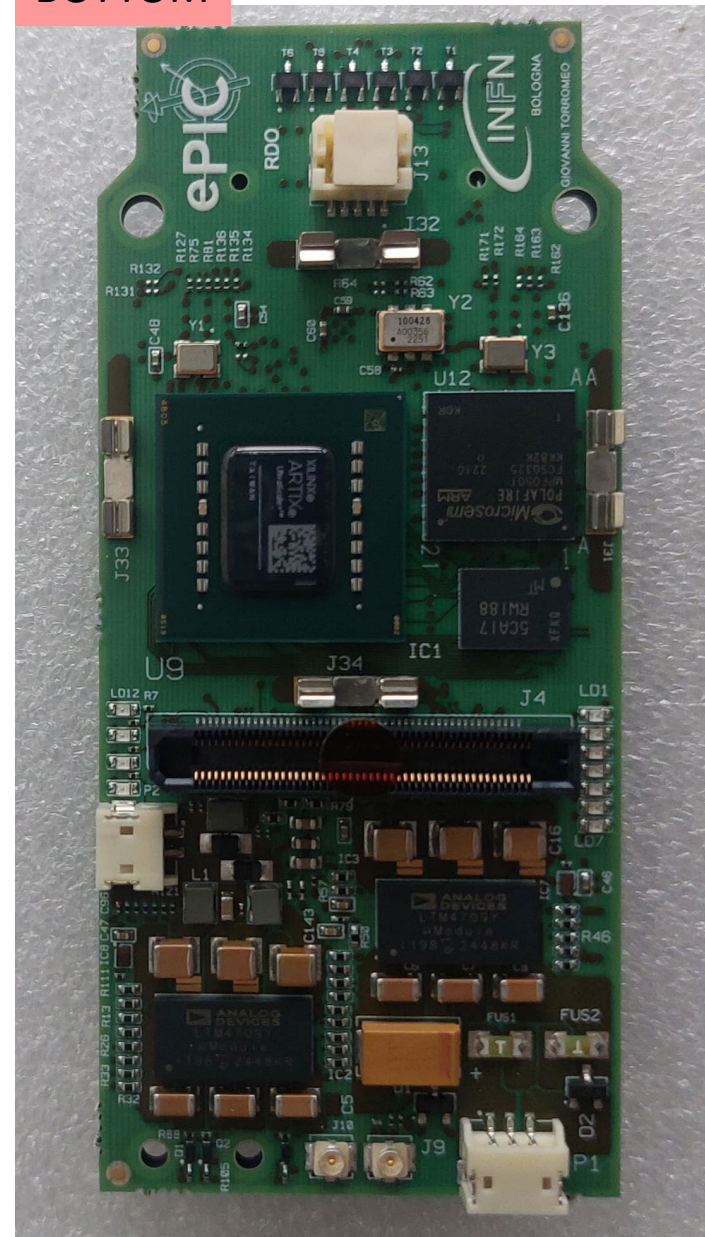
Pietro Antonioli, Davide Falchieri, Sandro Geminiani, Luigi Rignanese, Giovanni Torromeo
on behalf of the INFN Bologna RDO team

TOP



We received 2
complete RDO boards
on 24th July 2025

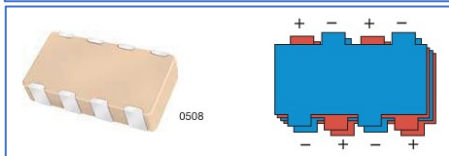
BOTTOM



A detailed, colorful illustration of a smartphone's internal components, showing the motherboard, processor, memory, camera, and other hardware parts. The components are arranged in a symmetrical layout, with the processor and memory modules at the top, the camera and other sensors at the bottom, and the battery and other components in the center. The illustration is highly detailed, showing individual components like the processor, memory modules, camera, and various sensors, as well as the overall layout of the motherboard. The colors are vibrant and the style is clean and modern.

FL1 removed to not power U7

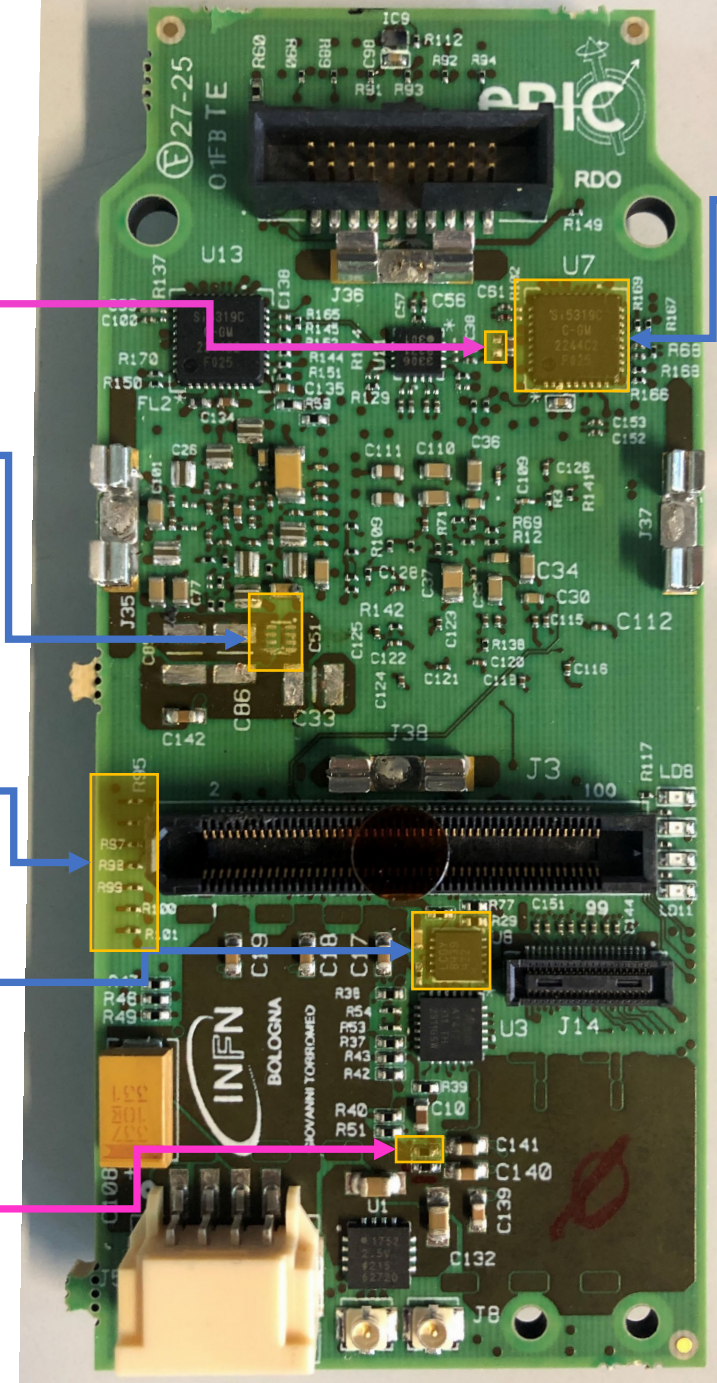
Problem with
footprint of **C51**



Changing value of resistors:
R95,R96,R97,R98,R99
R100, R101 from 33 Ω to 330 Ω

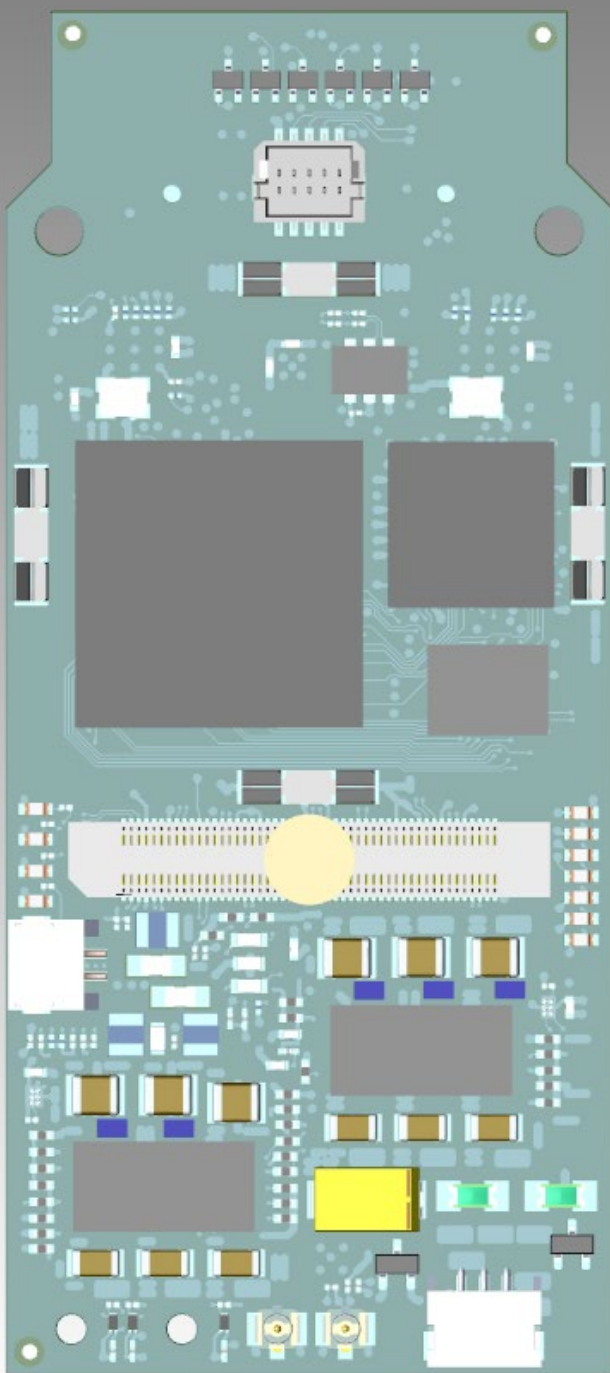
Problem with **U8**
LTC3203BEDD-PBF

R19 1.5K changed to 2.2K Ω to correct VOH level with wrong U8 (charge pump at 5V)



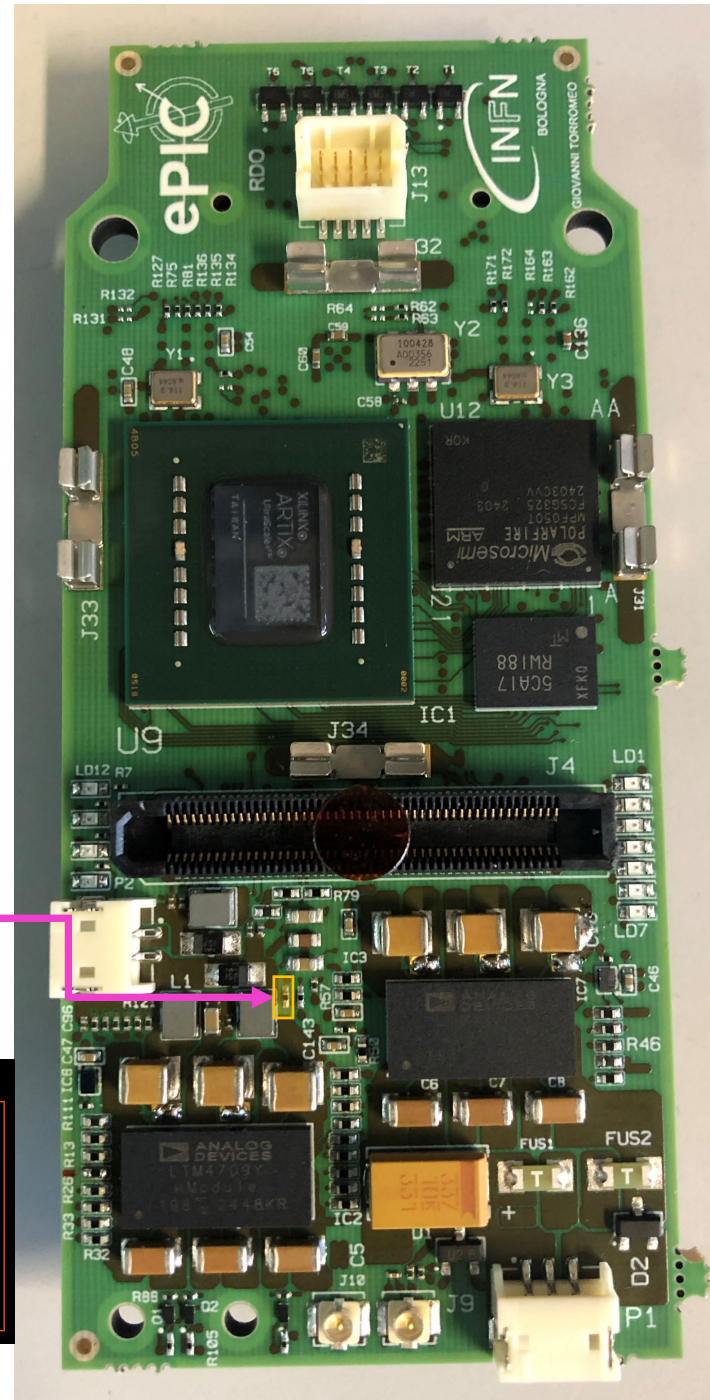
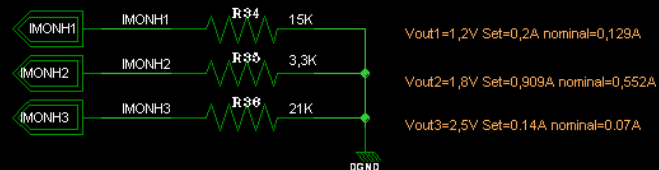
U7
Si5319
instead
Si5326

TOP





R34 15K Ω changed
with 8.2K Ω
to set 1.2V
Iout limit

Resistor to set the LDO maximum current and convert the current Iout to voltage for ADC ATtiny

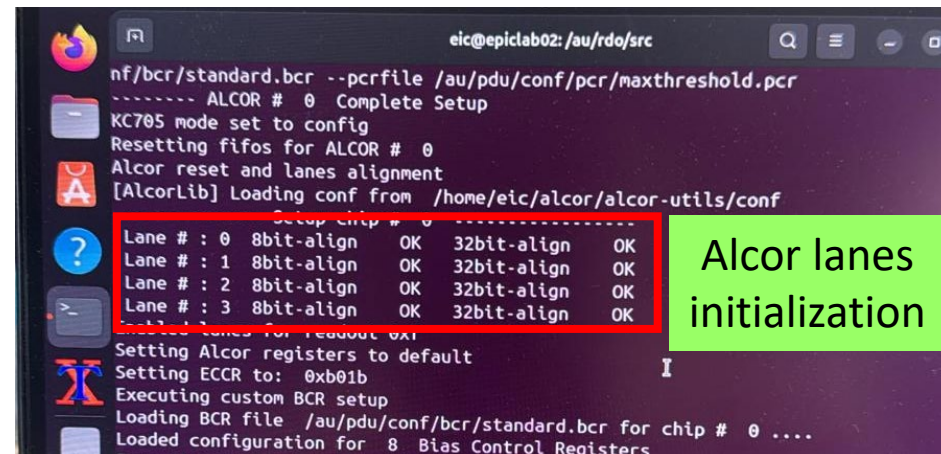


BOTTOM

First tests on RDOs

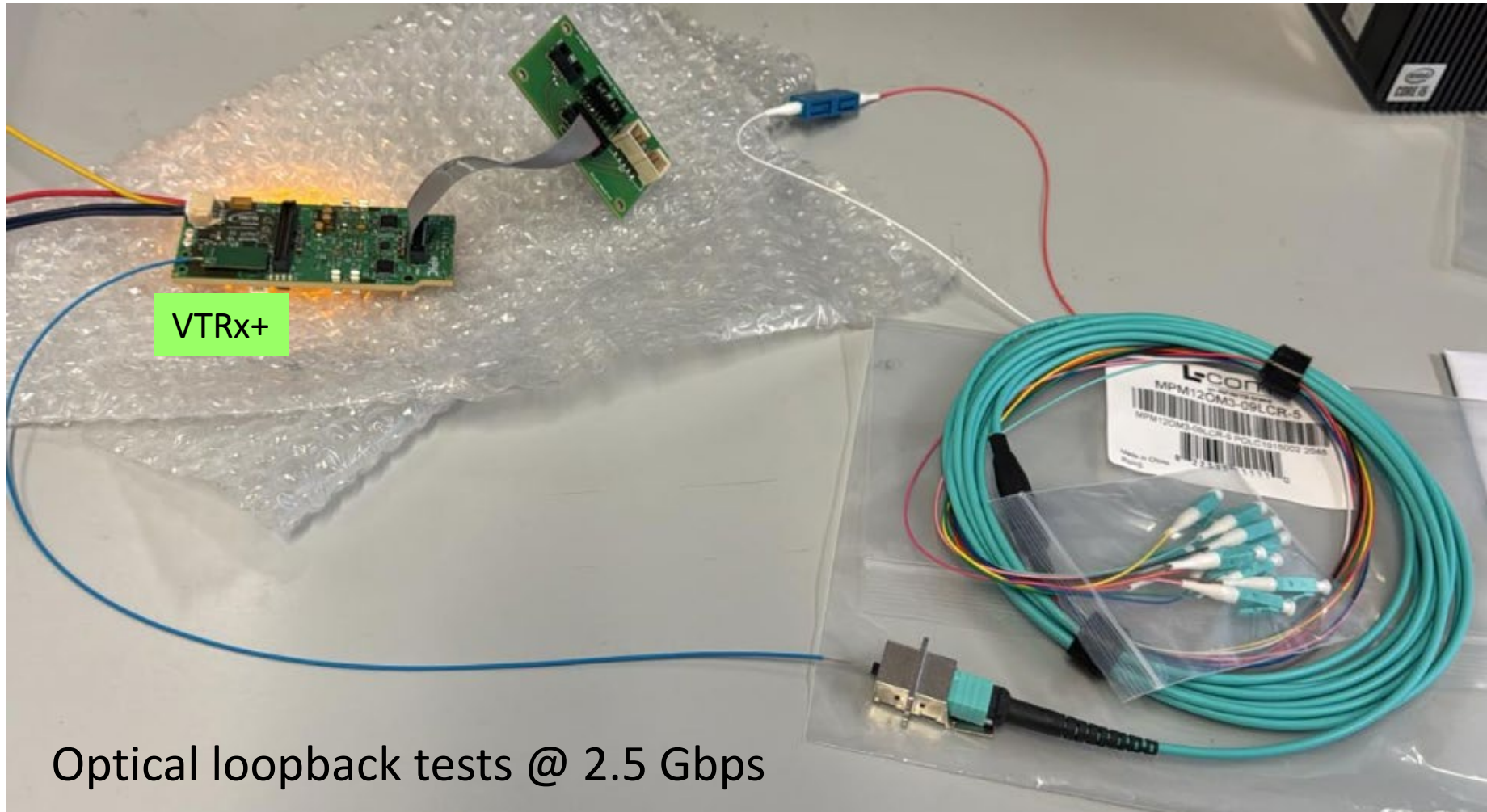
- ✓ 1. mechanical pairing with fake-FEB
- ✓ 2. power-up: 2.5V / 1.4V jumper to avoid power to other sections
- ✓ 3. program μ C via external connector
- ✓ 4. power-up with μ C (after programming the μ C): check LDO Vouts
- ✓ 5. program Artix US+ via external connector
- ✓ 6. program Polarfire via external connector
- ✓ 7. program Artix \rightarrow SkyWorks (programming 125 MHz of Si5319)
- ✓ 8. check the power consumption
- ✓ 9. check UFL I/Os
- ✓ 10. link IPbus via VTRx+ [MT-MPO adapter + MPO-LC fibers]
- ✓ 11. program ALCOR via fake-FEB (via IPbus \rightarrow VTRx+) 
- ✓ 12. ALCOR readout (via IPbus \rightarrow VTRx+) 

```
FEB # 0 TOP Master OK
FEB # 1 TOP Slave OK
FEB # 2 BOTTOM Master NOT REACHABLE
FEB # 3 BOTTOM Slave NOT REACHABLE
----- FEB # 0 ALCOR32 chip # 0 Complete Setup
RDO mode set to config
ECCR  : 0xB01B 0xB01B 0xB01B 0xB01B
BCR   : 0x003D 0xC72C 0x003D 0xC72C 0x003D 0xC72C 0x003D 0xC72C
Ch. 00: 0x7777 0x8888 0xFFFF 0x0202
Ch. 01: 0x7777 0x8888 0xFFFF 0x0202
Ch. 02: 0x7777 0x8888 0xFFFF 0x0202
```



```
eic@epiclab02: /au/rdo/src
nf/bcr/standard.bcr --pcrfile /au/pdu/conf/pcr/maxthreshold.pcr
----- ALCOR # 0 Complete Setup
KC705 mode set to config
Resetting fifos for ALCOR # 0
Alcor reset and lanes alignment
[AlcorLib] Loading conf from /home/eic/alcor/alcor-utils/conf
Setup chip # 0
-----
Lane # : 0 8bit-align OK 32bit-align OK
Lane # : 1 8bit-align OK 32bit-align OK
Lane # : 2 8bit-align OK 32bit-align OK
Lane # : 3 8bit-align OK 32bit-align OK
-----
Setting Alcor registers to default
Setting ECCR to: 0xb01b
Executing custom BCR setup
Loading BCR file /au/pdu/conf/bcr/standard.bcr for chip # 0 ....
Loaded configuration for 8 Bias Control Registers
```

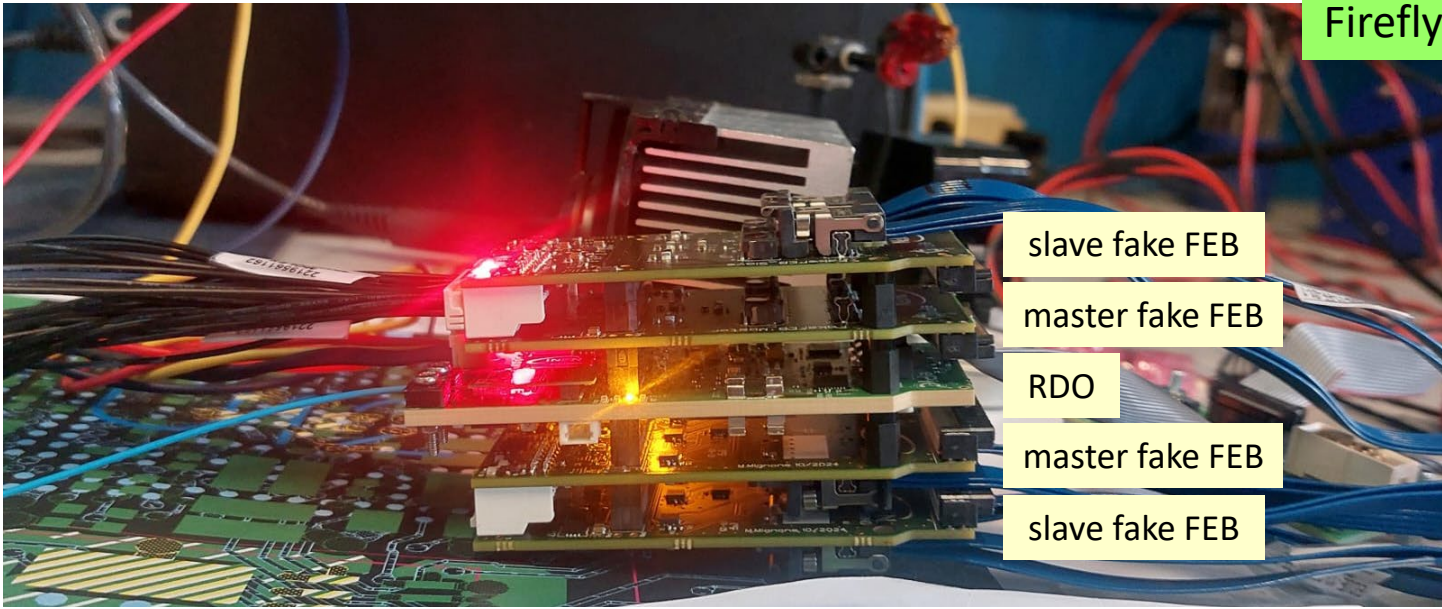

US+ - VTRx+ validation tests



Optical loopback tests @ 2.5 Gbps

We used the IBERT core on the US+ firmware to test the FPGA-VTRx+ devices on loopback mode @ 2.5 Gbps: no errors found

First RDO setup



Firefly cables

FEBs



4 dual FEBs each with 2 32ch Alcor chips

RDO with 2 master fake FEBs + 2 slave fake FEBs

optical fiber

NIC card



```
eic@epiclab02: /au/rdo/src
nf/bcr/standard.bcr --pcrfile /au/pdu/conf/pcr/maxthreshold.pcr
----- ALCOR # 0 Complete Setup
KC705 mode set to config
Resetting fifos for ALCOR # 0
Alcor reset and lanes alignment
[AlcorLib] Loading conf from /home/eic/alcor/alcor-utils/conf
Setup chip # 0
Lane # : 0 8bit-align OK 32bit-align OK
Lane # : 1 8bit-align OK 32bit-align OK
Lane # : 2 8bit-align OK 32bit-align OK
Lane # : 3 8bit-align OK 32bit-align OK
Setting Alcor registers to default
Setting ECCR to: 0xb01b
Executing custom BCR setup
Loading BCR file /au/pdu/conf/bcr/standard.bcr for chip # 0 ....
Loaded configuration for 8 Bias Control Registers
Executing custom PCR setup (channel ON/OFF driven by PCR file & mask)
Loading PCR file /au/pdu/conf/pcr/maxthreshold.pcr for chip # 0 Mask 4294967
95 ....
Loaded specific configuration for 32 channels
Sending test pulse to reset pixel logic
----- End of configuration
eic@epiclab02: /au/rdo/src$
```

Alcor lanes initialization

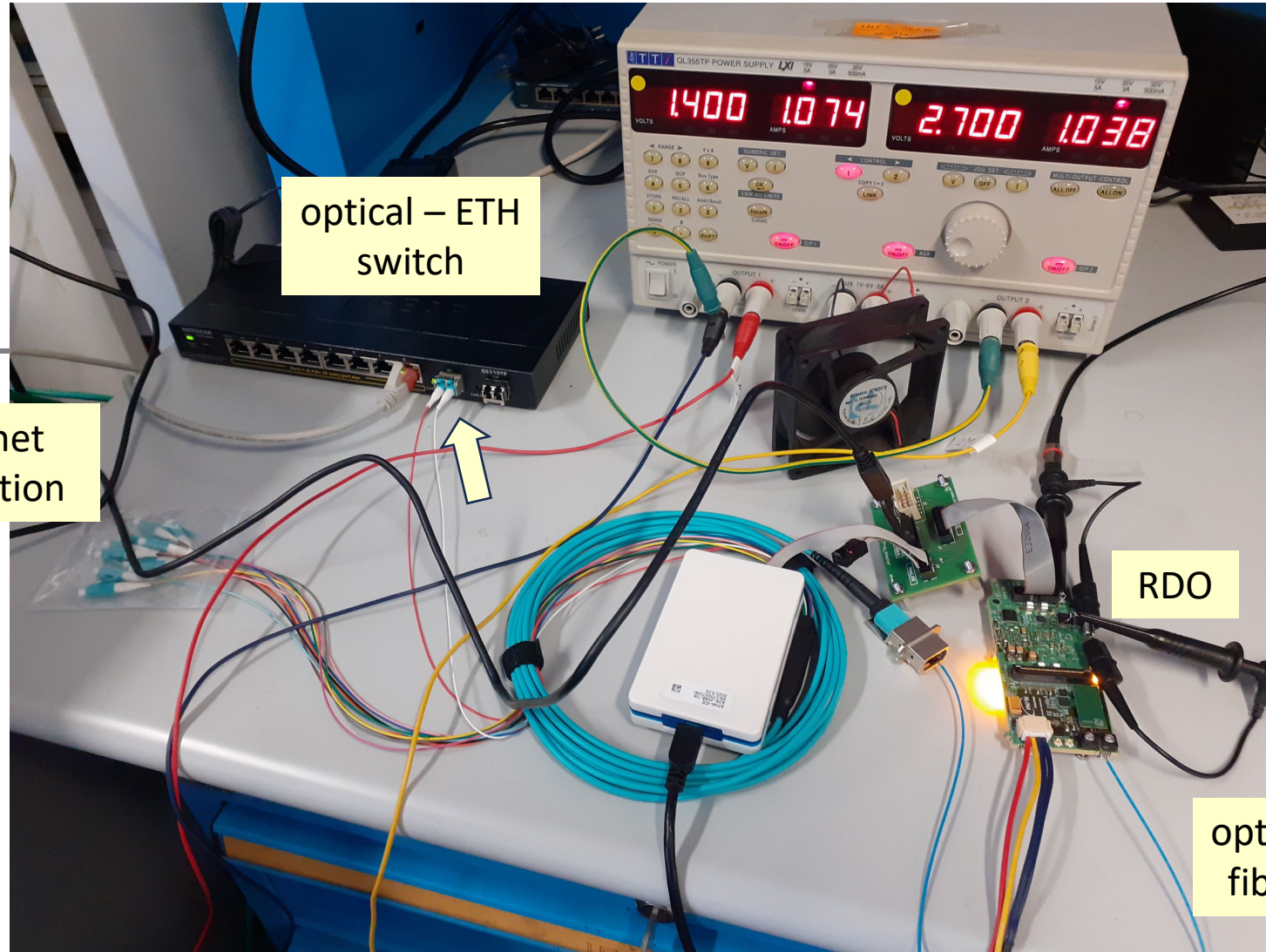
The first RDO setup is mainly devoted to test the communication between the US+ and the Alcor chips

Fetching the IP value from an EEPROM memory on a temperature sensor currently under test

Second RDO setup



Ethernet
connection



optical – ETH
switch

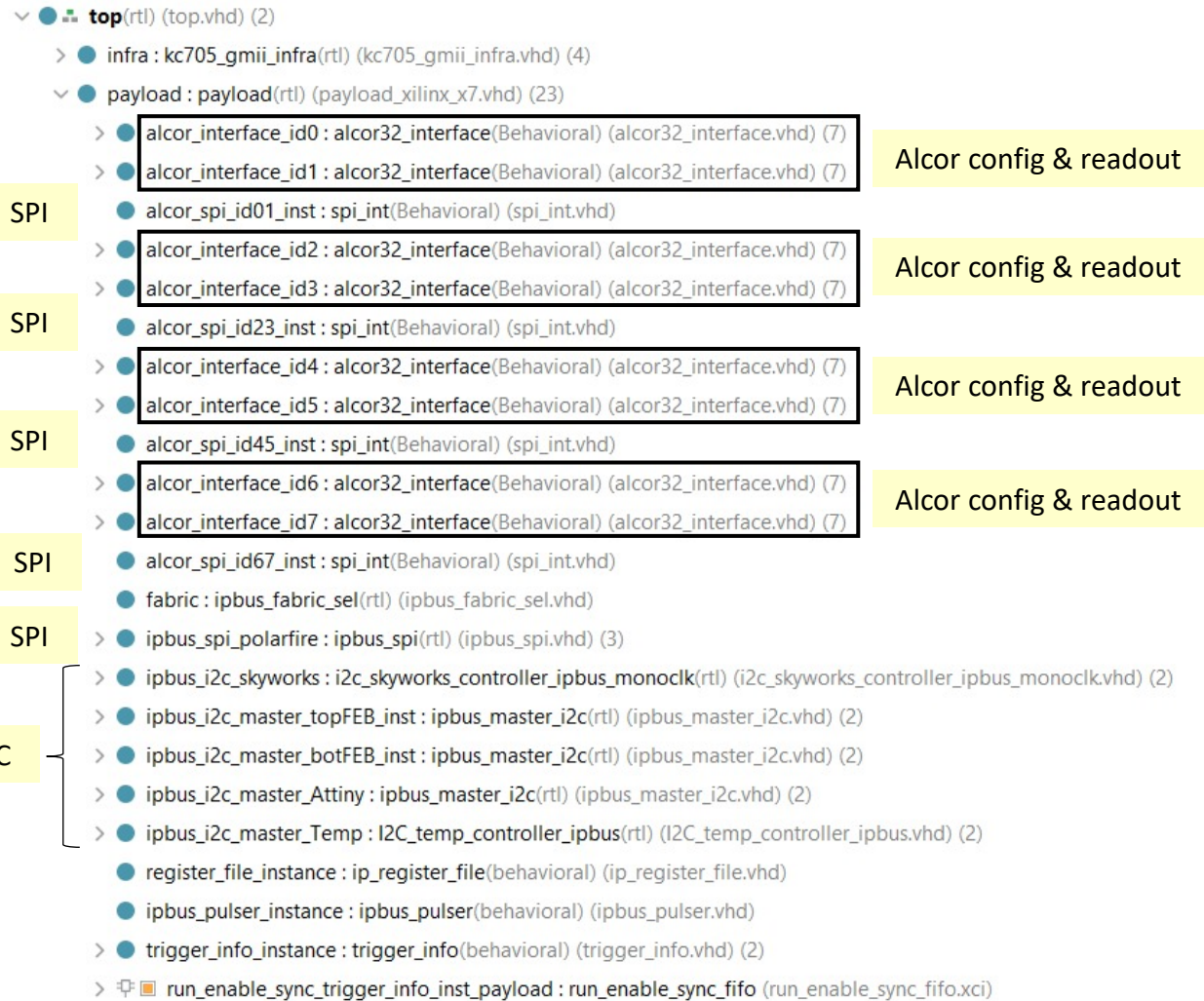
RDO

optical
fiber

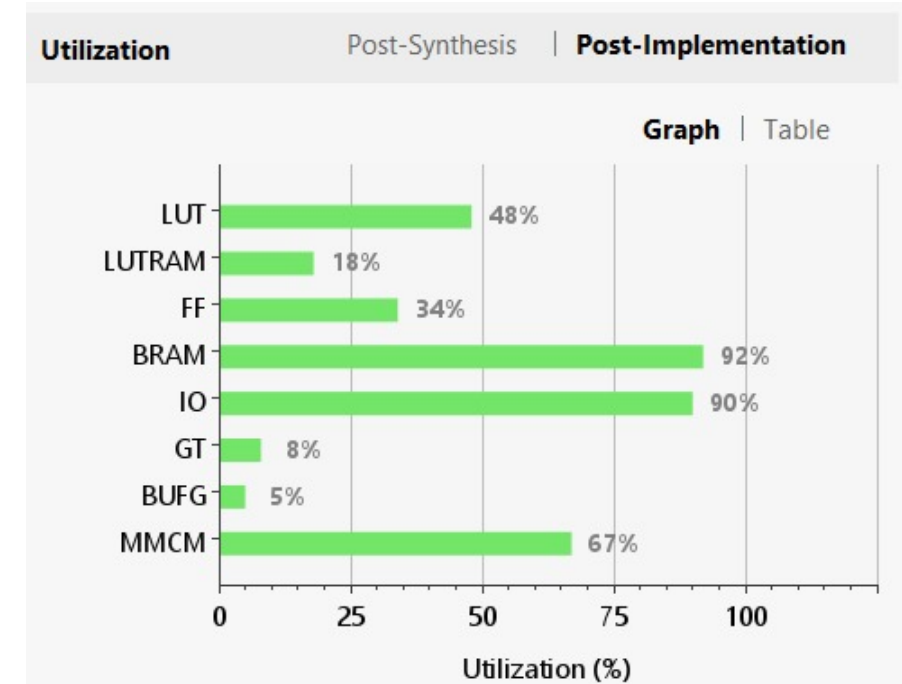
We are currently
using this setup to
test the US+ / ATtiny
I2C communication

Next, we are going to
use it to validate the
data bus between
US+ and Polarfire

Firmware design on the US+ FPGA



design hierarchy



utilization of internal resources

From 2 to 10 RDOs

On 10 September 2025 we gave the green light to the company for the mounting of other **8 RDOs**:
production done → just arrived today (02 October 2025)



10 RDOs

for the November test beam at CERN



Plans

The 10 RDOs will be connected to the Alcor chips and the SiPMs via the Firefly cables.

What is still to be done/tested in preparation for the test beam (**5-19 November 2025**):

- use of external clock (all the 10 RDOs will receive and distribute the same clock)
- provide a different IP to each RDO
- prepare a mini-rack with 10 RDOs
- test the stability of data acquisition with the complete system
- pray !

