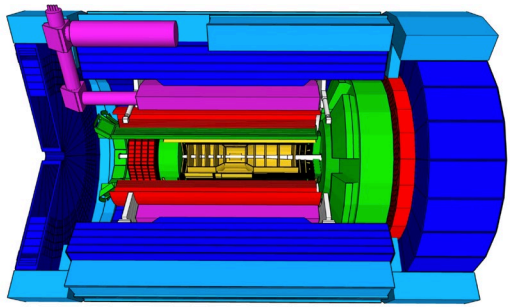


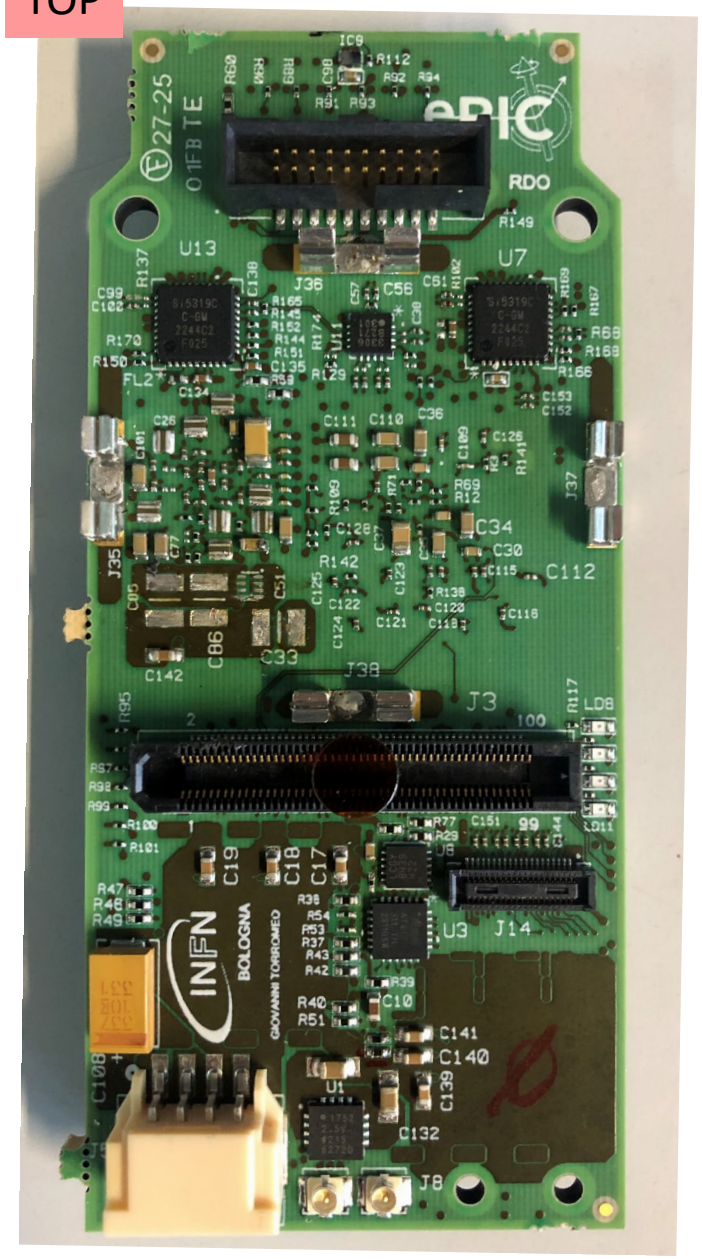
eRD109 update: dRICH RDO

Pietro Antonioli, Davide Falchieri, Sandro Geminiani, Luigi Rignanese, Giovanni Torromeo
on behalf of the INFN Bologna RDO team

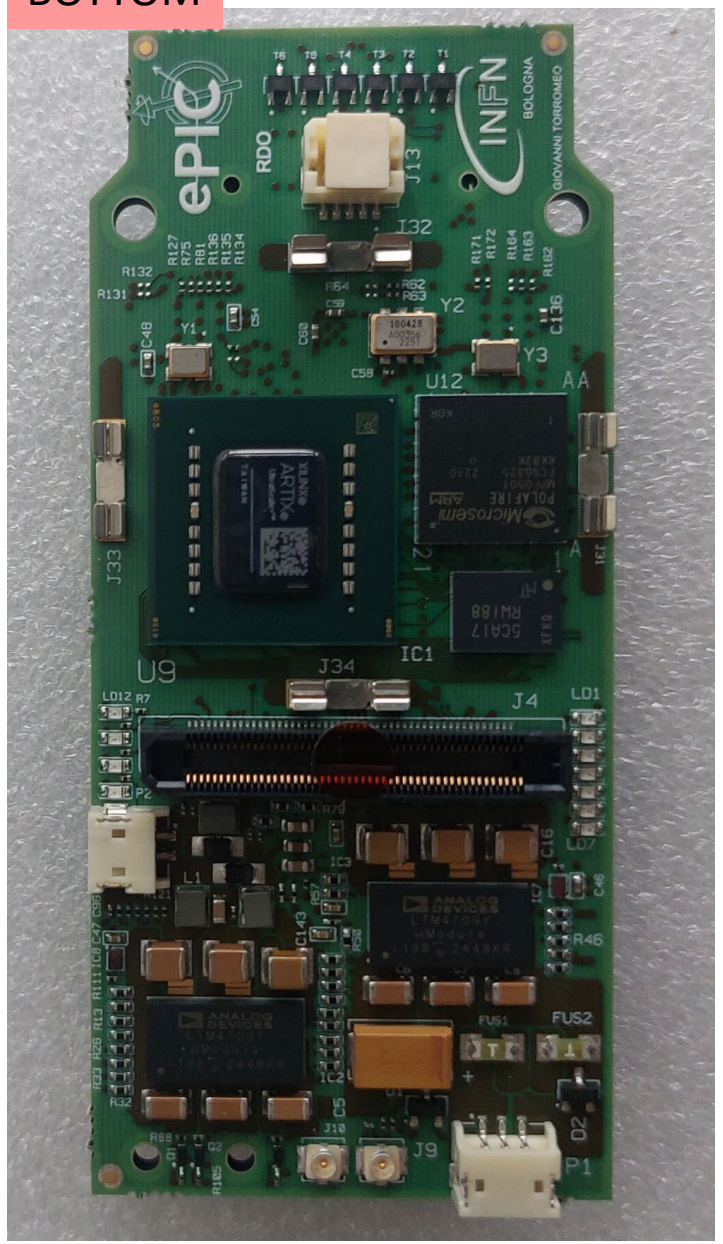
EPIC Electronics & DAQ WG meeting
02 October 2025

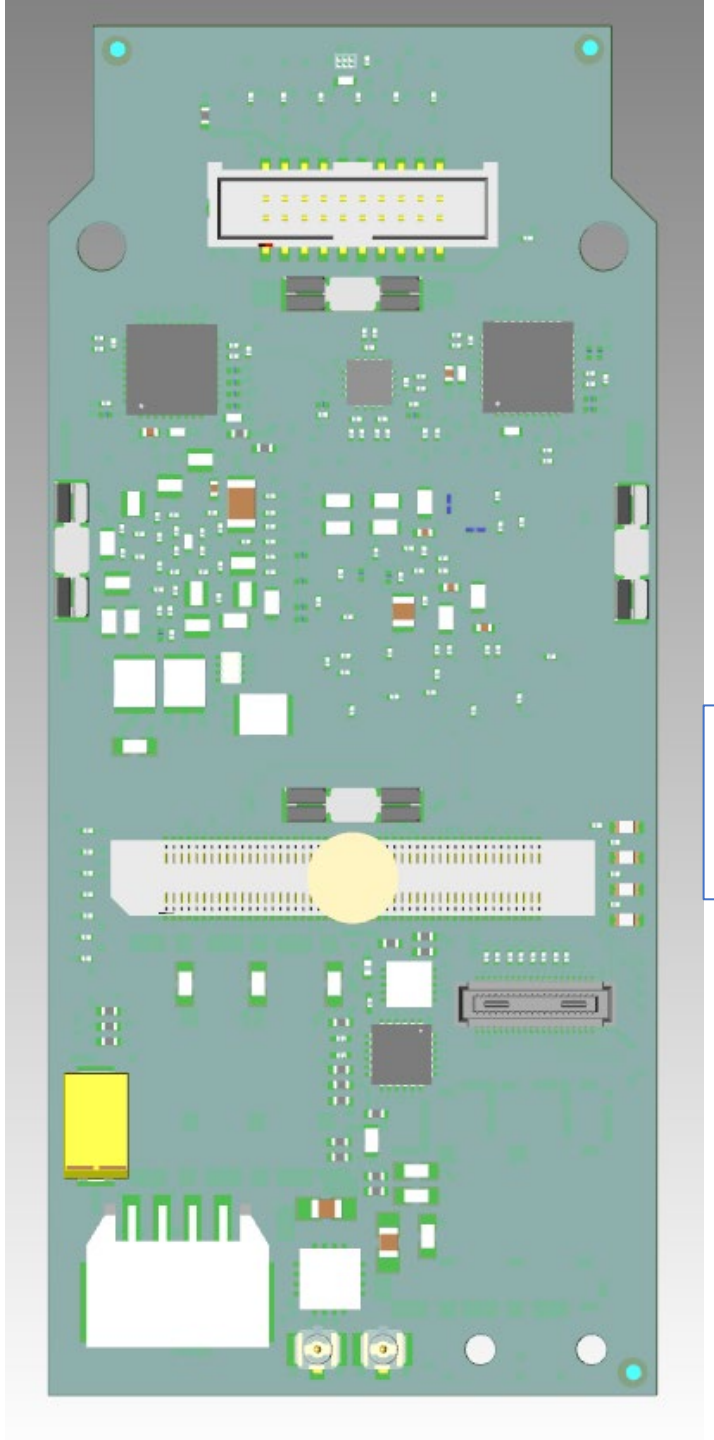
We received 2 complete RDO boards on 24th July 2025

TOP



BOTTOM

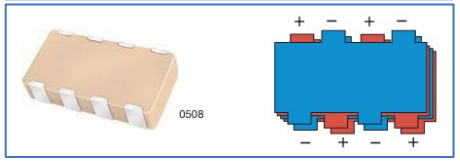




Problems found:

FL1 removed to not power U7

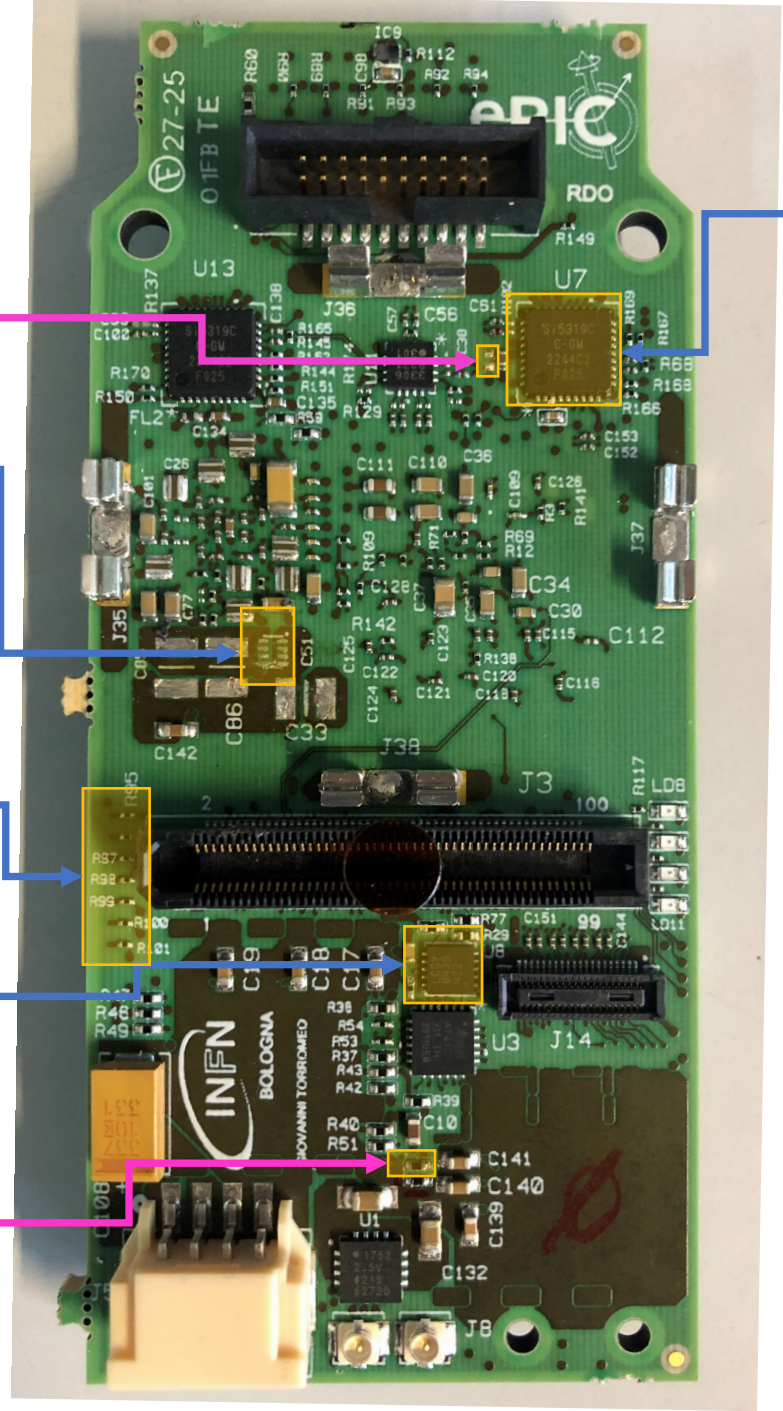
Problem with footprint of **C51**



Changing value of resistors:
R95,R96,R97,R98,R99
R100, R101 from 33 Ω to 330Ω

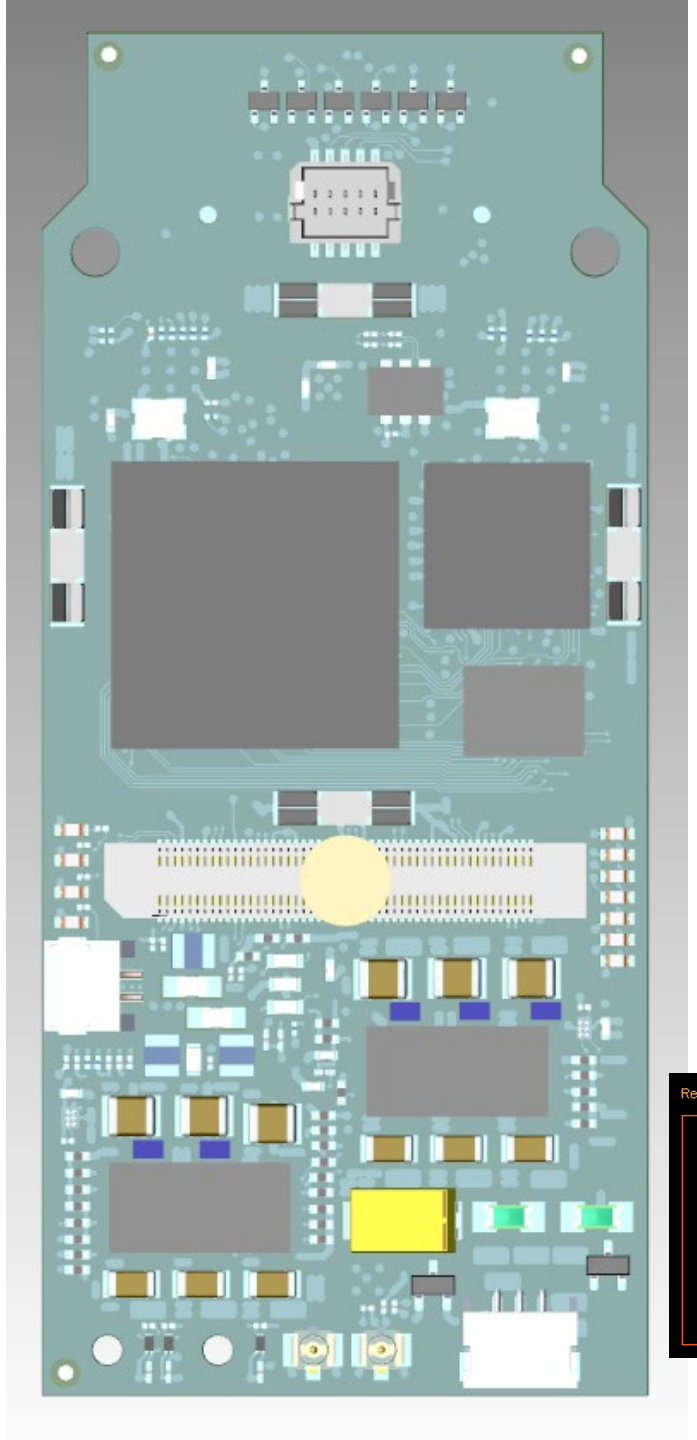
Problem with **U8**
LTC3203BEDD-PBF

R19 1.5K changed to 2.2K Ω to correct VOH level with wrong U8 (charge pump at 5V)

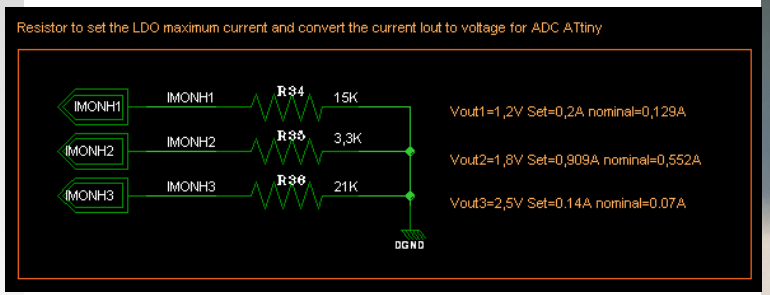


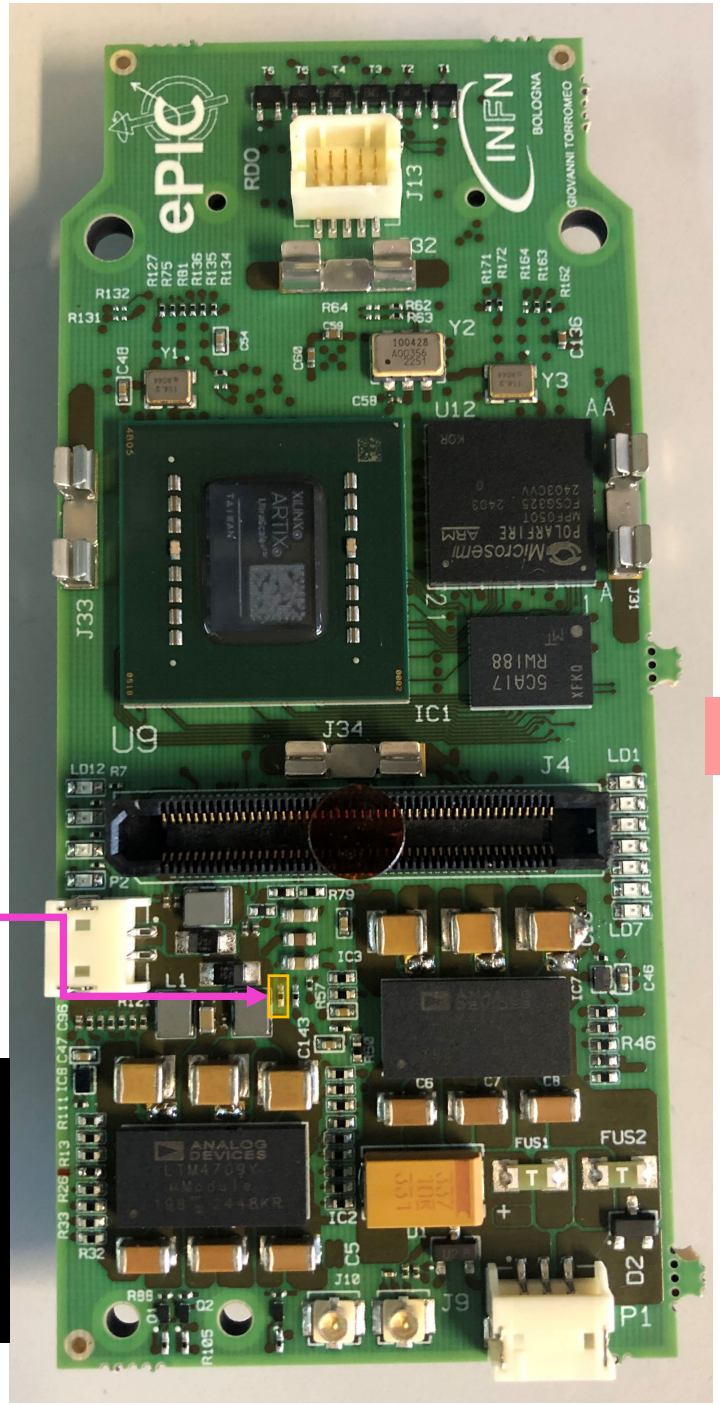
U7
Si5319
instead
Si5326

TOP



R34 15KΩ changed
with 8.2K Ω
to set 1.2V
Iout limit



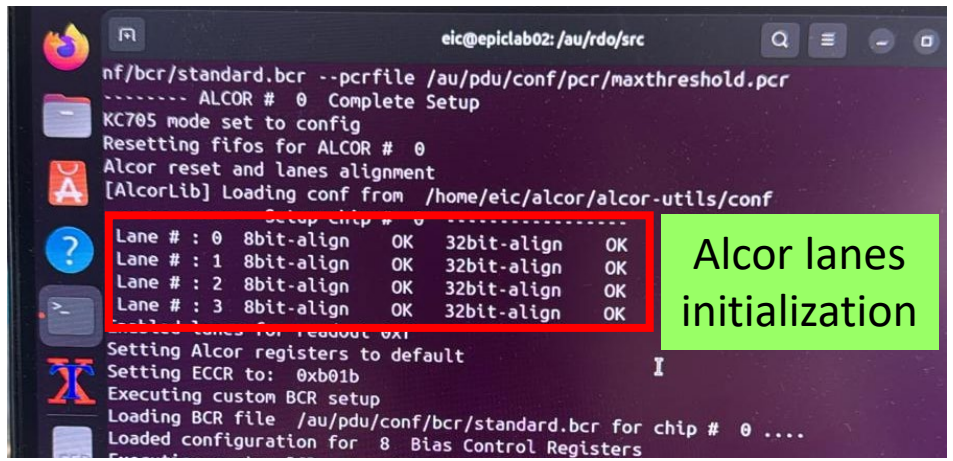


BOTTOM

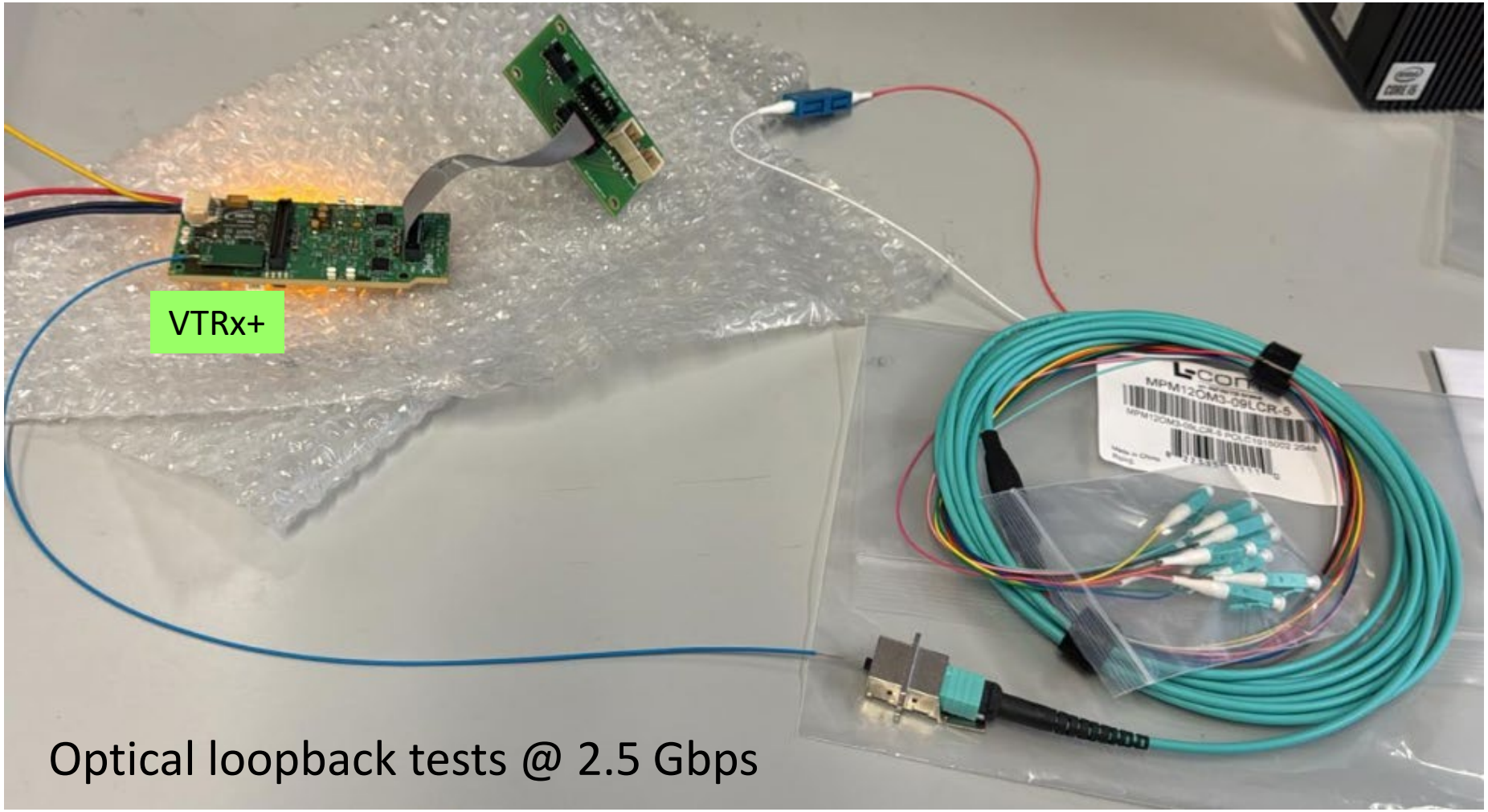
First tests on RDOs

1. mechanical pairing with fake-FEB
2. power-up: 2.5V / 1.4V jumper to avoid power to other sections
3. program μC via external connector
4. power-up with μC (after programming the μC): check LDO Vouts
5. program Artix US+ via external connector
6. program Polarfire via external connector
7. program Artix → SkyWorks (programming 125 MHz of Si5319)
8. check the power consumption
9. check UFL I/Os
10. link IPbus via VTRx+ [MT-MPO adapter + MPO-LC fibers]
11. program ALCOR via fake-FEB (via IPbus → VTRx+)
12. ALCOR readout (via IPbus → VTRx+)

```
  FEB # 0 TOP Master OK
  FEB # 1 TOP Slave OK
  FEB # 2 BOTTOM Master NOT REACHABLE
  FEB # 3 BOTTOM Slave NOT REACHABLE
--------- FEB # 0 ALCOR32 chip # 0 Complete Setup
RDO mode set to config
ECCR   : 0xB01B 0xB01B 0xB01B 0xB01B
BCR    : 0x003D 0xC72C 0x003D 0xC72C 0x003D 0xC72C 0x003D 0xC72C
Ch. 00: 0x7777 0x8888 0xFFFF 0x0202
Ch. 01: 0x7777 0x8888 0xFFFF 0x0202
Ch. 02: 0x7777 0x8888 0xFFFF 0x0202
```



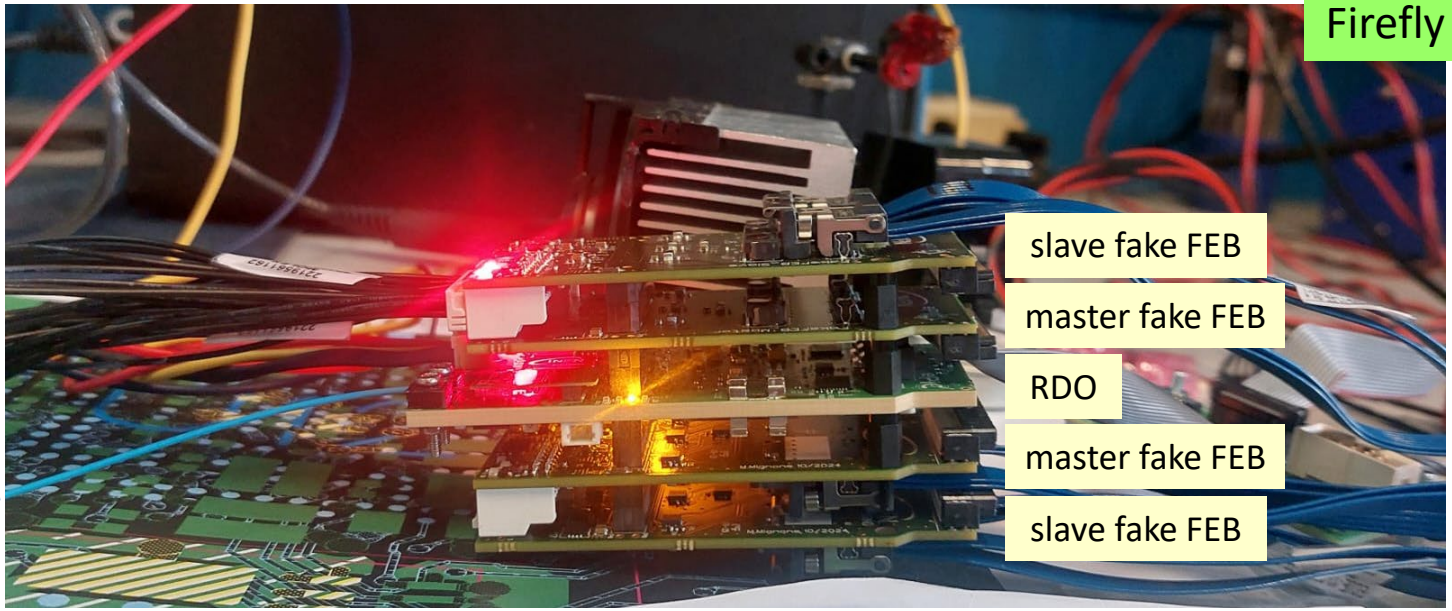
US+ - VTRx+ validation tests



We used the IBERT core on the US+ firmware to test the FPGA-VTRx+ devices on loopback mode @ 2.5 Gbps: no errors found

First RDO setup

RDO with
2 master fake FEBs
+ 2 slave fake FEBs

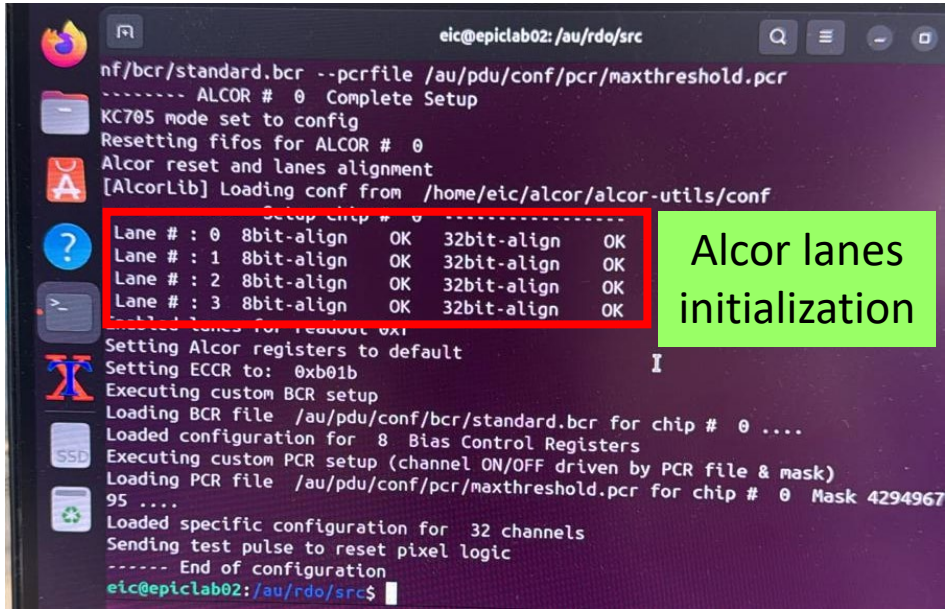


FEBs

4 dual FEBs each with
2 32ch Alcor chips

optical fiber

NIC card



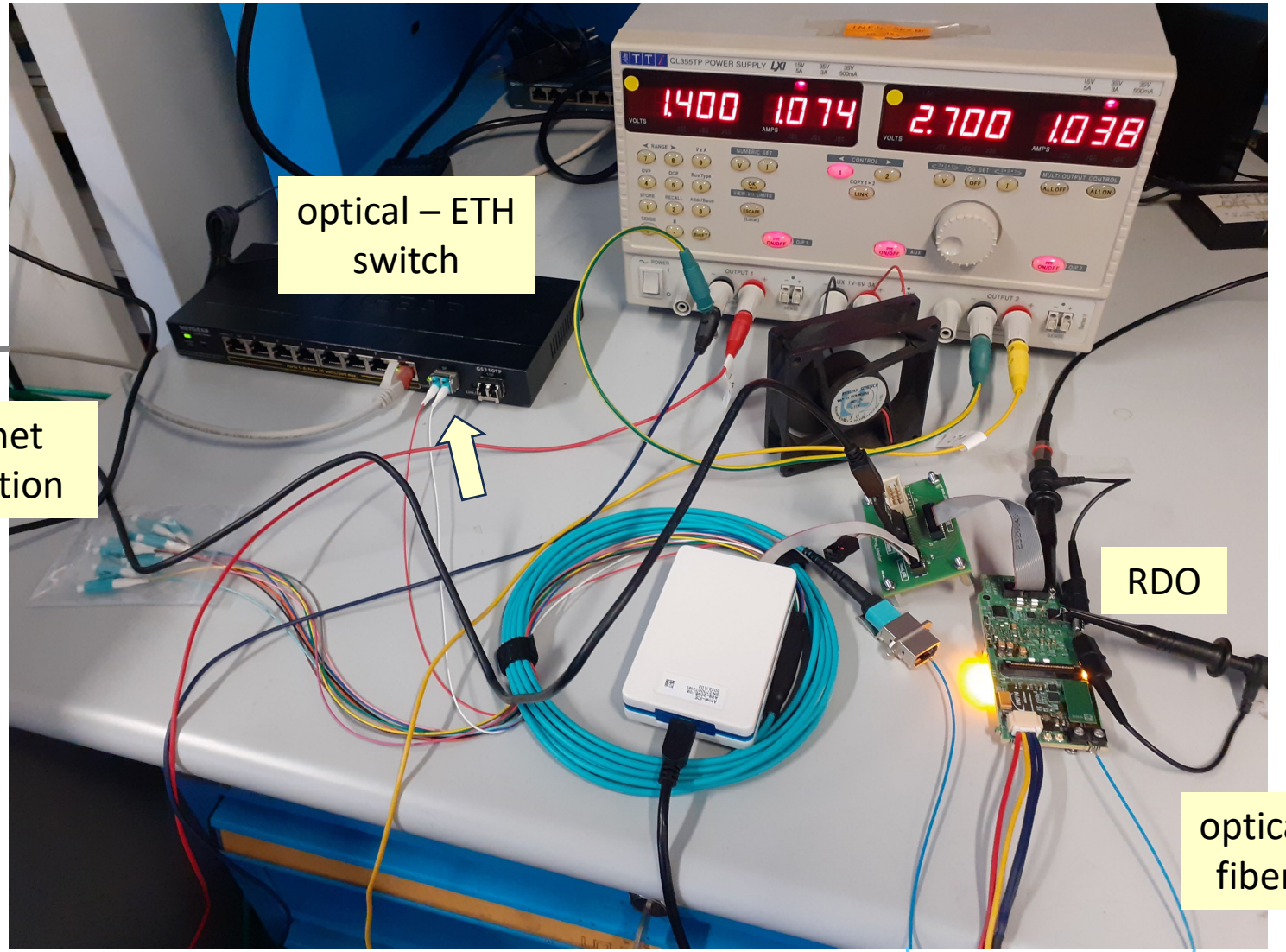
Alcor lanes initialization

The first RDO setup is mainly devoted to test the communication between the US+ and the Alcor chips

Fetching the IP value from an EEPROM memory on a temperature sensor currently under test

Second RDO setup

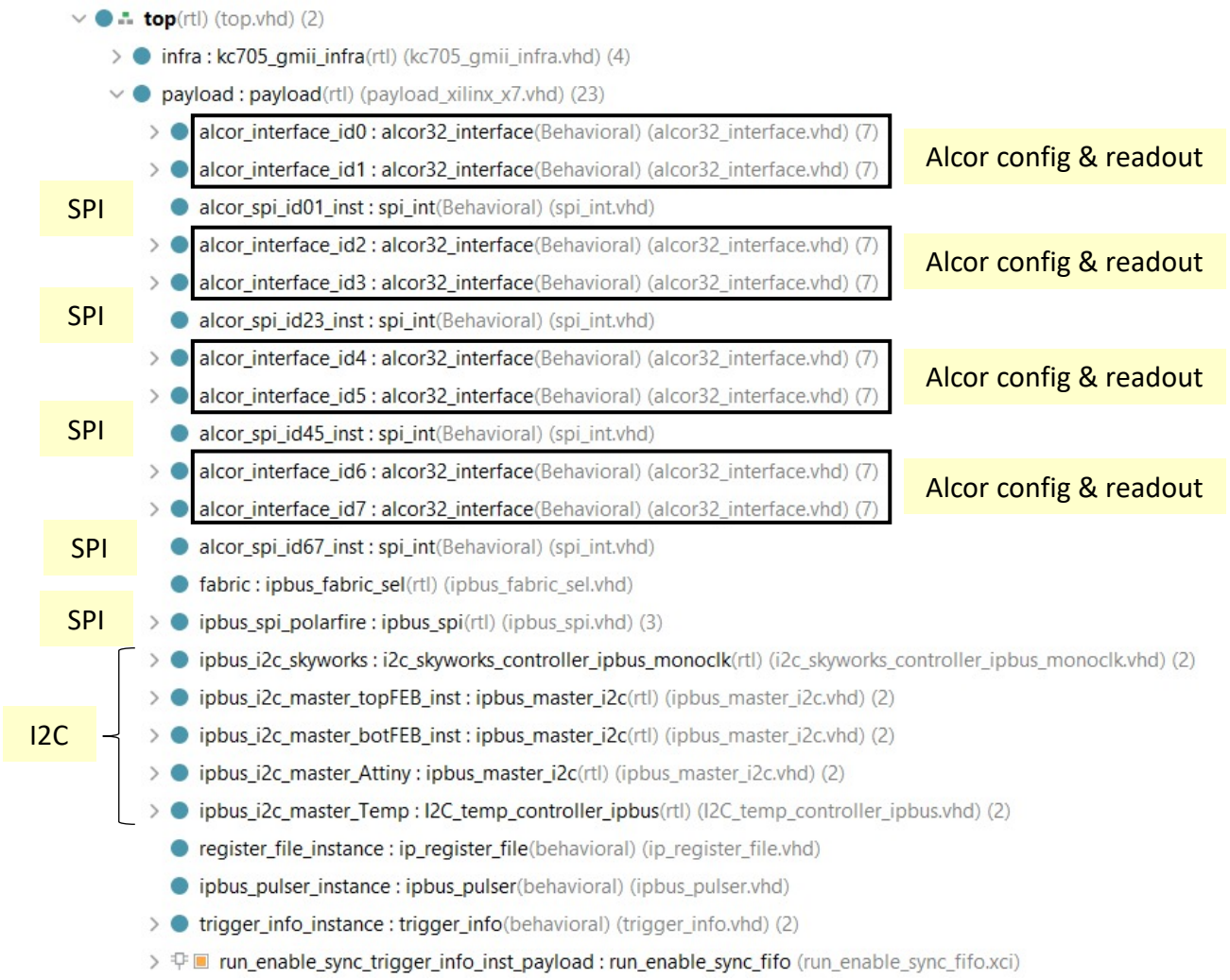
Ethernet connection



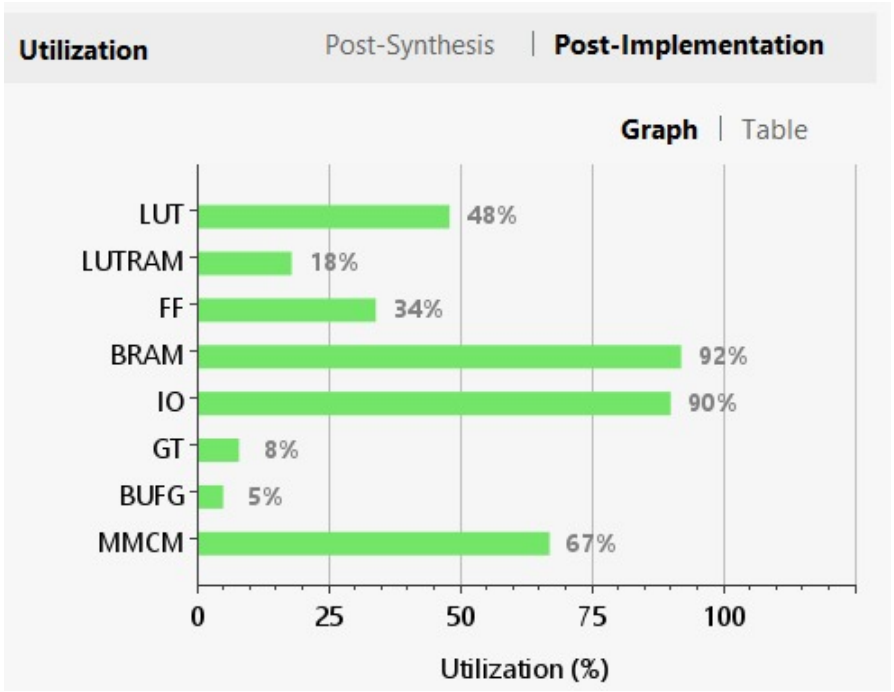
We are currently using this setup to test the US+ / ATtiny I2C communication

Next, we are going to use it to validate the data bus between US+ and Polarfire

Firmware design on the US+ FPGA



design hierarchy

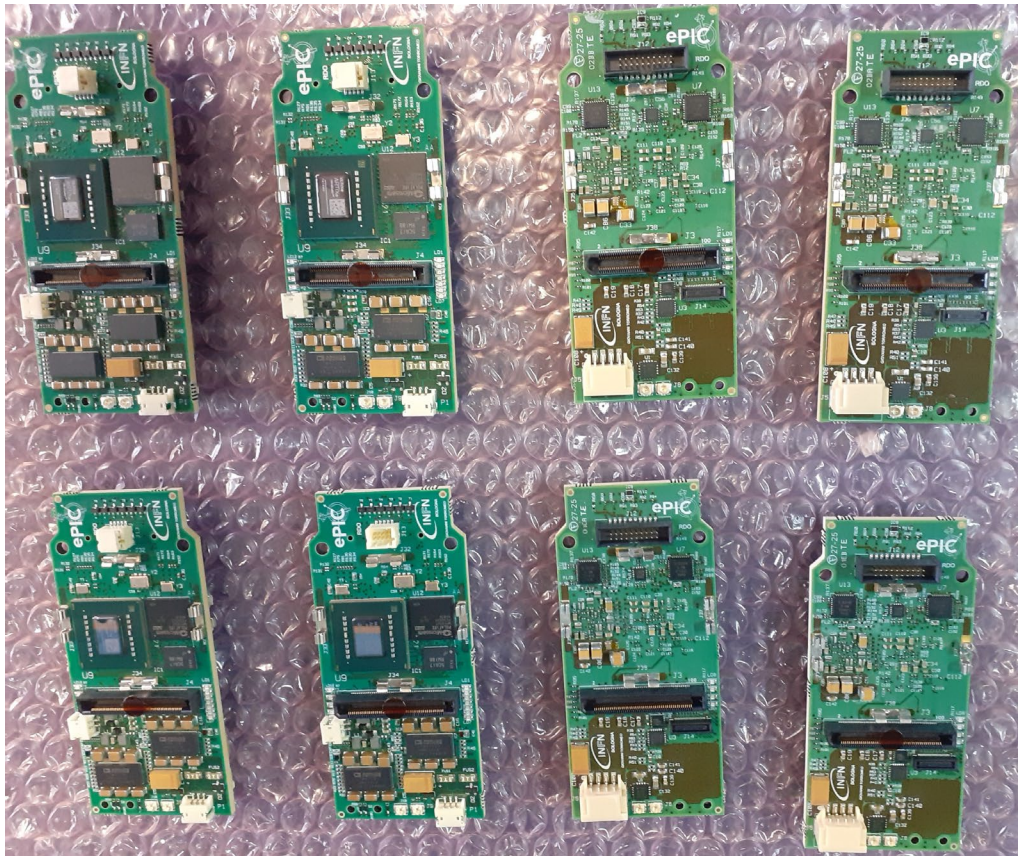


utilization of internal resources

From 2 to 10 RDOs

On 10 September 2025 we gave the green light to the company for the mounting of other **8 RDOs**: production done ➔ just arrived today (02 October 2025)

10 RDOs for the November test beam at CERN

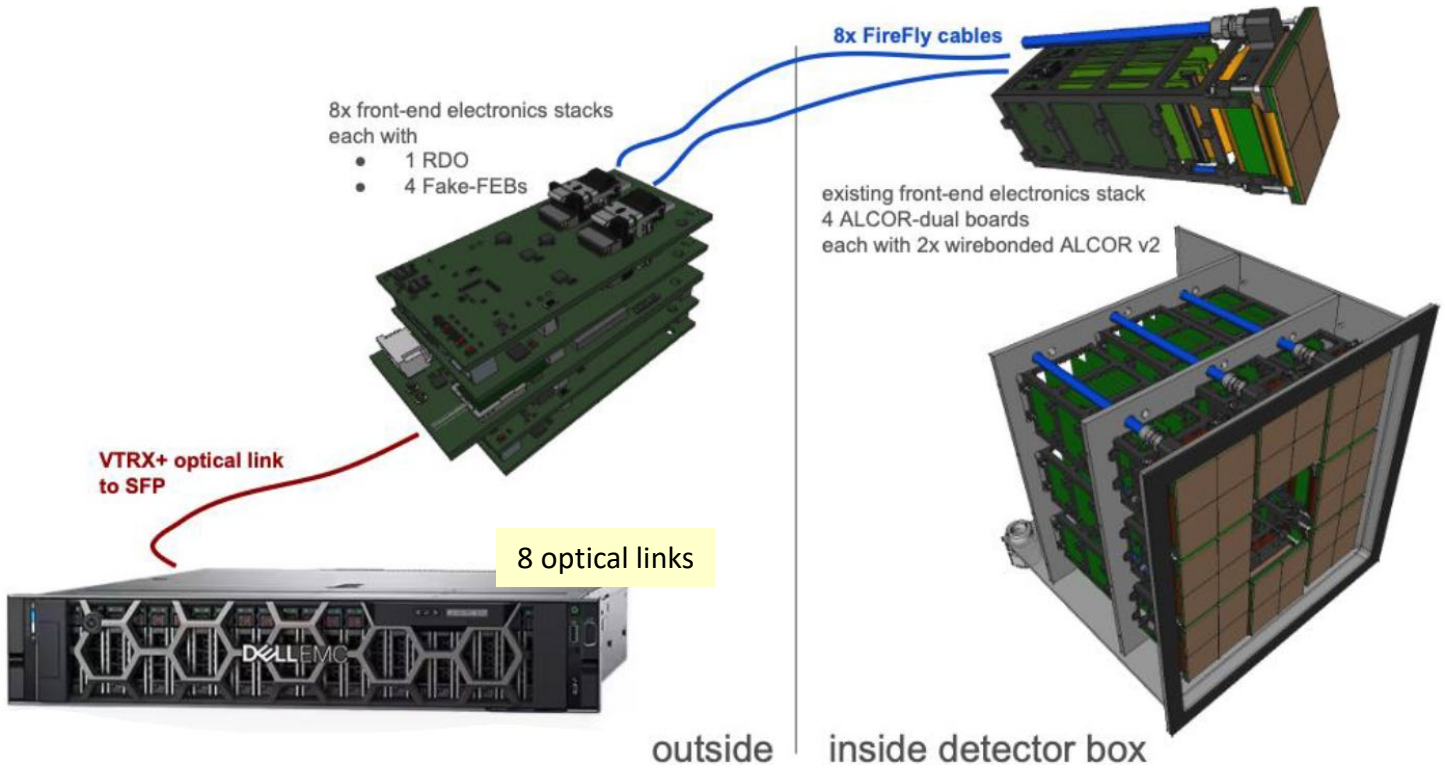


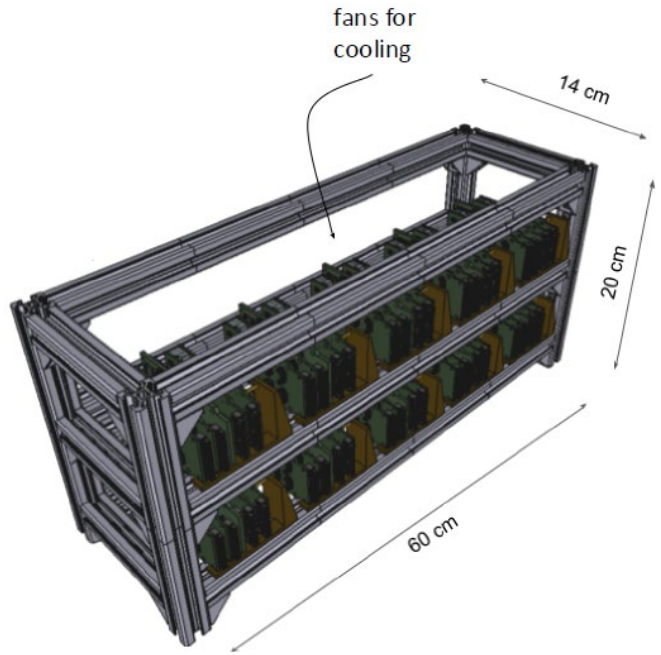
Plans

The 10 RDOs will be connected to the Alcor chips and the SiPMs via the Firefly cables.

What is still to be done/tested in preparation for the test beam (**5-19 November 2025**):

- use of external clock (all the 10 RDOs will receive and distribute the same clock)
- provide a different IP to each RDO
- prepare a mini-rack with 10 RDOs
- test the stability of data acquisition with the complete system
- pray !





rack for hosting RDOs + fake FEBs