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Status report of the eRD109 project on SALSA chip development

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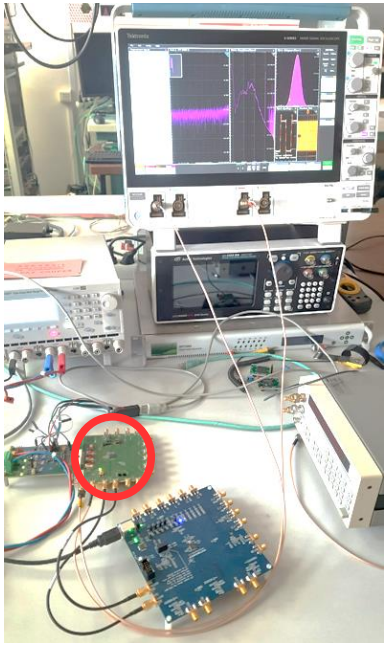
EPIC DAQ/electronics WG meeting

2/10/2025

STATUS OF THE PROTOTYPES: PRISMEV1

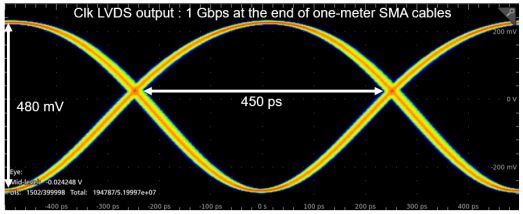
PRISMEv1 prototype (PLL test chip)

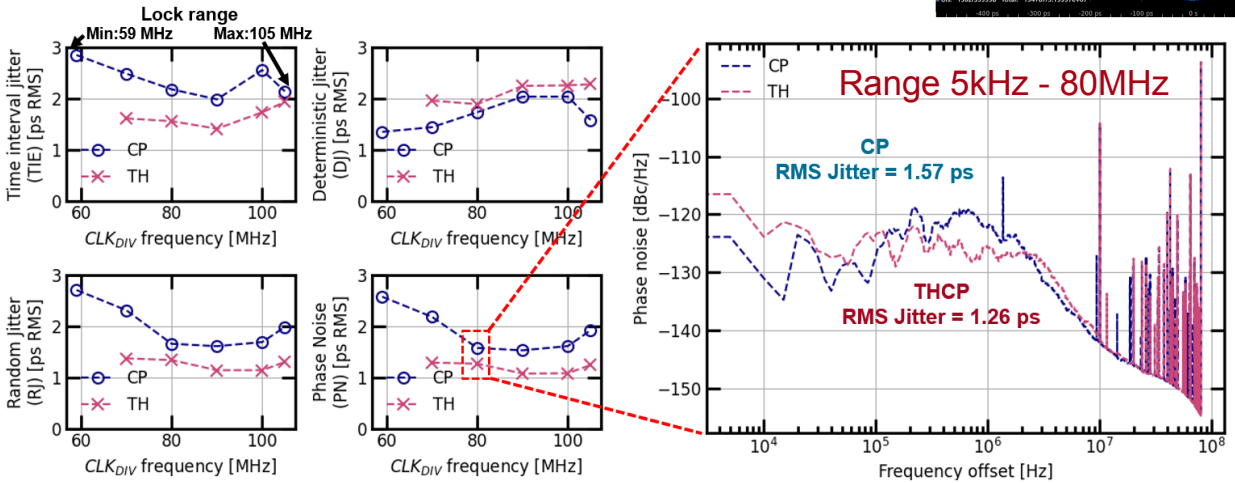
- Updates done on the PLL block since original PRISME prototype: improved deterministic jitter noise, radiation hardness, lower internal frequency, inclusion of CDR for unified input interface, compatibility with lpGBT input frequency
- 2 modes: charge pump (CP) and track and hold charge pump (THCP)
- Tests ongoing since July

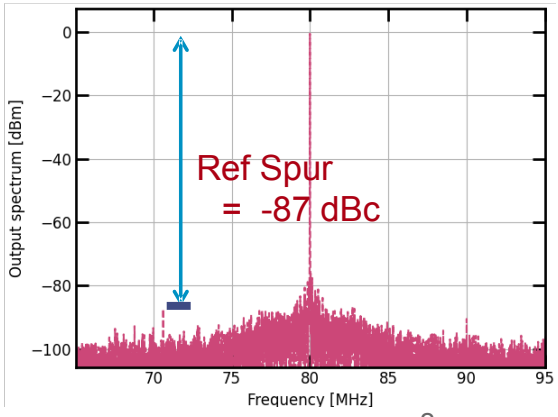


Results

- Noise performance in range 5 kHz – VCO/20 (VCO in range 1.18-2.1 GHz)
- Lock range 59 – 105 MHz
- THCP allow 20% noise reduction
- Gigabit LVDS output with wide eye diagram



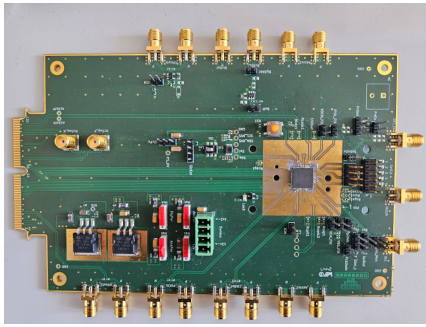


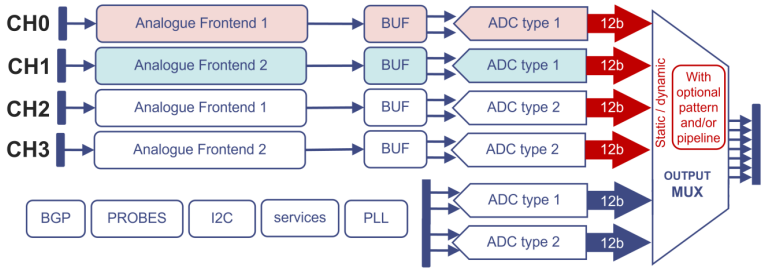


STATUS OF THE PROTOTYPES: SALSA1

SALSA1 prototype

- Tested since mid-December 2024, new test-cards with SALSA1 soldered on them instead of socket since July, systematic measurements ongoing
- 2 kinds of front-ends, how to choose the final one ?
  - SALSA0 like → CH0
  - Updated pole-zero cancellation (PZC) + CSA R_f → CH1
- Measurements done on CH0 and CH1: gain, noise, PZC perf, saturation, crosstalk, hit rate; several ASICs tested
- Internal PLL deactivated due to jitter → external 800MHz clock
- To do next: temperature, TID
- Posters at TWEPP conference



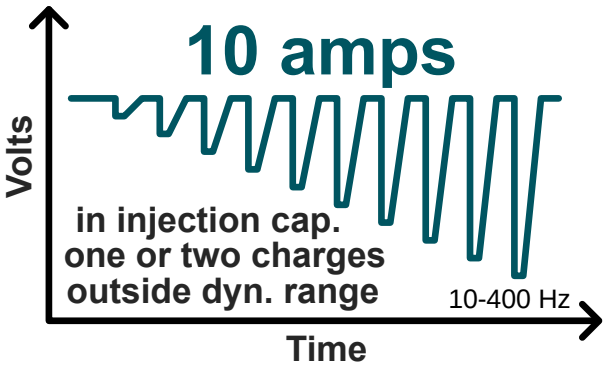


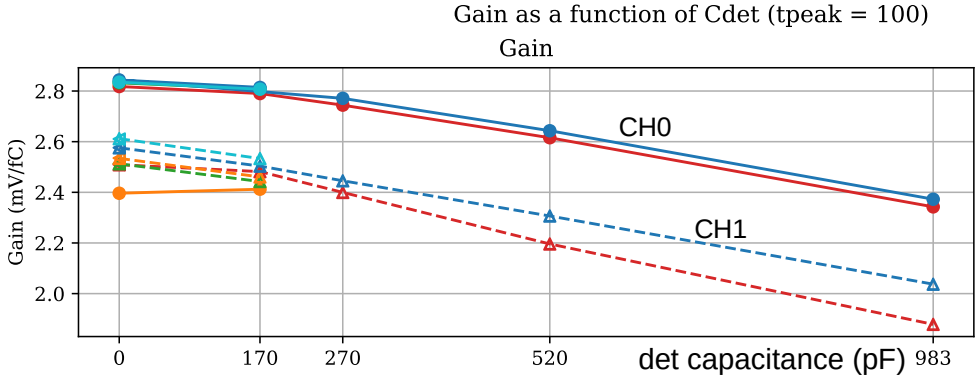
Difference between 2 front-ends

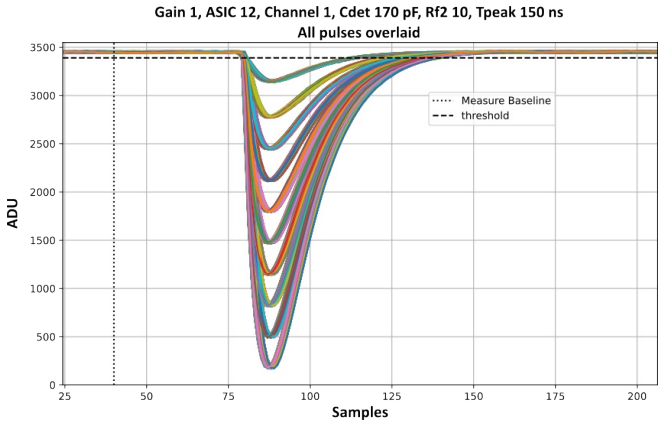
STATUS OF THE PROTOTYPES: SALSA1

Gain measurements

- Step signals injected through 5pF capacitor, with slow return slope to zero
- 10 different amplitudes covering 120% dynamic range
- Good linearity, with residual < 20 ADC
- But return slope tends to perturb next signal if rate too large

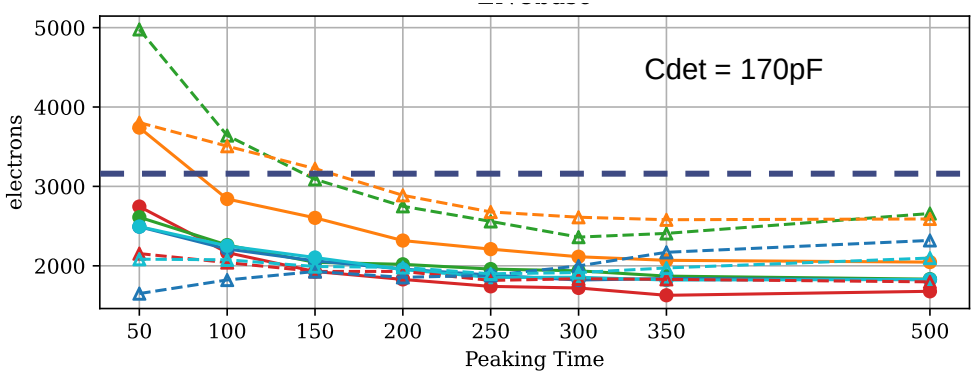




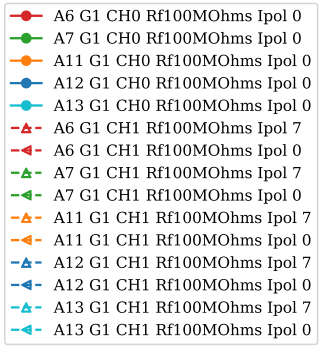


Noise measurements

- ENC vs peaking time, < 0.5fC for most of t_{peak} and ASICs



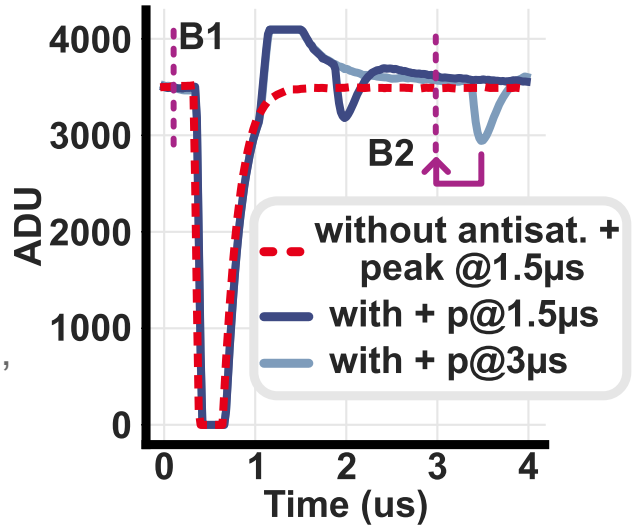
0.5 fC



STATUS OF THE PROTOTYPES: SALSA1

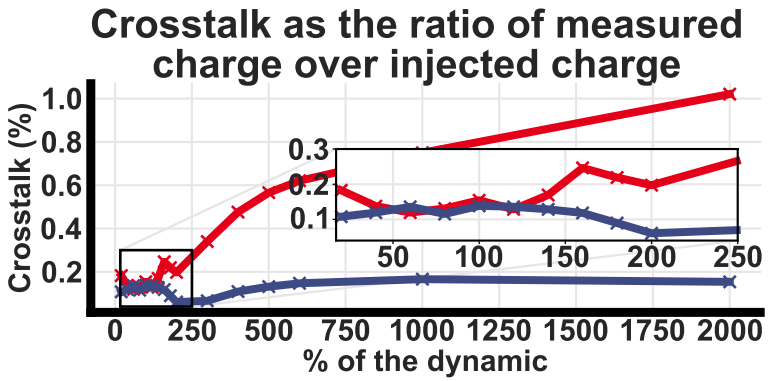
Saturation measurements

- Signal sent after 50pC saturating charge
- Without anti-saturation no detection during > 12µs
- With anti-saturation, signal can be measured even at 1.5µs
- Baseline instabilities for CH0, no such problem with CH1



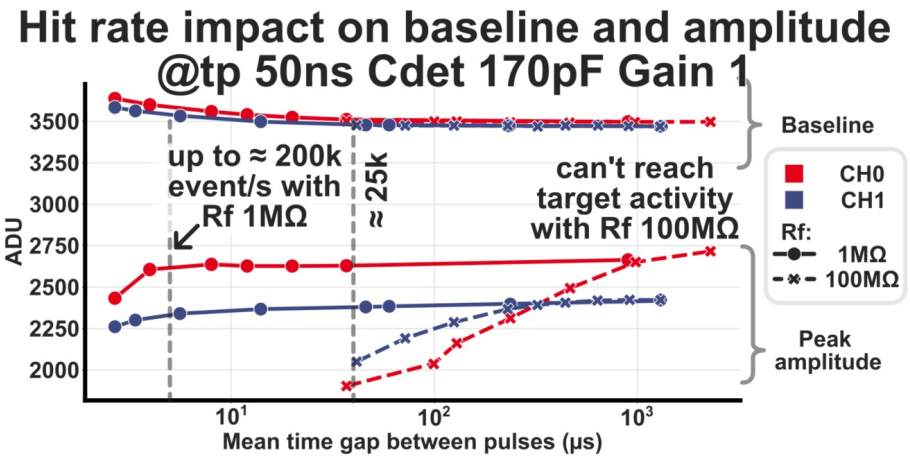
Cross-talk measurements

- Impact of signal injected in CH1 (then CH3) to CH0, below 1%, and even 0.5% in dynamic range



Hit rate impact

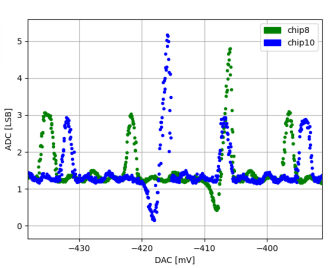
- Injection with laser + photodiode (no ret. sig)
- Random signals with mean time between pulse 1-100µs
- Can reach 200kev/s with no mean amp. drop with CSA in fast mode (R_f = 1MΩ)

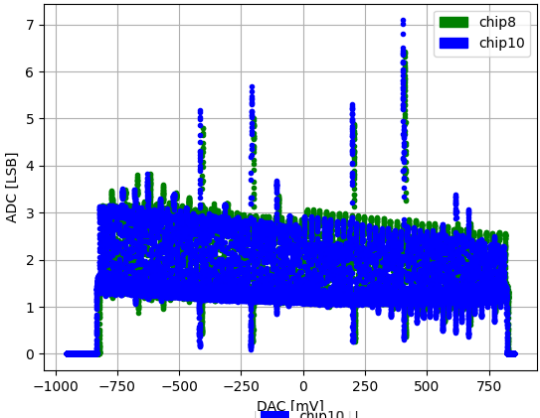


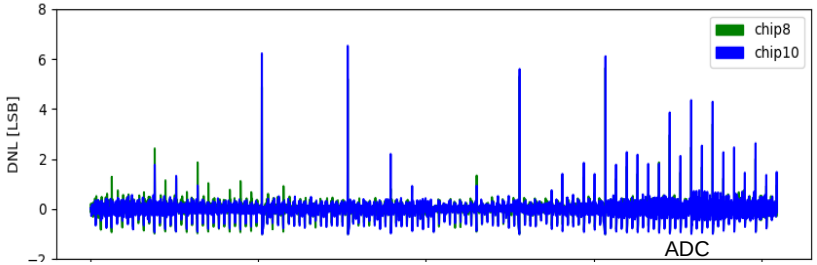
STATUS OF THE PROTOTYPES: SALSA1

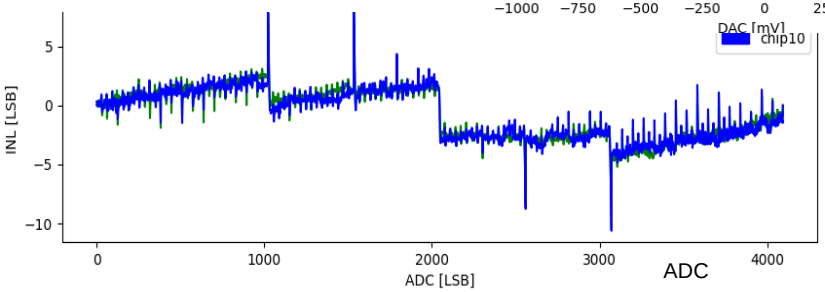
ADC measurements

- Tests done on Sao Paulo ADC of 2 ASICs
- 800MHz external clock to avoid internal PLL noise
- Input range 1.6Vpp differential
- Noise with static input voltage at 1.3 LSB, but peaks at 3 (mod 32) and 7 LSB (mod 512)
- DNL > -0.17 LSB, INL > -10/8.5 LSB



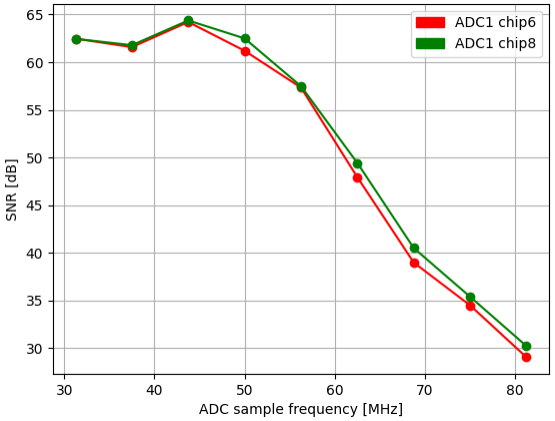


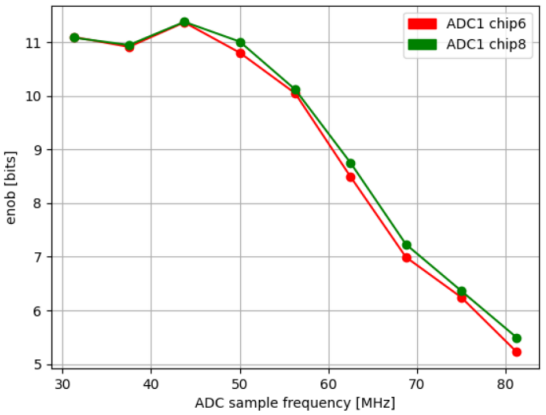




Study with different sampling rates

- 10MHz sinusoidal to ADC input
- SNR and ENOB drop above 50MS/s





Conclusions

- Some DNL imperfections
- Performance consistent bw ASICs
- Performance worsen above 50MS/s
- Results to be confirmed by studies at USP

CURRENT STATUS: SALSA2

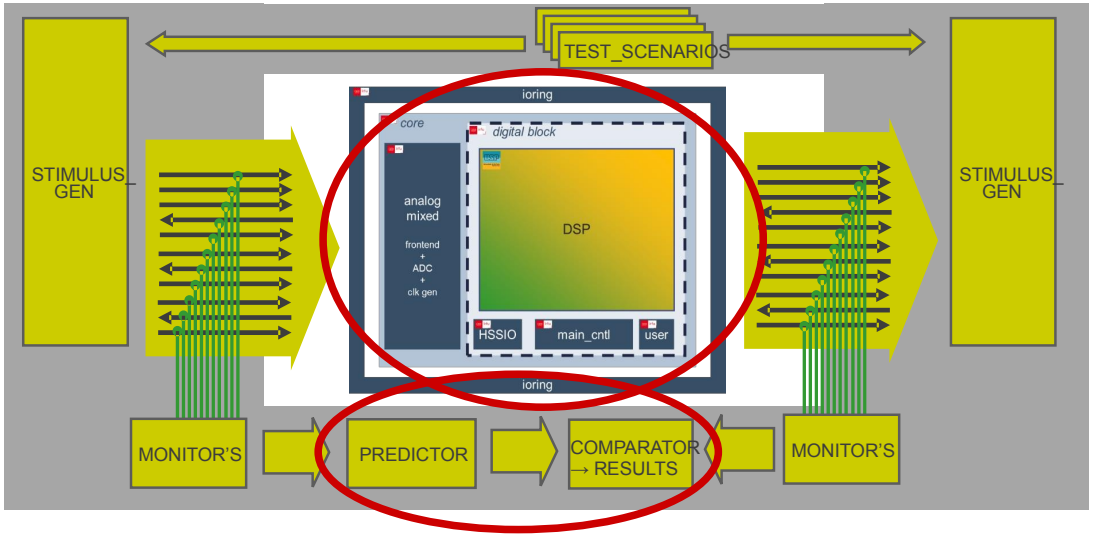
SALSA2 development status

- Development of RTL code mostly done, work ongoing and preparation for integration
- Work on clock generator box (adaptation to change of frequencies in PLL) and its synchronization
- DSP integration into rest of digital block ongoing, done for multiplexer and packetizer
- Also work ongoing on digital test-bench and UVM environment, in order to play data in DSP and compare with golden model
- Definition of floor plan in progress, idem for slow-control registers

Timeline

- Still a lot of works ahead:
  - code verification and validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen beginning of 2026
- Tests end of 2026
- Distribution to users beginning 2027

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done
- Test card production → done
- Performance evaluation of SALSA1 → finishing

Generic R&D program for EIC project (new 65nm PLL block)

- Fully done, follow-up with PRISMEv1 new prototype (not financed by this program)

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming beginning of 2026
- Beginning of SALSA2 tests → 2nd semester 2026

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming December 2025, probably 1st semester 2026
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

Very next steps

- SALSA1 tests → temperature, TID tests in November
- New PRISMEv1 chip → tests ongoing, TID tests in November
- SALSA2 development → in progress