



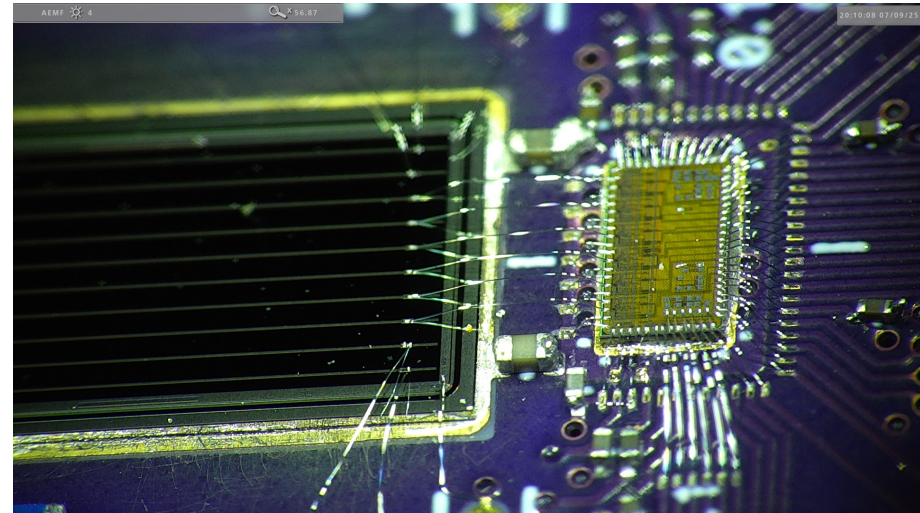
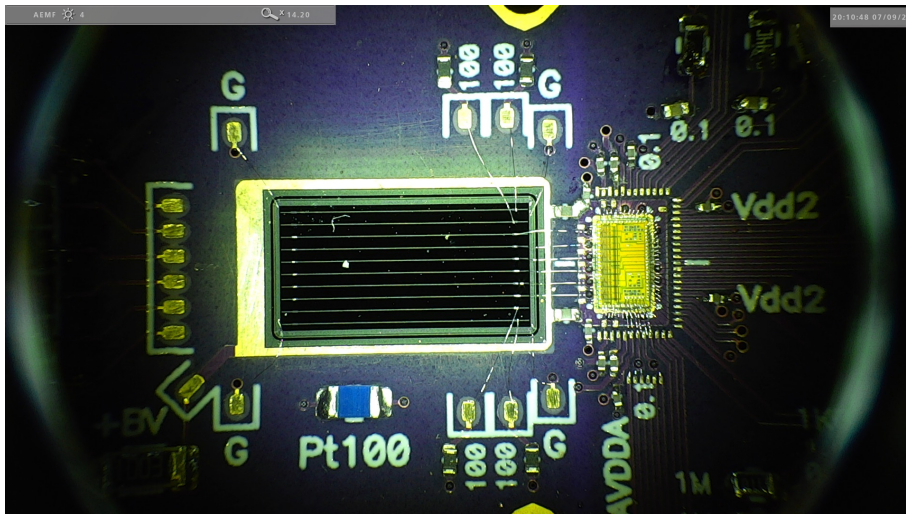
FCFD status

Artur Apresyan

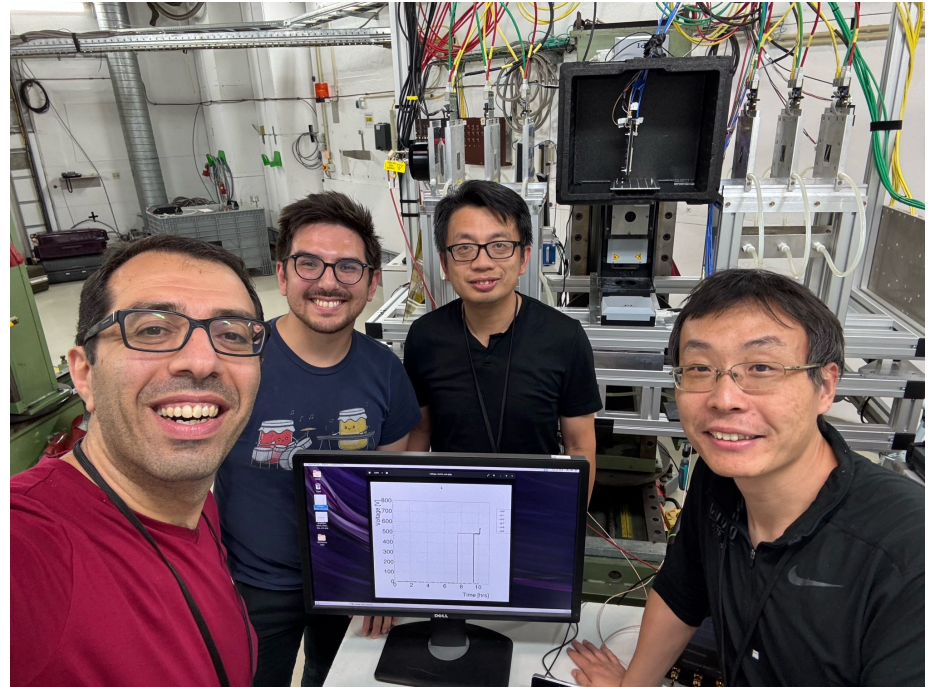
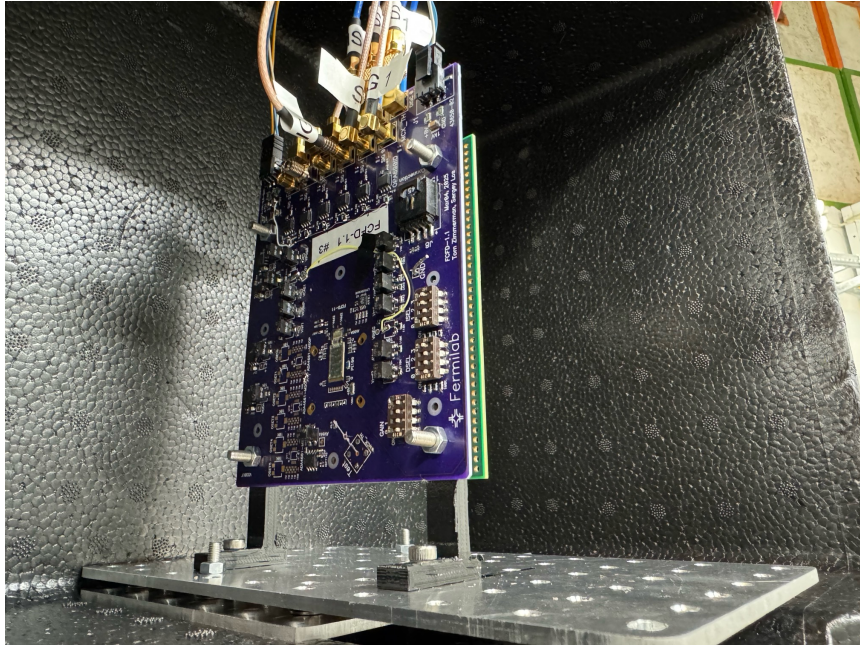
*EPIC Electronics & DAQ WG meeting : eRD109 Monthly Progress Reports
Oct 2, 2025*

FCFDv1.1 testing status

- Chip was received in Fermilab in early June.
- Mounted on testing board and testing started immediately
 - Wirebonded to a HPK 1-cm strip sensors, 6 strips connected
 - Sensor specs as we agreed in the previous presentations
- Test-beam campaign in DESY and CERN in Summer 2025

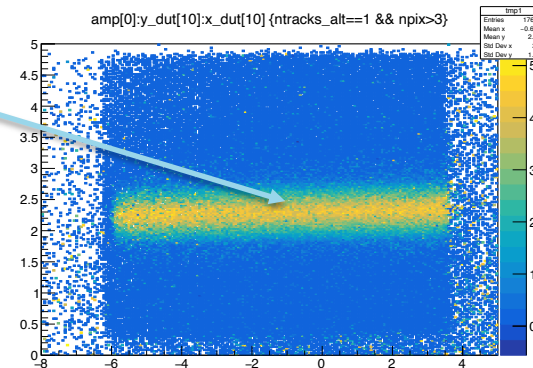
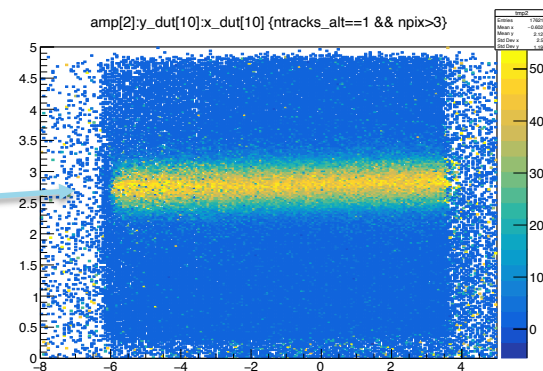
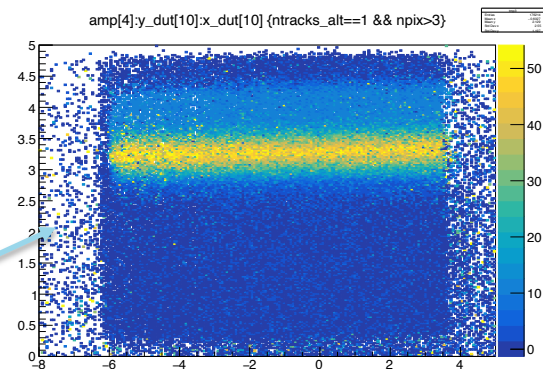
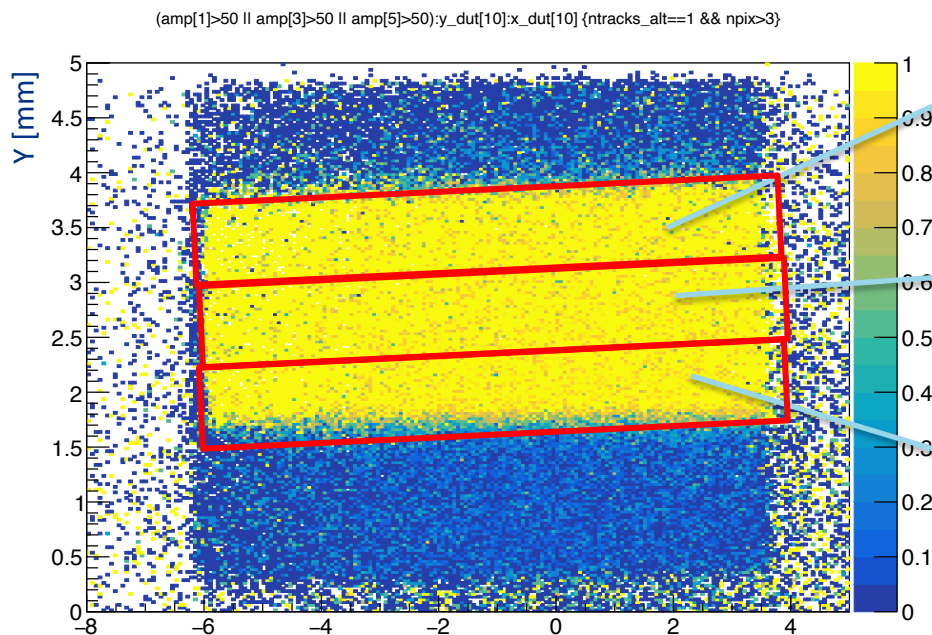


Test beam campaigns in DESY and CERN



Test beam measurements with FCFD1.1

- Demonstrated 100% detection efficiency with particle beams
- Readout is fully analog for this prototype
 - All channels fully functional, perform as expected

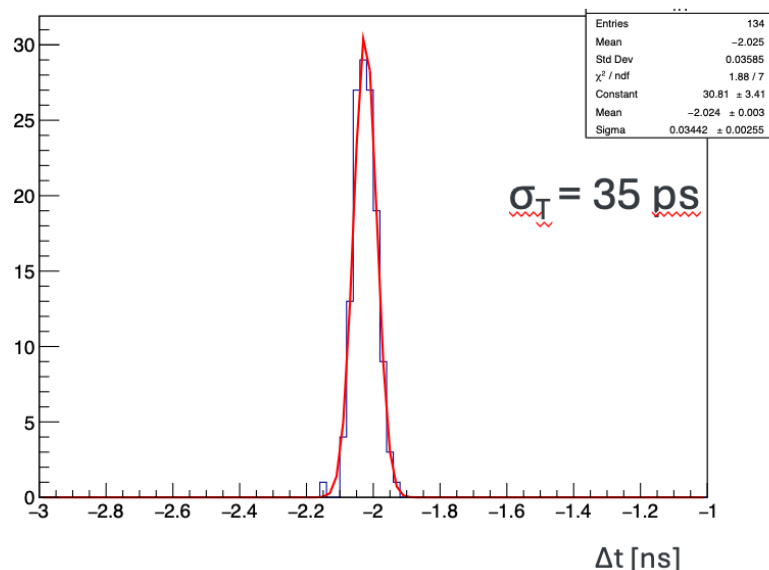


100% detection efficiency across 3 channels

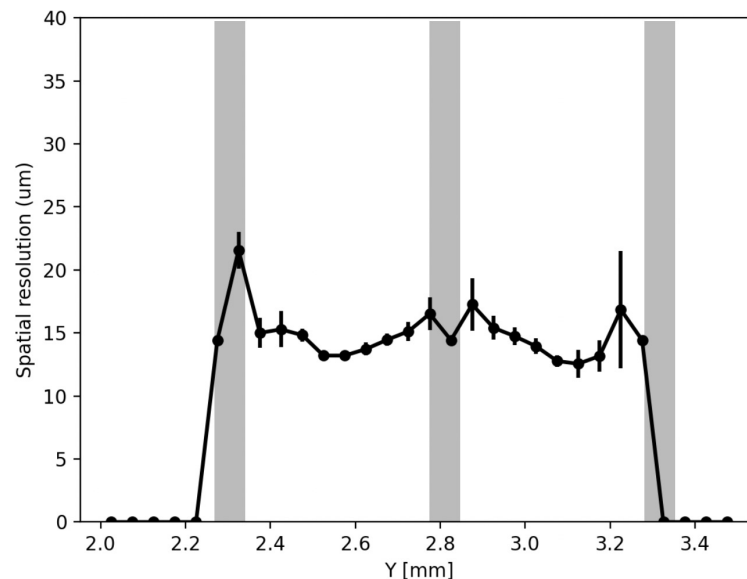
Test beam measurements with FCFD1.1

- Time resolution demonstrated to be within specifications
 - Measured **time resolution ~40 ps** across sensor surface
 - Measured **spatial resolution ~15-20 μm**
 - Compatible with reference measurements from same sensor performed with commercial, high-power amplifiers

Time resolution for Channel #1

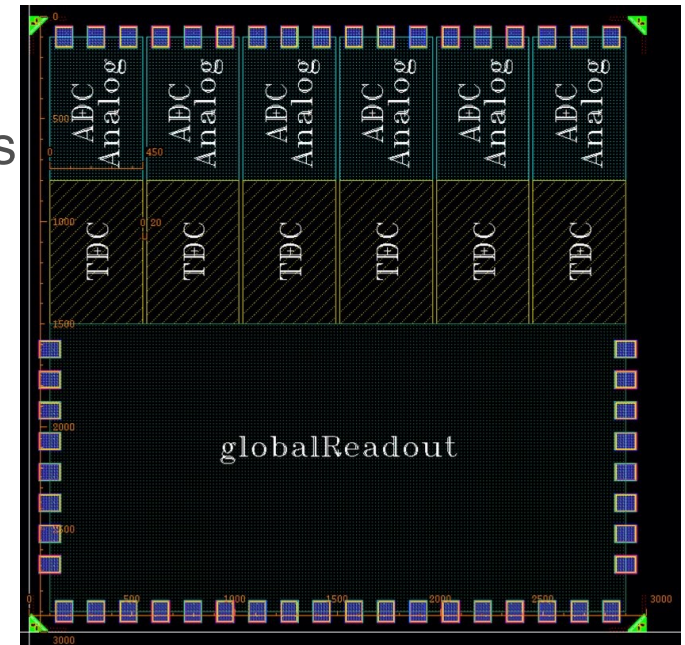


Resolution vs Y



Design status for FCFD1.2

- FCFD1.2 will implement TDC, ADC, I2C, and simplified readout on a 6-channel chip
 - Goals: test and verify all main components
 - Aim to submit by the end of 2025
- Design status
 - Design of the TDC and I2C is complete
 - Data format defined
 - ADC design in progress
 - Started to work on integration and verification of various blocks



Floorplan and I/O