EICROC status and plans
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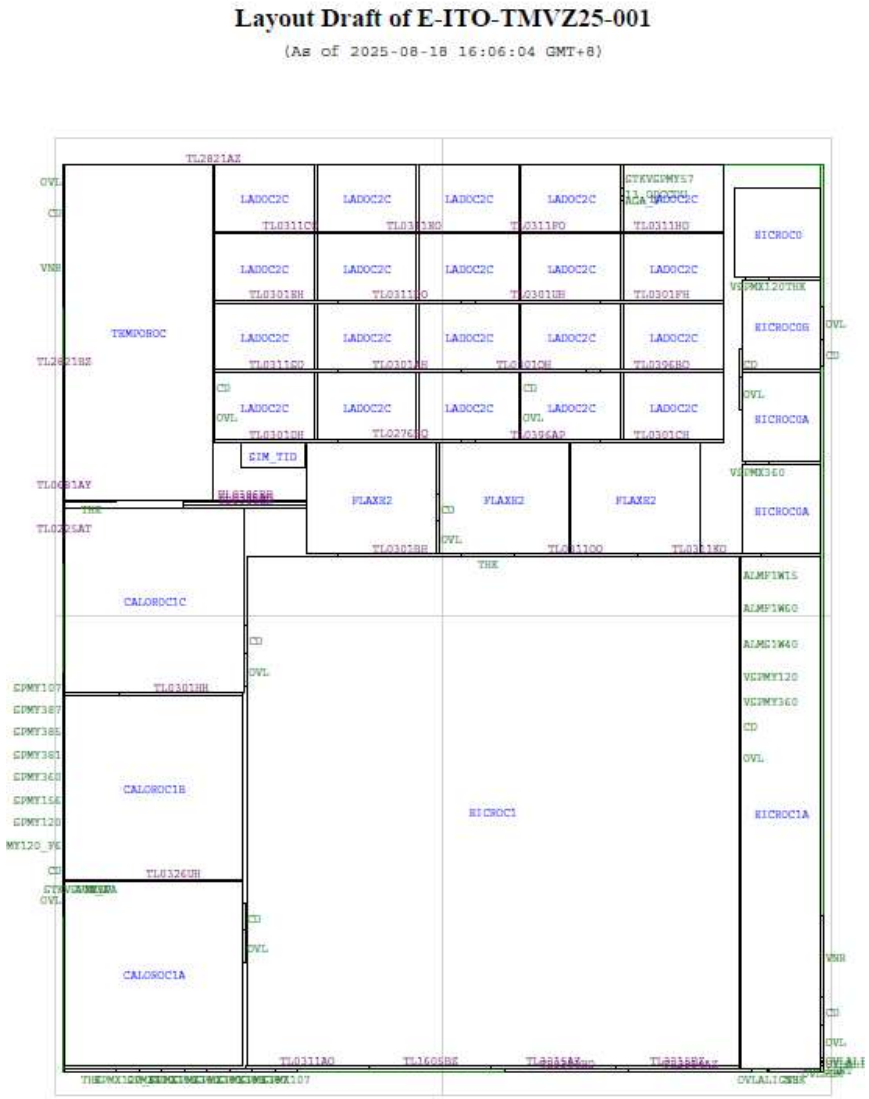
Organization for Micro-Electronics desiGn and Applications

EICROC reticle 2025

- EIC/ATLAS engineering run (may 25)
  - Just started this week (long administrative issues)
  - Still minor discussions with IMEC/TSMC
  - 5 wafers to be fabricated + 1 on-hold

- EIC chips 63% of wafer area
  - EICROCs 48%

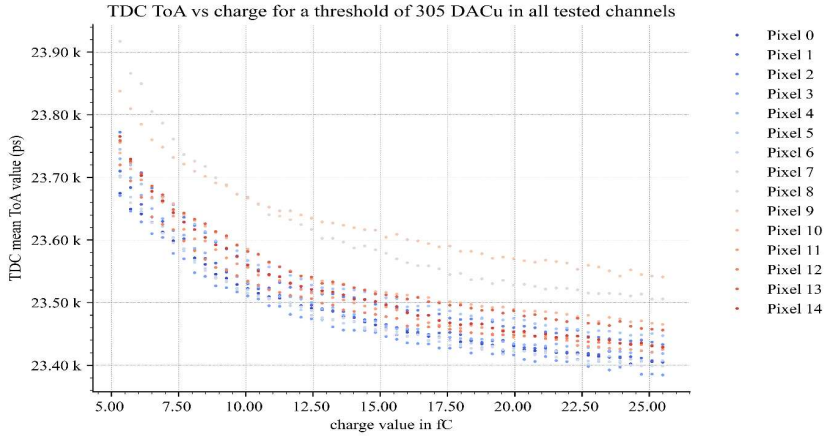


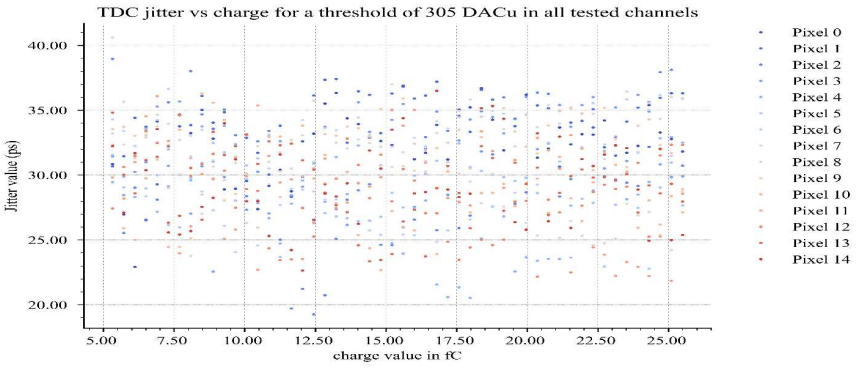
2025 : EICROCs variants

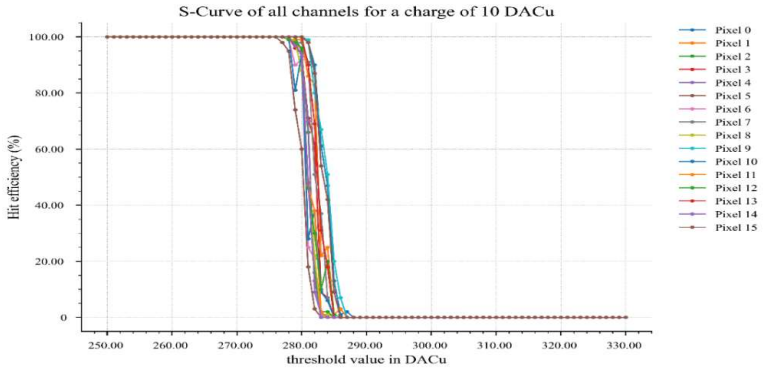
- EICROC0A : same as EICROC0 with more testability
  - Each pixel can be by-passed by SC (clock is then turned off)
  - Buffers in SC to allow extension to 4x32
- EICROC0B (4x4)
  - Same preamp/discri/TDC/integrator
  - ADC and driver replaced by peak sensing and Wilkinson ADC
- EICROC1A : 4x32
  - Same I/Os than EICROC0, same testboard
- EICROC1 : 32x32 (final I/Os)
  - Test interface with DAQ : fast commands and 320 Mb/s data output

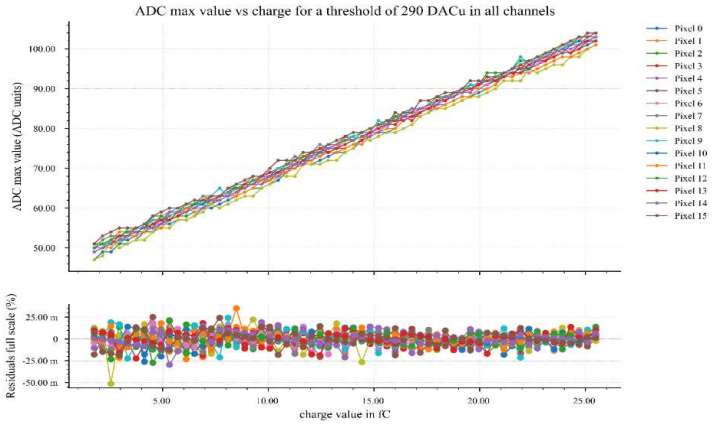
EICROC0 tests

- Electrical tests at OMEGA (ASIC alone)
- Tests with source and laser at IJCLAB (with sensor)







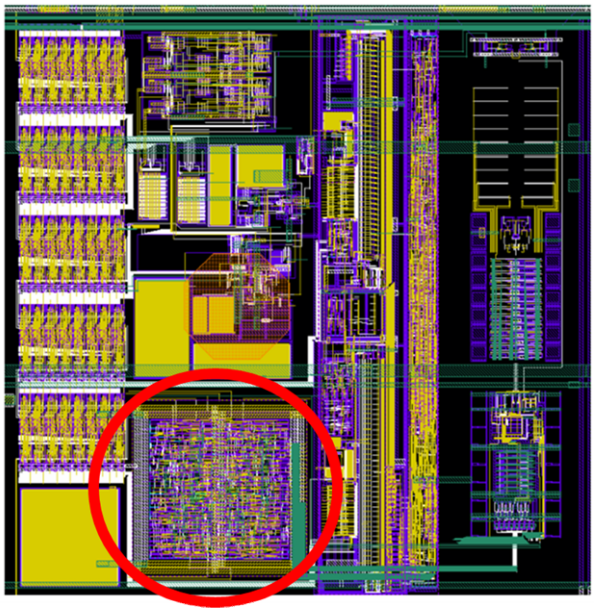


Future EICROC2 (2026)

- What is missing in EICROC1 ?
  - Larger rate compatibility ?
  - Derandomizer for successive events (how many ?)
  - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
  - Auto-trigger and zero_suppressed data
  - Power reduction if possible down to ~1 mW/ch

- Our colleagues from Clermont Ferrand now joining to help on the DoT
  - Already participated in ATLAS ALTIROC
  - The design and verification should take ~1 year from now

- Technology choice ?
  - Depends mostly on rate estimates and complexity of digital



Summary

- EICROCs finally going in fabrication
- Testboards being prepared for the end of Q4
- More measurements on EICROC0 going on
  - testpulse at OMEGA and laser at IJCLAB
- EICROC2 design started with Clermont Ferrand
  - Technology choice 65n/130n should be possible Q3 2026