Status of the AC-LGAD Readout Chain PED

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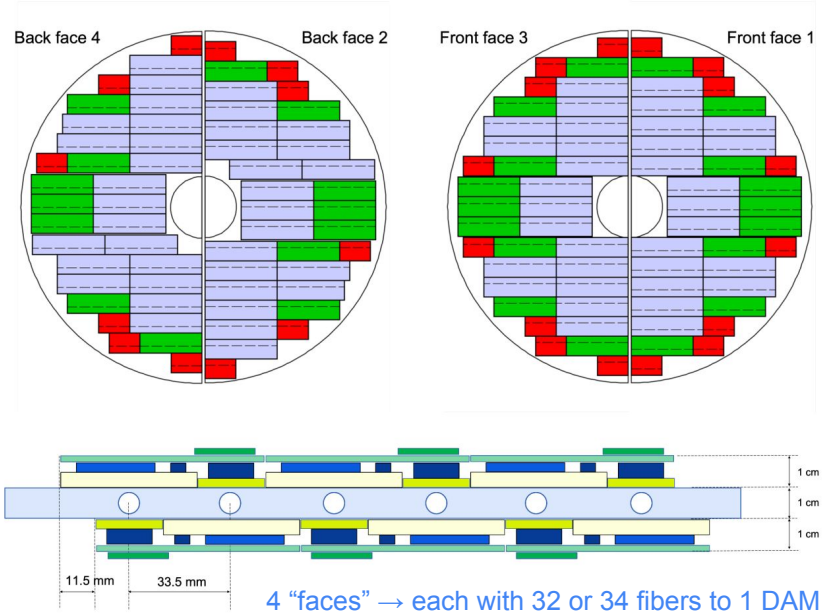
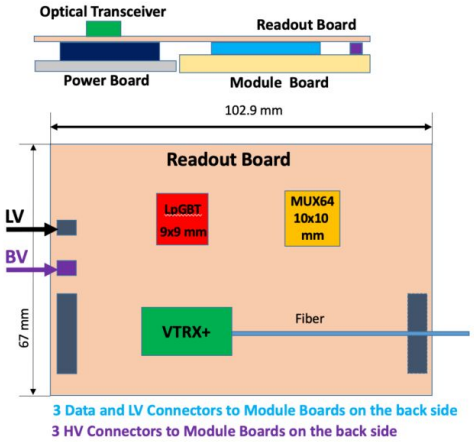
Tonko Ljubicic
for
Rice University, BNL, LBNL

Electronics Components Overview, using FTOF as an example

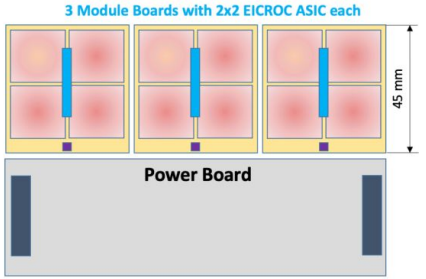


4 “faces” → each with 32 or 34 fibers to 1 DAM
⇒ total 4 DAMs

ETL FTOF Readout Board Prototype

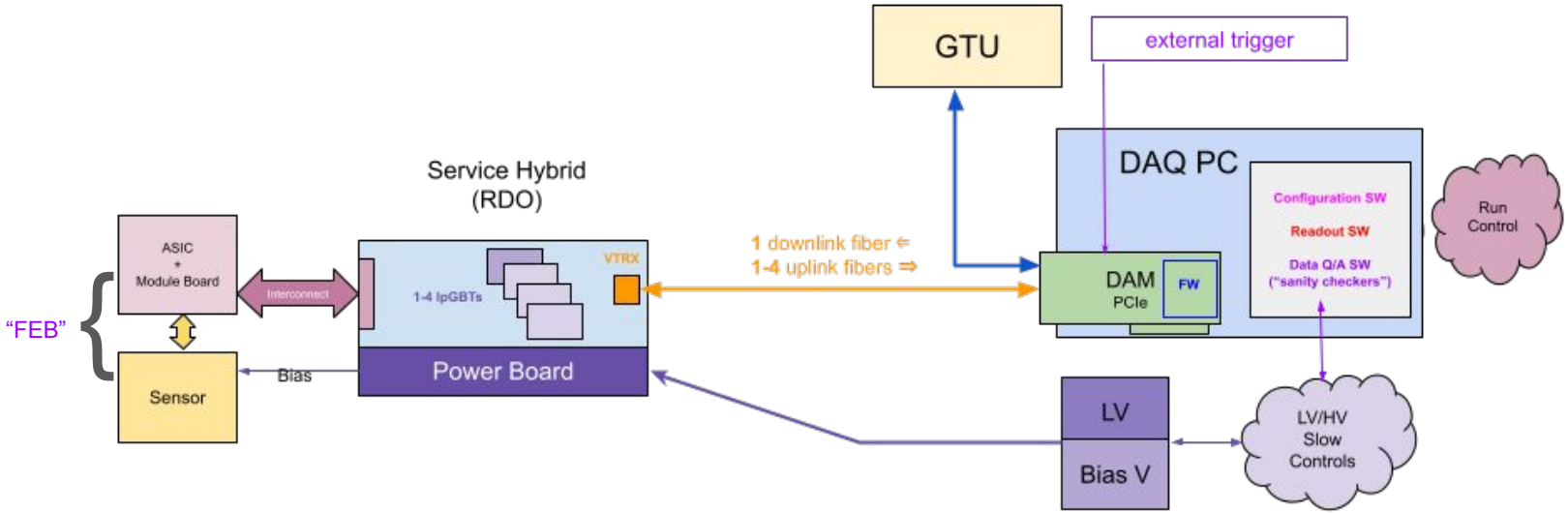


LpGBT: 10Gbps Rad Hard Transceiver ASIC
VTRX+: Rad Hard 4xTx (10Gbps) + 1Rx (2.56Gbps)
MUX64: Rad Hard 64-channel analog multiplexor



Notes:
1) Power Board is mounted on the Cooling Manifold as is the Module (ASIC) Board for cooling efficiency
2) All connections to the outside must go through the RB which is on the outside: fiber, LV but also Bias Voltage (BV)
3) These are small boards, ≤ 10 cm per side

What's the AC-LGAD Readout Chain



Deliverables of this PED

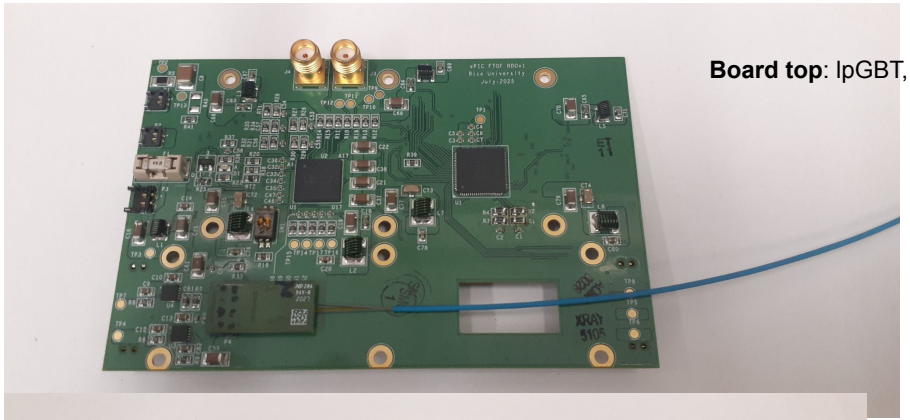
- AC-LGAD Readout Board RBv1 (Completed)
  - lpGBT & VTRX+ based
  - can interface to up to 12 EICROC1[2] ASICs
  - *serves FTOF, Roman Pots, B0 and other pixel AC-LGAD friends*
  - also serves as a V0 prototype for Barrel TOF
    - where it is expected to house 4 lpGBTs and to interface to FCFD ASICs
- Forward TOF Power Board PBv1 (Completed)
  - CERN bPOL48 as the main converter
  - serves also as V0 prototype for other AC-LGAD detectors
- Full Streaming Readout Chain over PCIe into DAQ using the Alinx AXAU15 DAM (Completed Stage 1 & 2)
  - equipped with an external trigger input, if required (completed) [Note: EICROC1 is still a triggered ASIC]
  - equipped with William's GTU adaptor for immediate interfacing to the future GTU (in progress)
  - can be used by any lpGBT-based detector
- Full measurement and compensation of jitter and other sources of clock drift (in progress)
  - very important for precise timing!
  - see later slides

External Boards to this PED

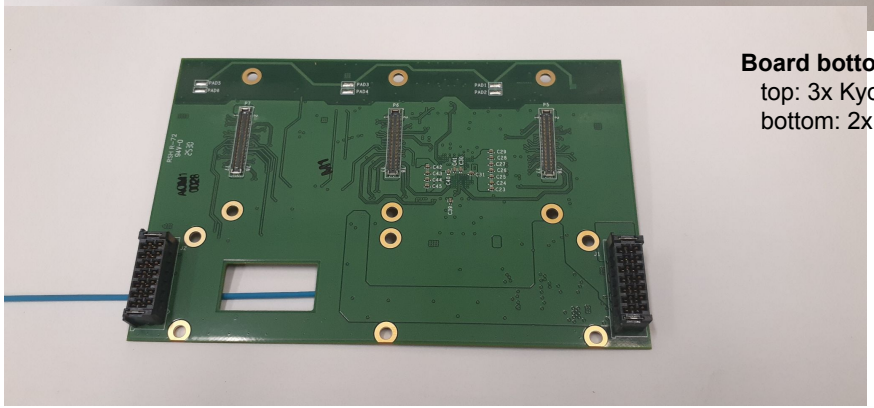
- William's GTU & Fiber Interface FMC card
  - for the AXAU15
  - obtained 2 pieces from JLab (thanks William & Dave!)
  - even without an actual GTU it enables a realistic clock propagation scheme
- EICROC1 Testboard (with an EICROC1)
  - via the EICROC1 Team
  - schematics obtained (thanks Kinann & Christophe!)
  - we plan to make a small adaptor card from the FMC connector of the Testboard to our Kyocera connector on RBv1 → in progress

More on this later

Deliverable 1: Readout Board RBv1



Board top: lpGBT, VTRX+, MUX64

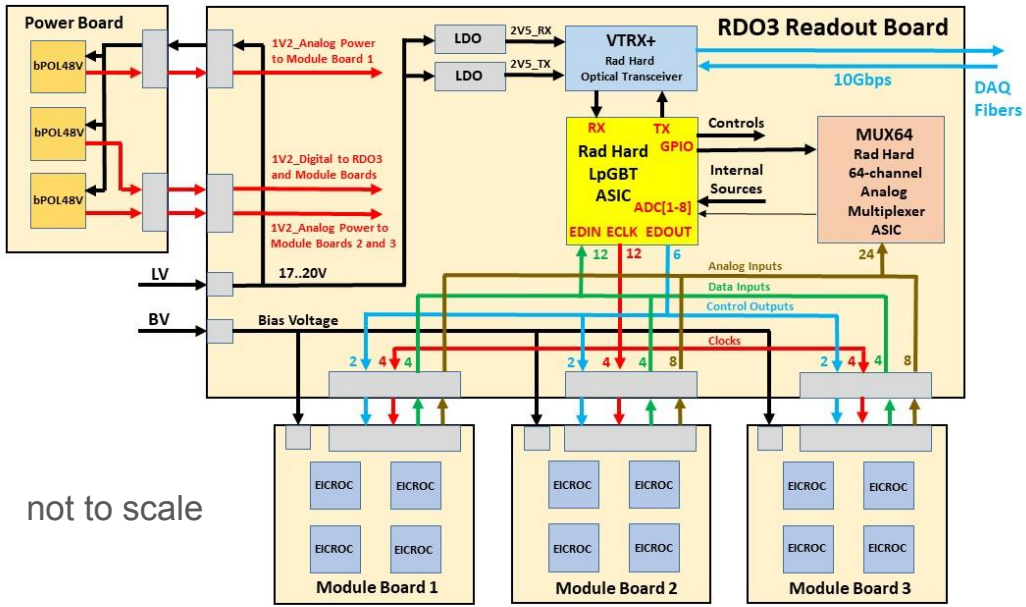


Board bottom:
top: 3x Kyocera connectors to 3x ASIC Modules
bottom: 2x connectors to the Power Board

Board size 103 x 67 mm (small…)

6 boards assembled
all 6 boards tested

Powering Scheme Reminder



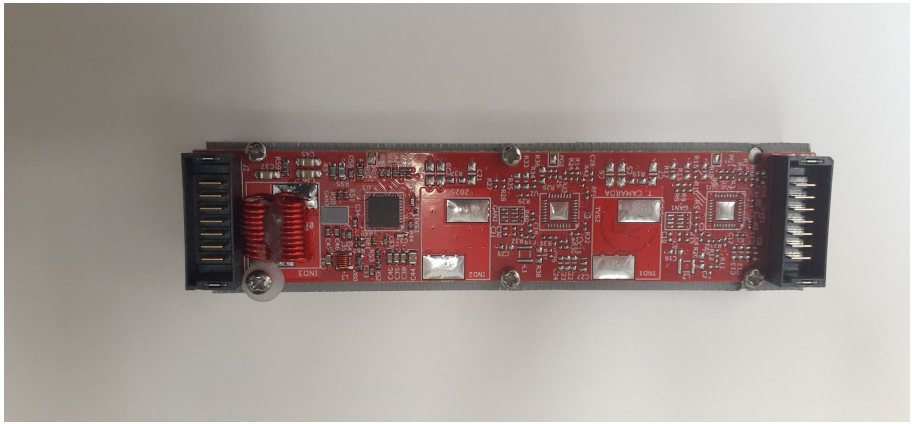
not to scale

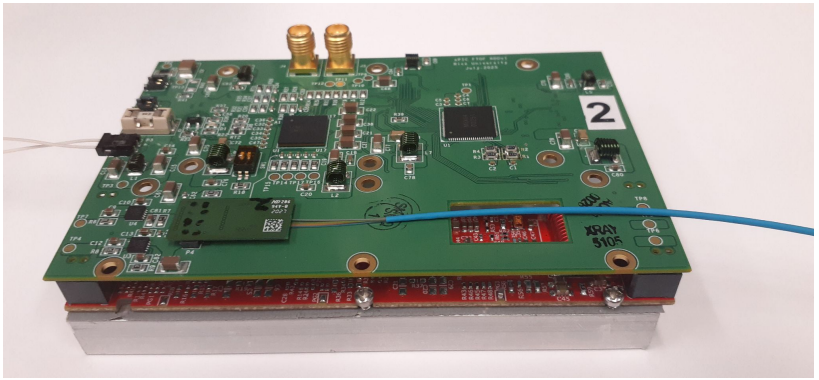
Note: Power Board ("PB"; leftmost) requires **3x bPOL48s**
2 for analog 1.2V to the ASICs
1 for digital 1.2V to the ASICs as well as the RB

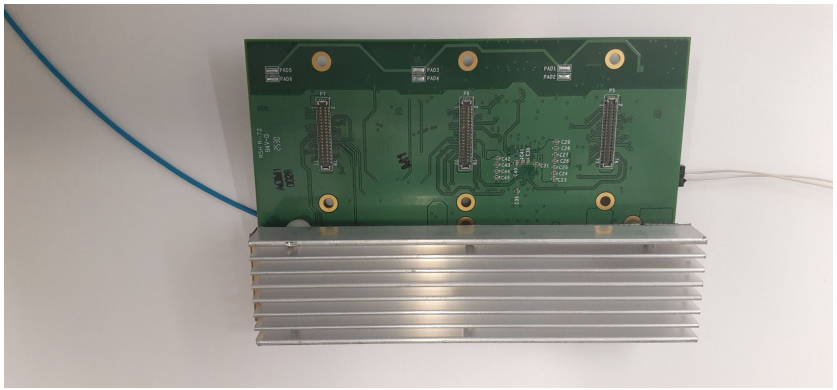
We can power 12 EICROCs with this V1 flavor of the PB

Deliverable 2: PBv1 Board

- Boards at BNL
  - we assembled 1 with 1 “analog”-channel **bPOL48** and tested the load
  - we assembled 1 with 1 “digital”-channel **bPOL48** and tested with our RBv1 at Rice [photos] – works and fits nicely!
  - we assembled 1 with all 3 **bPOL48** channels – will be used for further testing & characterization at BNL
  - NOTE: we only had 5 (five!) **bPOL48**s and have considerable problems in obtaining more due to EPIC-CERN interaction – HELP needed from the Project with small prototyping quantities (10 or so…)





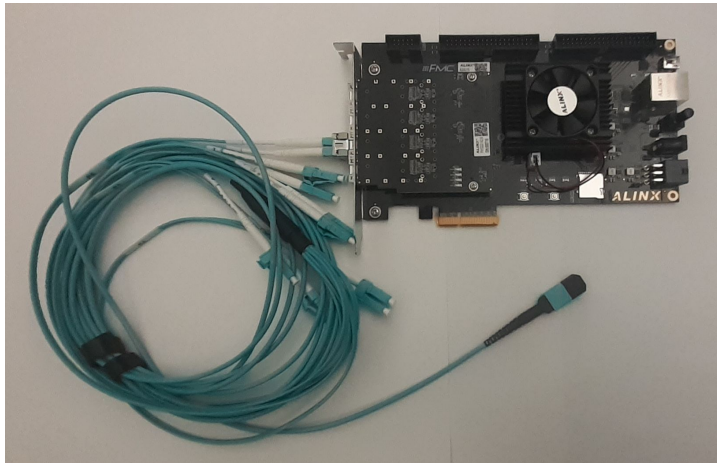


⇐ PBv1 is 103 x 22 mm

Cooling fins above act as the detector’s “Cooling Manifold” (slide 2)

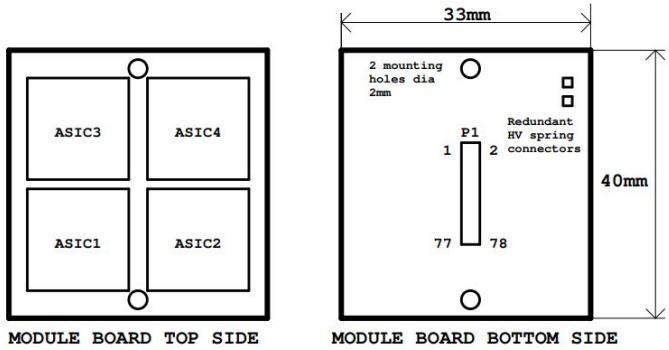
FELIX-lite DAM (purchased)

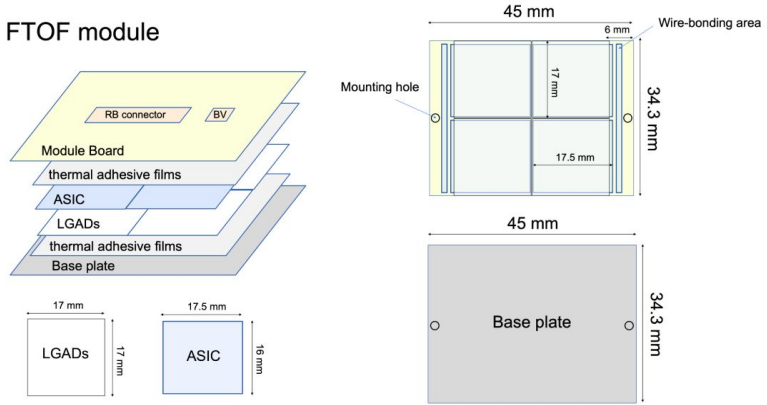
- we are using Alinx AXAU15 with a Xilinx Ultrascale+ Artix
  - available, cheap but similar in functionality to the FELIX
  - 8 possible fiber links
  - PCIe x4 PC interface
    - or USB
  - William's GTU FMC interface was tested with it
- FW sends and receives data to lpGBT at 10 Gbs
  - configures lpGBT
  - reads Slow Controls data (ADCs)
  - writes Control values (GPIO)
  - also to an ETROC "demonstrator" ASIC
- Streaming Readout into PC memory
  - software, device drivers, etc complete
  - typical timeslice ~1 ms



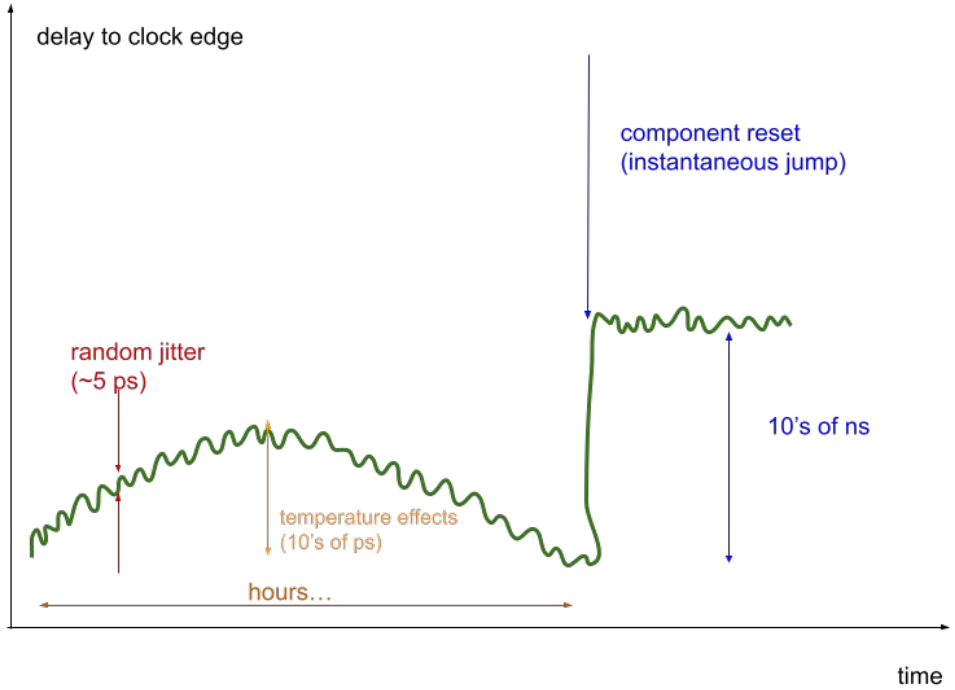
ASIC Interface (EICROC1)

- We plan to produce a small adapter card from our Kyocera connector on RBv1 *to the future EICROC1 Testboard's* FMC
  - We obtained the schematics and are checking if this can be done
    - so far we are iterating with Omega on this subject but don't expect show-stoppers
- We are also considering making our own ASIC Module Board "MBv1" as we expect to have it in our FTOF design [ORNL] (see ⇒)
  - this is under discussion…
  - …but outside the scope of this PED
- We plan to be 100% ready for ASIC integration and testing once the EICROC1 is available [end of CY2025 or early CY2026?]
- Note that we have a "generic" connector to an ASIC Module so we can adapt other designs where the ASIC is further away via cables of flex PCBs
  - Roman Pots, B0, BTOF…
  - …but outside of this PED





Critical Clock Delays – Measurement & Control



Sources of jitter and clock drift

- Random Jitter (the “proper” jitter)
  - 20-30 ps AC-LGAD sensor
  - ~10 ps ASIC internals + TDC resolution (estimated)
  - ~10 ps external clock to the ASIC
    - ~5 ps from lpGBT (measured but we will re-measure using our RBv1)
    - ~2-5 ps due to transmission medium/cable (guess)
      - longer cables increase jitter
      - this needs a more careful study for detectors with cables from the RDO to the ASIC – depends on the particular cable & length
- Slow Variation (~hours)
  - CERN showed 10’s of ps variation due to temperature changes of the (long!) fibers
  - CERN developed the “TCLink” firmware for Xilinx devices which measures and automatically compensates with <10ps variation ⇒ something we will use and are currently implementing in the AXAU15 board
  - NB: we don’t expect significant (>2 ℃) changes in temperature in EPIC (IMHO), however we would really like to have it *continuously tracked and measured* regardless
- Reset Jumps
  - Non-deterministic change of clock propagation delays at times of component reset (at startup, during auto-recoveries, etc)
  - Mostly in the fiber transceivers due to their internal nature (very manufacturer specific)
  - **Coarse –** multiples of the 320 MHz parallel data clock
  - **Fine** – multiples of the 10 GHz serial clock
  - Coarse
    - Observed with our Xilinx’s MGTs ⇒ <10ish internal 320 MHz clock cycles change reset-to-reset
    - Easy to observe using the internal lpGBT loopback
      - even more so with the ASIC internal loopback (expected to be implemented in EICROC, CALOROC, etc)
    - Jumps are quantized to a few different values
    - Solution: keep resetting the interface and stop when the most common value is observed
      - this value becomes a configuration parameter of this specific link
  - Fine
    - need TCLink’s machinery to manipulate the “TX buffer status” – in progress

Measurement plans

(Reminder: fiber parallel data clock is 315.2 MHz, same as the EICROC1 clock)

1. basic jitter measurement on the output of lpGBT (ECLKxx) which goes to the ASICs (315.2 MHz)
   a. RBv1 is equipped with SMA connectors for this purpose
   b. expect 4-8 ps
2. slow clock drift (temperature dependant) using a long 100m fiber
   a. difference of the clock edges of the input clock to the DAM vs the lpGBT ECLK
      i. we'll start with day vs night
   b. with and without TCLink compensation
3. reset jumps aka difference of the edge of the DAM input clock and the lpGBT ECLK after board resets
   a. reset RBv1, reset DAM, reset both ⇒ repeat many times, measure
   b. with and without compensation

Mostly to be done at BNL with a fast modern scope

Future, not in PED: FELIX

- …as stated, we plan to complete our full streaming readout chain using AXAU15
  - …and use it for beam tests, lab tests etc due to its convenience
- However, we would like to start with a real FELIX DAM
  - large amount of FW exists (a large group of CERN people involved)
  - we need to see what is available in the core FELIX FW and check if it meets our requirements
  - we (Rice) would like to do this in concert with the DAQ Group
    - what's the plan of the DAQ Group?
    - and what is the FELIX availability?

Summary

- We manufactured or received all components of the Readout Chain
  - apart from an ASIC module
- Firmware on the AXAU15 card in good shape
  - interface to lpGBT complete
  - streaming readout into the PC memory complete
  - software components in good progress
    - monitoring, slow controls and run-control in development
    - file formats and readers in progress
  - ASIC readout tested with ETROC module borrowed from CMS
  - Realistic GTU-like clocking in progress
    - using William's FMC card
- Jitter and clock stability measurements will start soon

Waiting for the EICROC1 ASIC!