Inner MPGD CyMBaL Status

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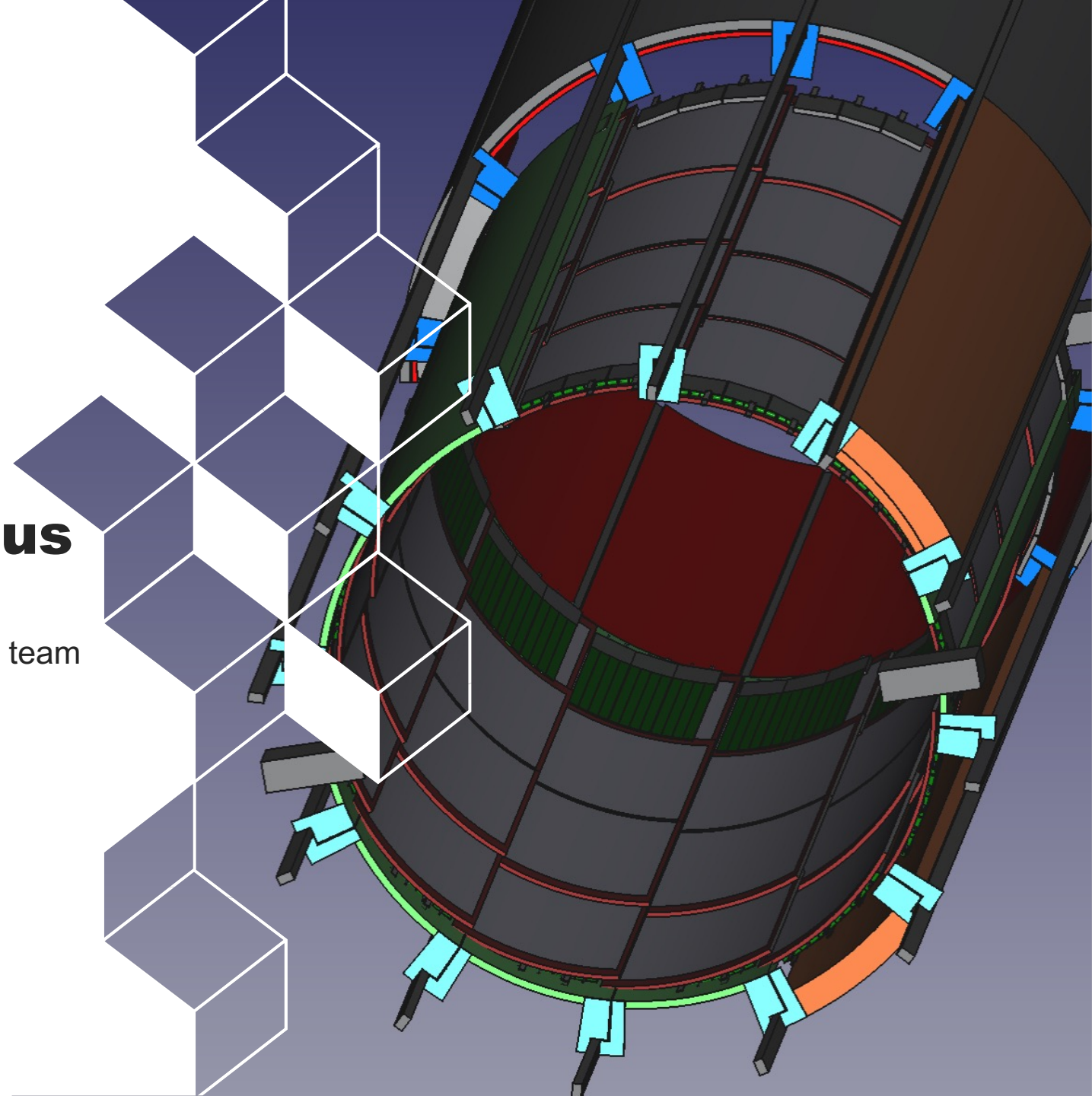
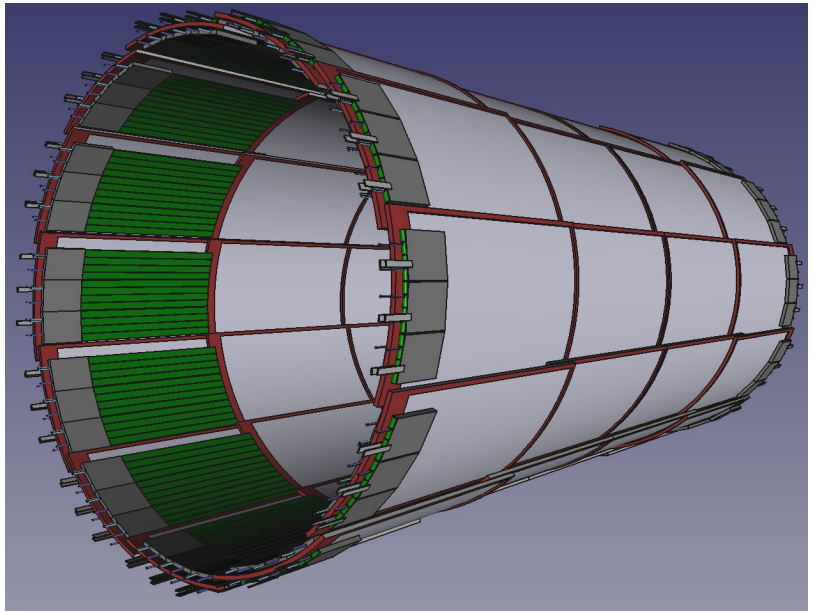


EIC/EPIC 3I meeting, 27 october 2025

CyMBaL tiles integration

CyMBaL: Current design



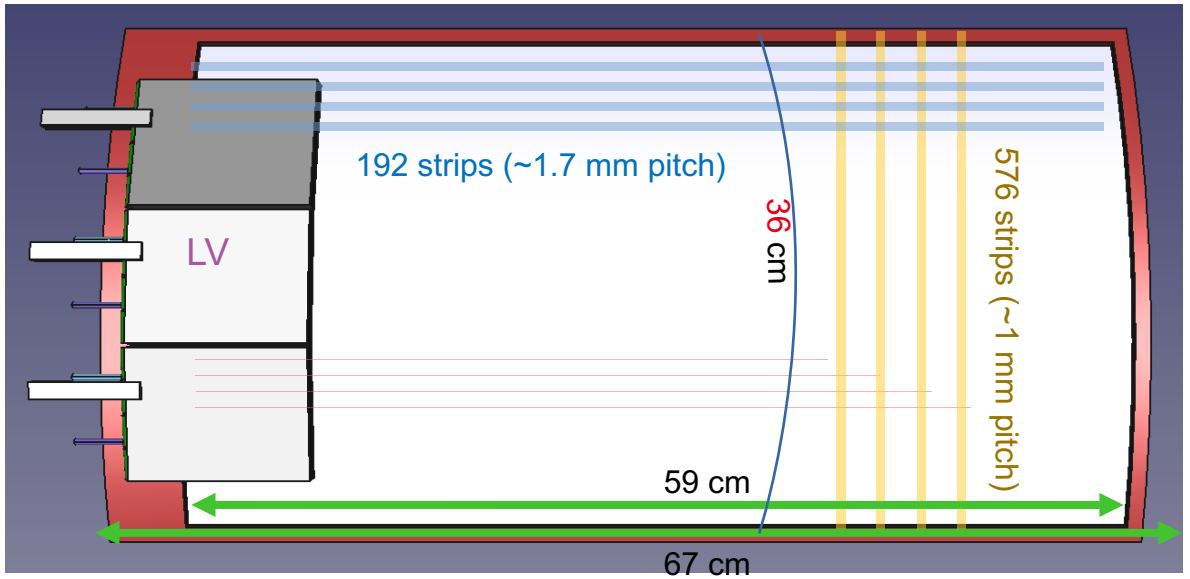
Services
via patch panel(s)

- 3 OF (to DAM)
- 5 HV cables (TbC)
- 3 LV cables (1 tile)
- Gas I/O (2 tiles)
- FEB cooling I/O

2 tiles – 6 FEBs+DC/DC

few l/mn of 18°C water

Design of a tile (**Cylindrical**)



48 tiles: 12 in ϕ × 4 in z (integration in GST in "fish scale")

- R_{min} = 55.5 cm; R_{max} = 61.0 cm **(new baseline October 6)**
- Overlaps in ϕ and in z for hermeticity
- 768 readout channels/module
- **36K readout channels in 3 FEBs/tile (increase from 32K)**

Module dimensions

Z = 67 cm / R*phi = 36 cm

Active zone dimensions

Z = 59 cm / R*phi = 34 cm

Weigh estimates

~1 kg / tile + ~0,6 kg / FEB

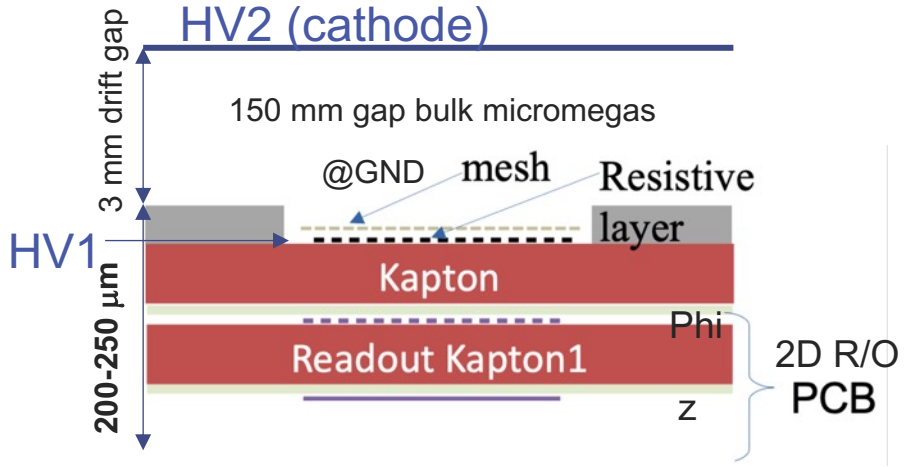
Expected performances

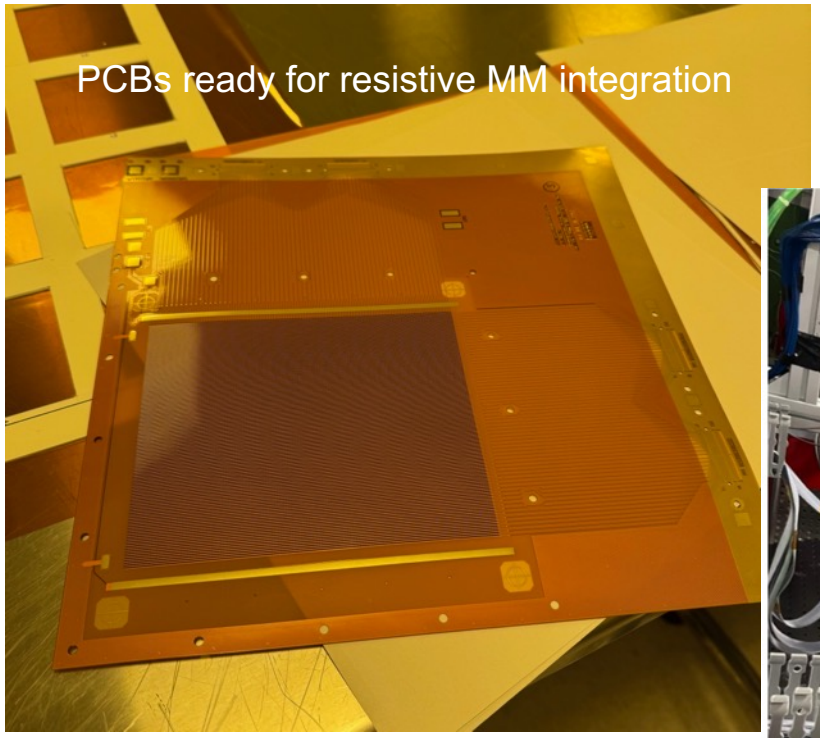
- Spatial resolution: < 300 (500) µm in Z (r*phi)
- Time resolution ~20ns
- Efficiency ≥ 98%
- Material budget ~0.5% X0

Start of wednesdays 11am ECT biweekly meetings for CyMBaL/TOF/GST design, status and /coordination (Dan, Roland, Alain, Seraphin, Sushrut, …)

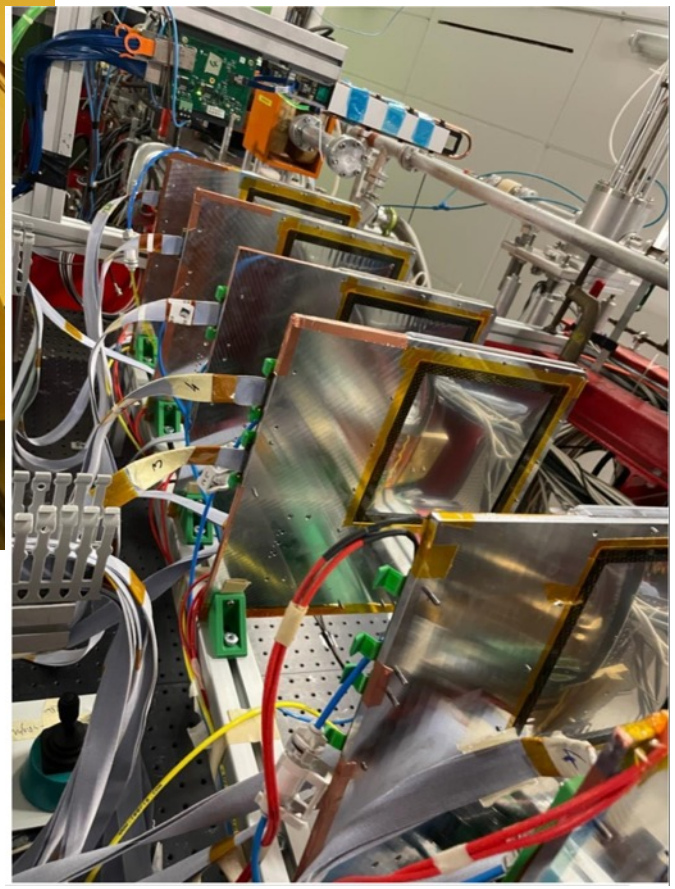
CERN/SPS upcoming testbeam preparation (w45-47)

Goal : spatial & timing resolution Vs resistive paste layer configuration (paste, pattern, resistivity)





2023 testbeam setup
(similar setup for 2025)



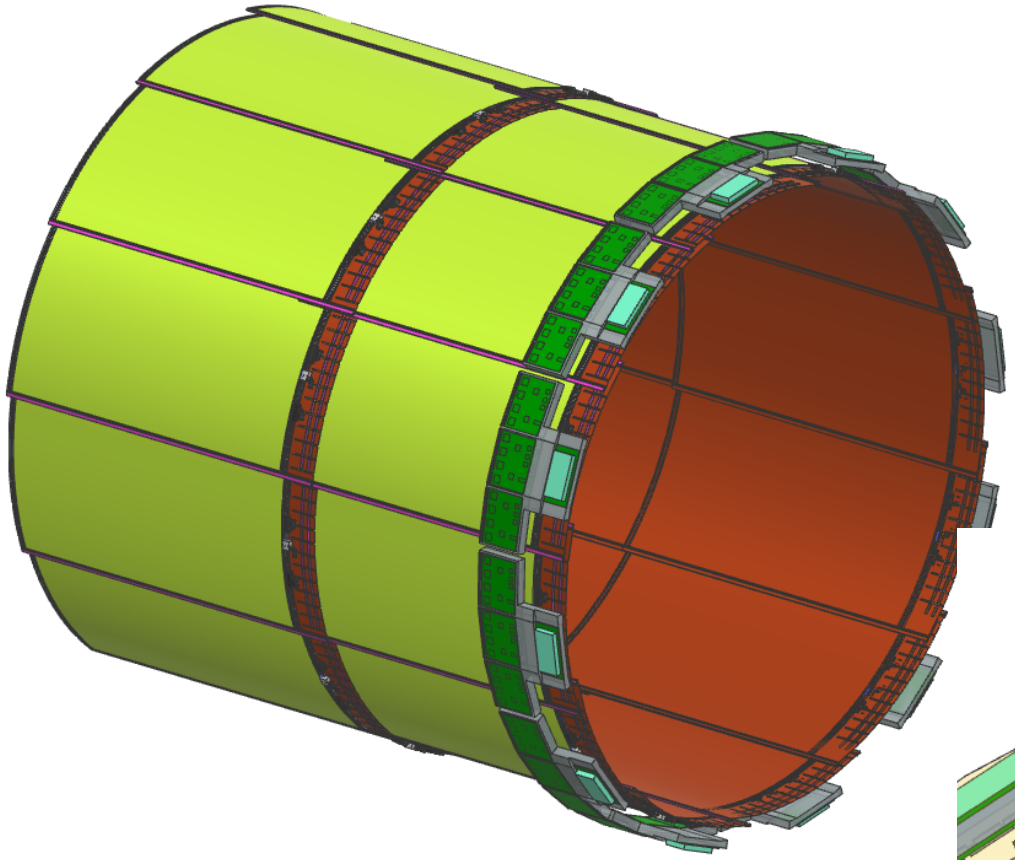
4 chambers (10x10 cm²) with new 2D R/O

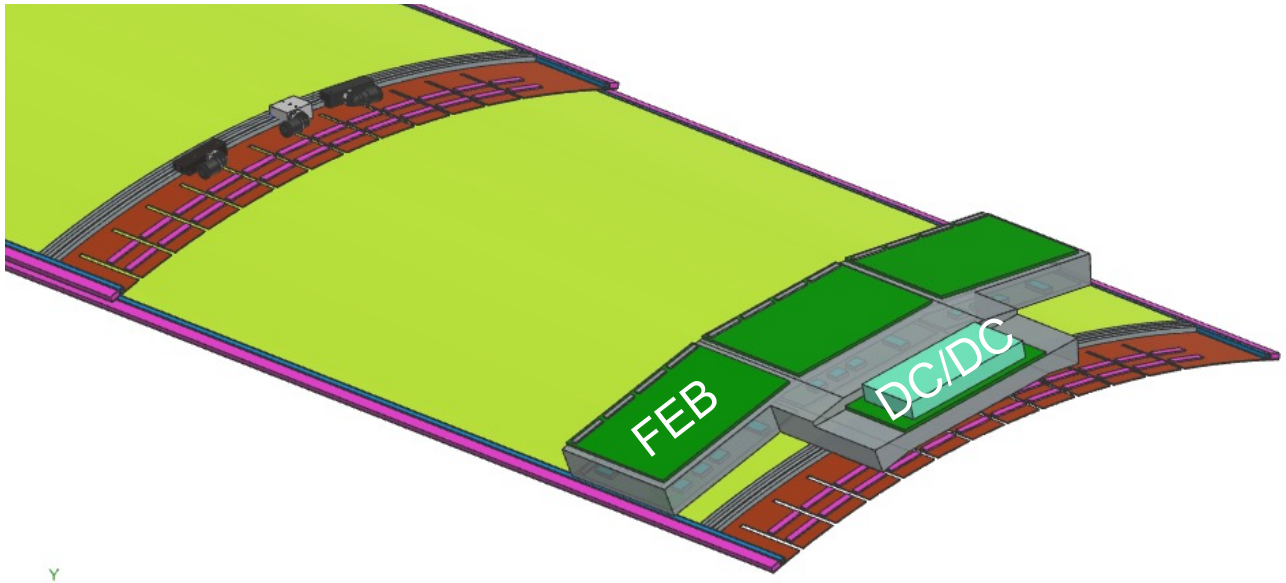
- Phi-z Strip pitch : 1 mm / 1.2 mm
- Phi-z strip width 300 µm / 1.08 mm
- Resistive layer : plain, strips, with 3 different inks (ESL, SARAL, VFP), 1-5 Mohm/sq.
- New micromegas bulk integration process with new photoimageable dynamask (2x75 µm layers)

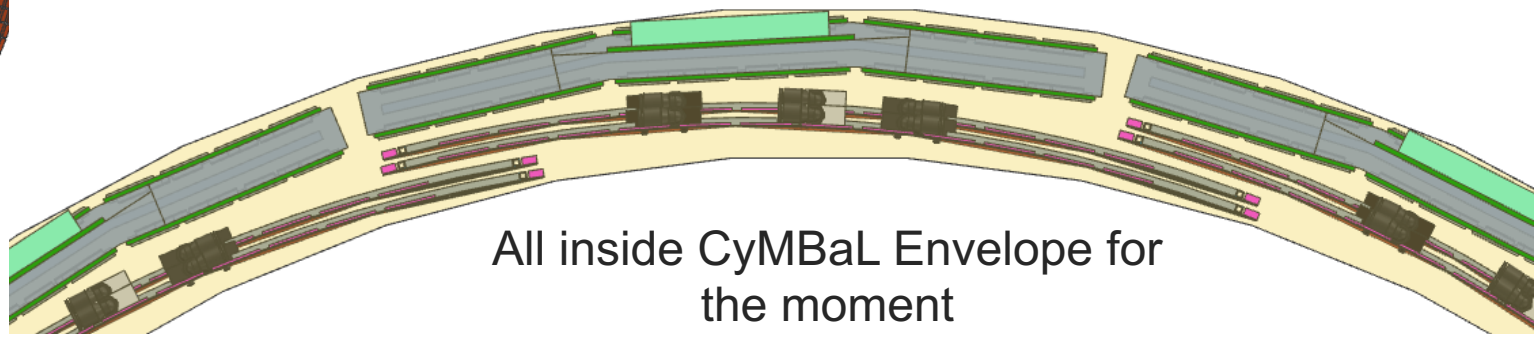
Note: Phi-z strips pattern following **old EPIC 32 CyMBaL tiles configuration !**
(1.7 mm / 0.7 mm (phi) – 1.02 mm / 0,9 mm (z))

On-going design study of CyMBaL integration

- The CAD design of a Scale 1 CyMBaL tile just started
  - Detector 2D readout printed circuit board with the 2D readout segmentation for best spatial resolution in z
  - Design and development of the mechanicals and tools for cylindrical shaping of the tile and its assembly
  - **FEB & DC/DC cards overlapping tile active area +** tile protective shell needed → **increase of x/x0 to estimate**

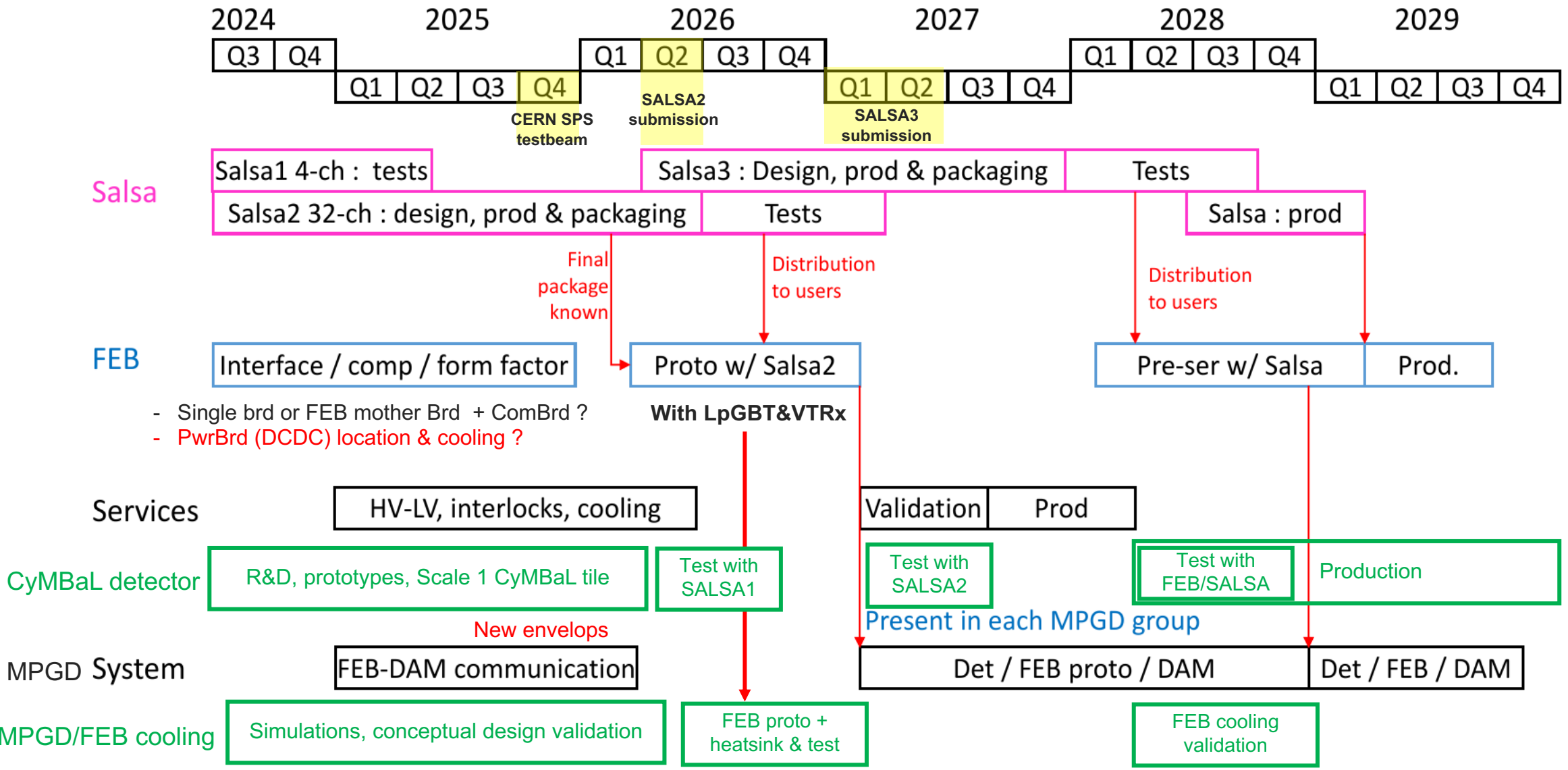






All inside CyMBaL Envelope for the moment

CyMBaL Timeline



Needed « global » Inputs : Chiller specs, pressure drop, coolant flow, … ?

EIC/DET project

3I PDR (8-9 dec)

CD-2

CD-3

To address at CyMBaL/TOF/GST biweekly meetings

- **Main goal of these biweekly meetings :** coordination of the design of 1/12 sector assembly of CymBal + TOF, its services routing, its support and mounting-dismounting on the GST.

- What is the **updated envelop for CyMBaL** ? → work with 55.5 cm – 61 cm (2025 oct 6).

- Is there any **additional space** that could be used for **DC/DC converter cards** ?
  → on-going study to fit them within CyMBaL envelop

- How is the **cable tray** space managed ? Space shared by CyMBaL & TOF ?

  → for CyMBaL, this space will be used for Gas pipes, Front-End electronics cooling pipes & HV cables. Signal micro-coax cables are within CyMBaL envelop & LV+optical fibers are connected on FEBs at both sides of the CyMBaL barrel.

- For installation/maintenance, what is the foreseen strategy for cabling : one reserved location for **patch panels** and/or does each sub-detector need to manage his patch panels within its own envelop ?