ePIC Electronics & DAQ WG DAQ Protocol discussion

ePIC DAQ meeting
Filippo Costa (CERN/ALICE)

Agenda

I will share my experience in ALICE, as firmware developer and detector readout expert.

I will go through some details of the GBT and lpGBT protocol in FPGA.

Challenges in DAQ operations concerning:

- Support.
- Debug.
- Code maintainability.
- slow and fast control.

With the risk to sound obvious I will cover some topics that I consider important at this stage of the development.

If I sound obvious, I apologize for that.

Filippo Costa

STAFF at CERN since 2008

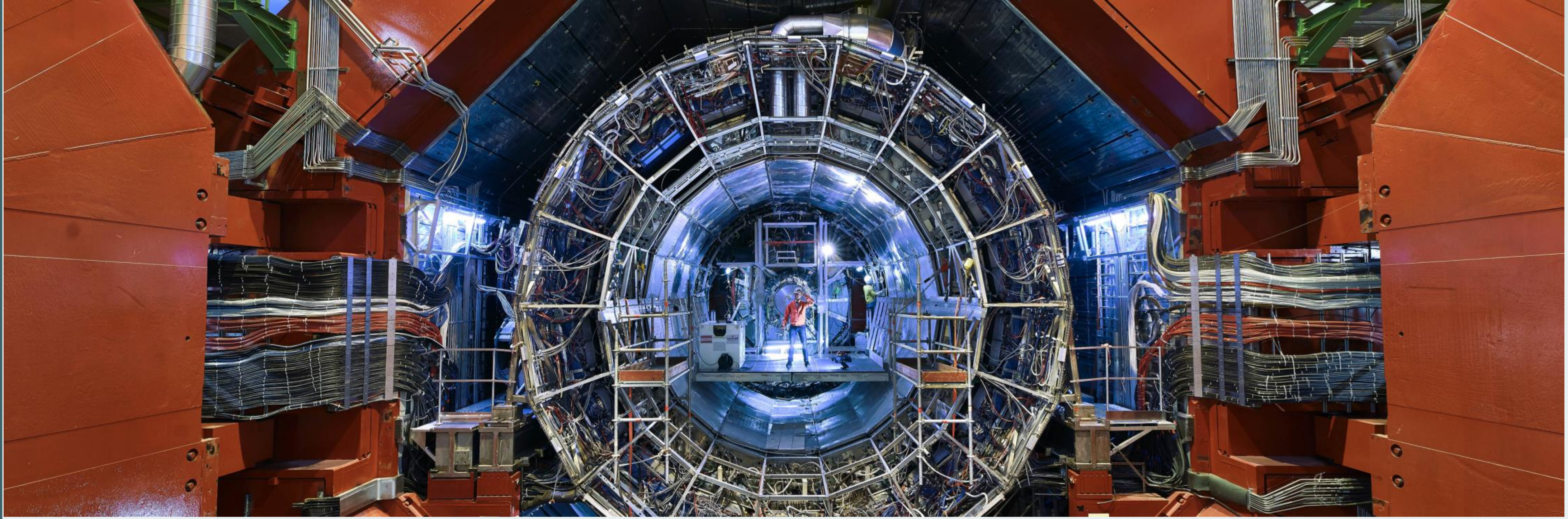
- DETECTOR READOUT EXPERT
- ALICE SW RELEASE COORDINATOR

Development:

- Software and firmware developer for DAQ readout card.
  - Experience in fw development for readout cards:
    - CRORC - XILINX VIRTEX 6 (old project still running on ISE)
    - CRU ALTERA ARRIA X
    - FELIX-182/155 (WIP)
  - Software, python tools to configure and monitor the card.

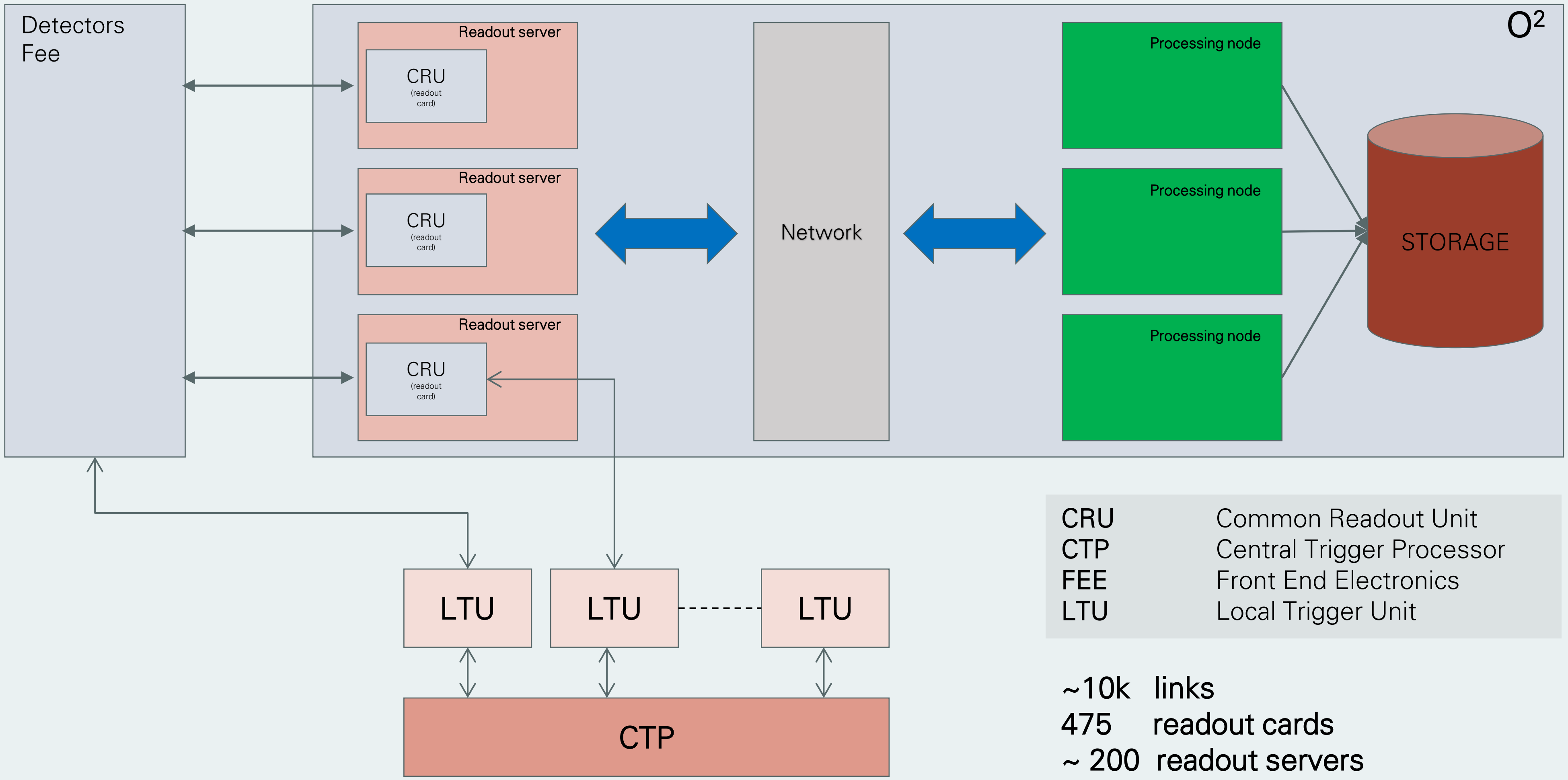
Coordination and support

- Responsible for the detector readout activities in ALICE.
- ALICE Software Release Coordinator.



ALICE OVERVIEW and LESSONS LEARNED FROM THE PAST.

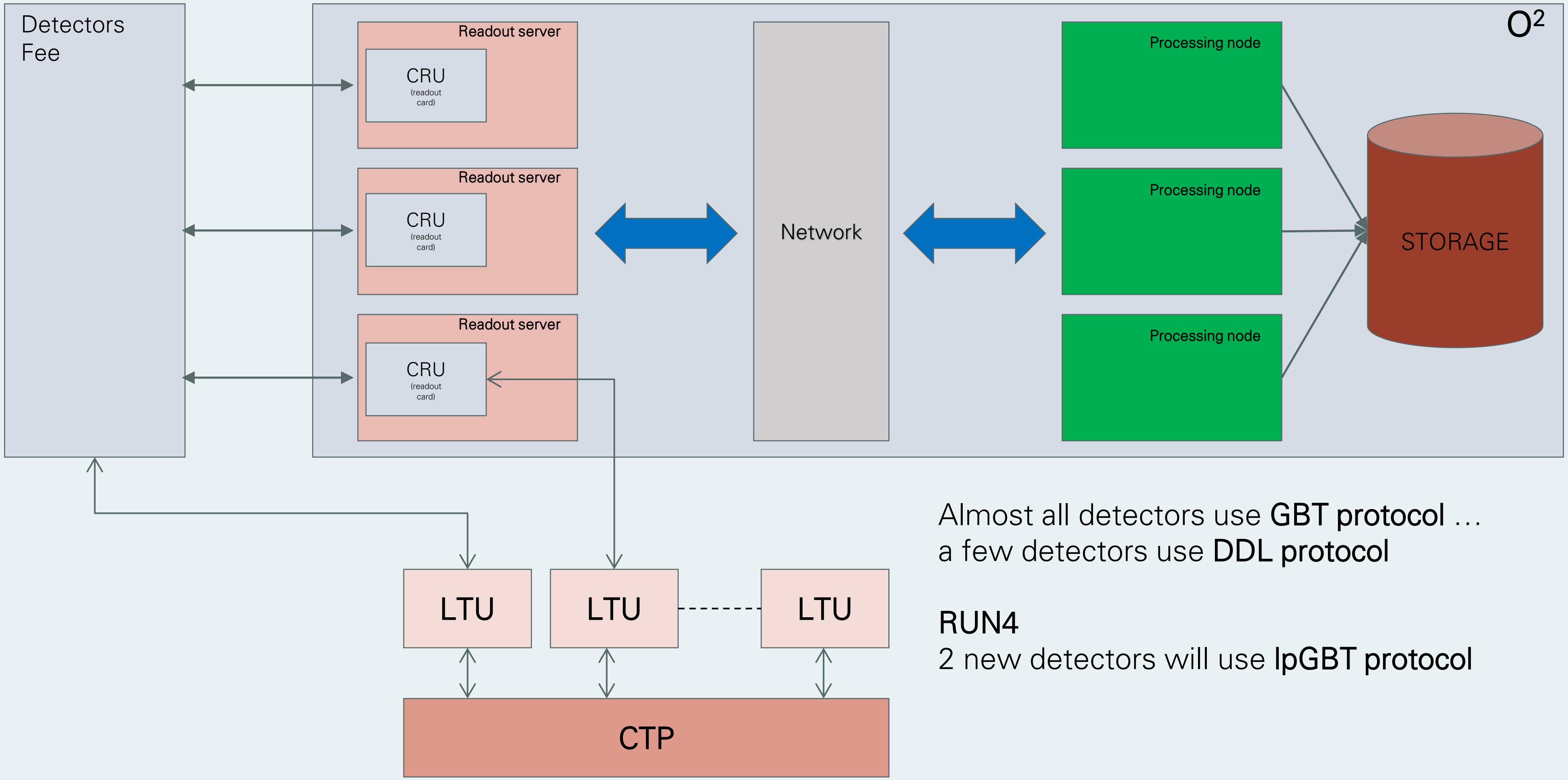
ALICE overview



CRU	Common Readout Unit
CTP	Central Trigger Processor
FEE	Front End Electronics
LTU	Local Trigger Unit

~10k links
475 readout cards
~ 200 readout servers
~300 processing nodes

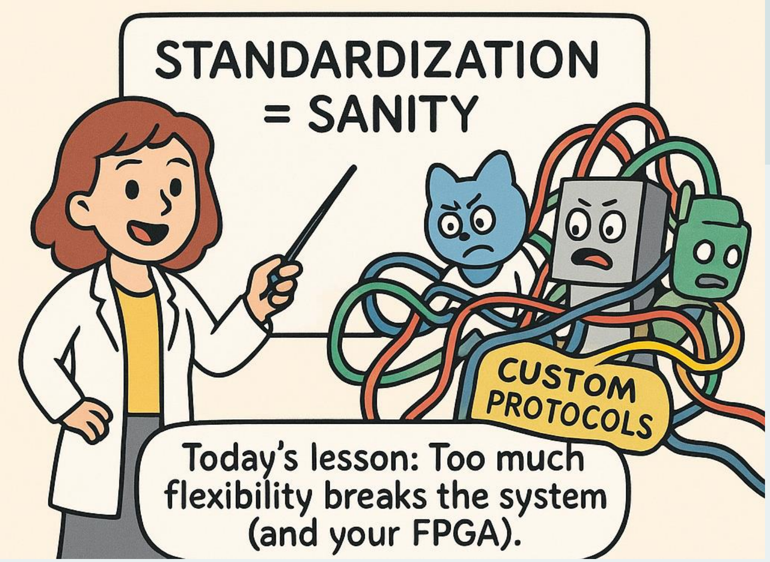
ALICE overview



Almost all detectors use **GBT protocol** …
a few detectors use **DDL protocol**

RUN4
2 new detectors will use **lpGBT protocol**

What we learned from the past



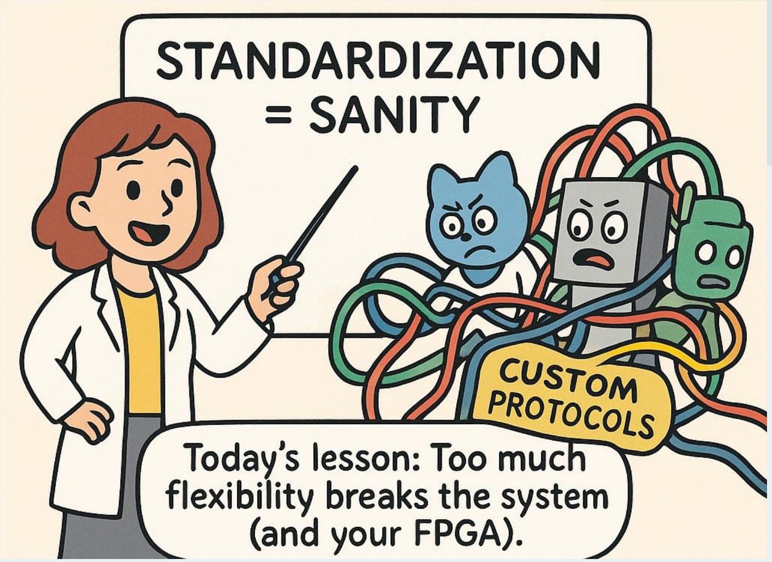
Why did we start RUN3 using different link protocols?

- Hard requirement, not a DAQ choice !!!
- Some detectors could not upgrade their front-end electronics.

Challenges in integrating the old protocol into the new system.

- The new continuous readout system was designed around the flexibility of the GBT protocol, enabling parallel operations (slow control, clock recovery, and data transfer). Integrating the legacy protocol required substantial adaptation and introduced operational limitations.
- Significant modifications were needed to make the old protocol compatible with the new software and higher data rates, as it was not originally designed for such performance.
- Most of the issues coming from the chain using the old protocol were not reproducible by other systems or in the lab and they required intense debug session in production.

What we learned from the past



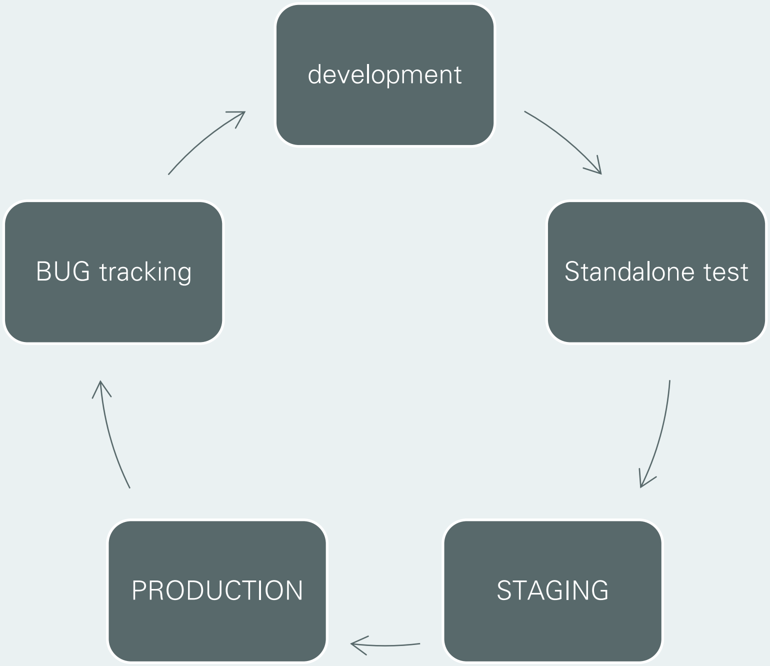
Challenges will not come only from protocol implementation. They will also arise from (technical/coordination issues):

- Firmware and software verification.
- Deployment in production.
- Coordination among experts working on different features.

ALICE sw deployment in 2022

ALICE sw deployment in 2025

We deploy and verify the sw in production in less than 1h with a success rate of 99%.



- Development
  - experts develop the new feature.
- Standalone test
  - experts verify the new feature in their test system.
- STAGING
  - the new sw is deployed in STAGING and tested.
- PRODUCTION
  - if STAGING test is passed the new feature is validated in PRODUCTION.
- BUG tracking
  - if there are new issues, tickets are opened and assigned to experts.

O2 General / O2-4771

SW verification in STAGING

Edit | Add comment | Assign | More | Open

Details

Type:	Story	Resolution:	Unresolved
Priority:	Major	Fix Version/s:	None
Affects Version/s:	None		
Component/s:	None		
Labels:	ALICE-PP-2024		

Description

This ticket collects the results of the software upgrade verifications in staging.

Attachments

Drop files to attach, or browse.

Sub-Tasks

1. SW validation - 2024/03/18	CLOSED	Filippo Costa	
2. new reference run 372	CLOSED	Filippo Costa	
3. SW validation - 2024/03/22	CLOSED	Filippo Costa	
4. PbPb reference run	CLOSED	Filippo Costa	
5. SW validation 2024/04/02	CLOSED	Filippo Costa	

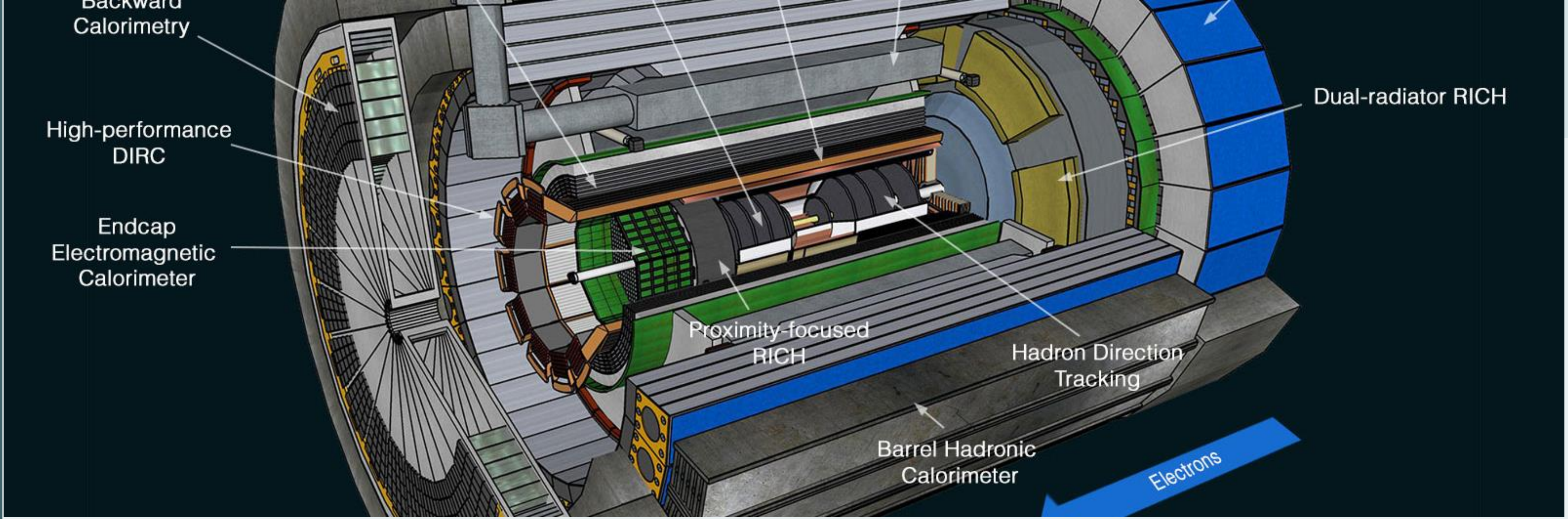
Issue	Assignee	Reporter	Priority	Status	Resolution	Created
∑ Summed Values						
~~O2-4813~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	01/Apr/24
~~O2-4788~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	22/Mar/24
~~O2-4762~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	14/Mar/24
~~O2-4736~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	07/Mar/24
~~O2-4704~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	28/Feb/24
~~O2-4690~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	26/Feb/24
~~O2-4662~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	15/Feb/24
~~O2-4653~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	13/Feb/24
~~O2-4610~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	30/Jan/24
~~O2-4600~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	FIXED	25/Jan/24
~~O2-4454~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	01/Dec/23
~~O2-4432~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	27/Nov/23
~~O2-4384~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	16/Nov/23
~~O2-4347~~ O2 sw update	Filippo Costa	Filippo Costa	Minor	CLOSED	DONE	08/Nov/23

Description

SW update JIRA: https://its.cern.ch/jira/browse/O2-4813

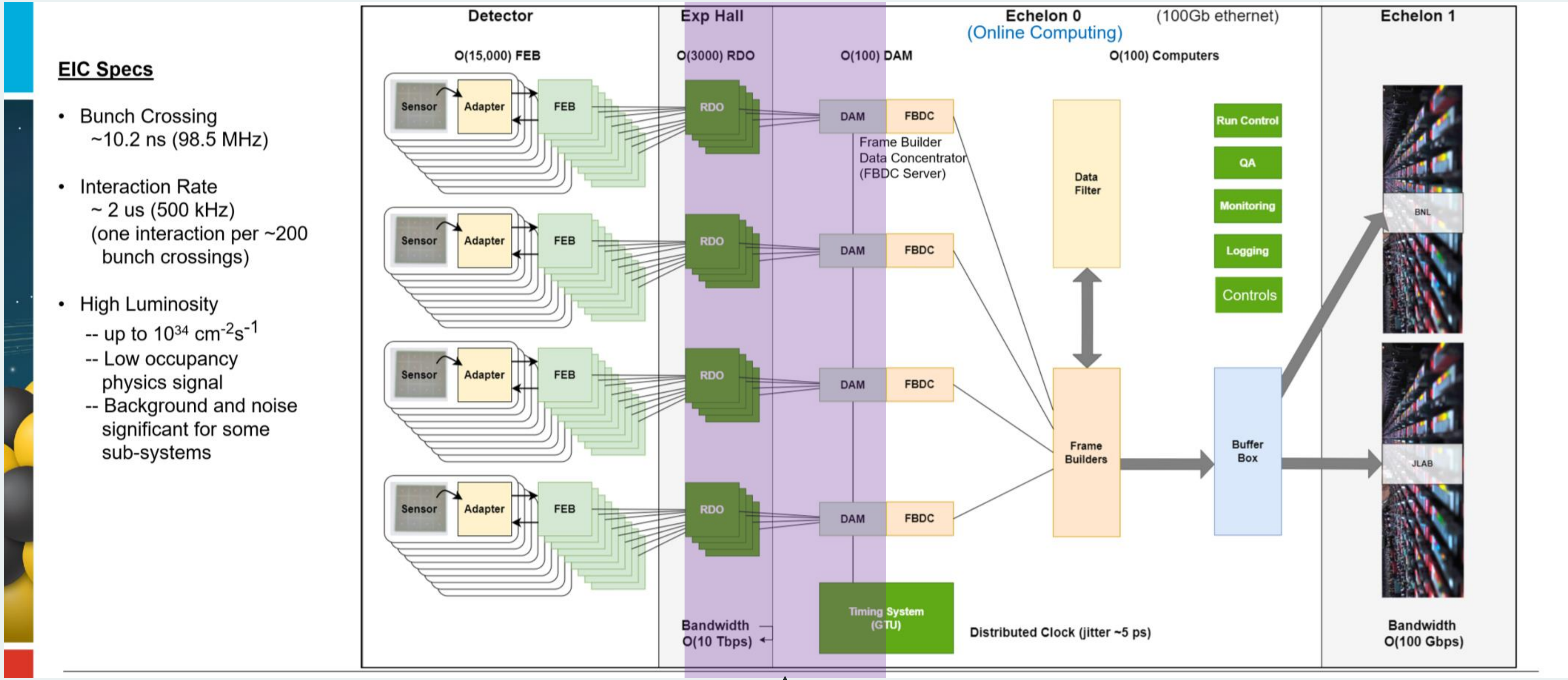
COMPONENT	NOTE/VERSION
FLP	1.26.0
PDP	O2PDPSuite/epn-20240329-DDv1.6.4-QCv1.139.0-flp-suite-v1.26.0-1
CTP	ctp: 23_01 ltus: 22_02 sw:32.1.8
QC	1.139

DETECTOR	QC layout (validation)	QC layout (reference)
CPV	validation - run 419	reference - run 372
EMC	validation - run 419	reference - run 372
FDD	validation - run 419	reference - run 372
FT0	validation - run 419	reference - run 372
FV0	validation - run 419	reference - run 372
HMP	validation - run 419	reference - run 372
ITS	validation - run 419	reference - run 372
MCH	validation - run 419	reference - run 372
MFT	validation - run 419	reference - run 372
MID	validation - run 419	reference - run 372
PHS	validation - run 419	reference - run 372
TPC	validation - run 419	reference - run 372
TOF	validation - run 419	reference - run 372
TRD	validation - run 419	reference - run 372
ZDC	validation - run 419	reference - run 372



ePIC OVERVIEW and some considerations.

ePIC DAQ framework (overview)



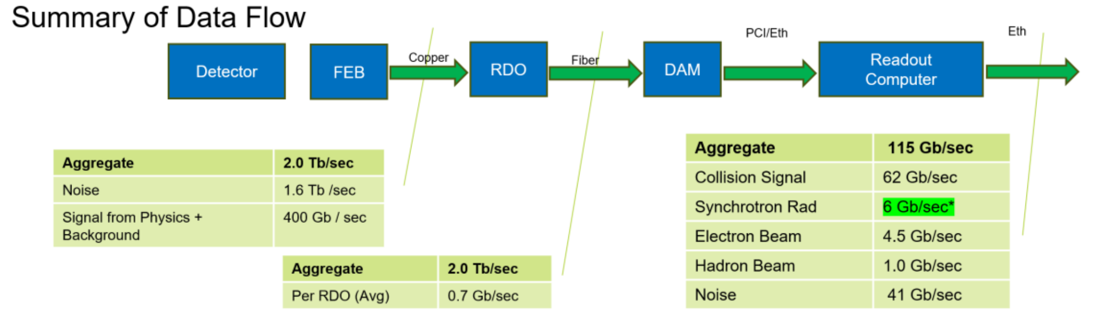
Readout links
I will focus on this part

ePIC DAQ readout links (~4K)

Summary of Channel Counts and Data Flow

Charge 1

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					187	4976	323	323	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364		1364	30	50	12
PID Cherenkov			318k		143k	1334	1334	1242	1334	33	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		3.4k					25	289	11	37	8
Lumi		128k	5.1k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**2,661**	**10,234**	**2,393**	**4,113**	**113**	**1,774**	**109**



Scale of the system:

- **Electronics**
  - ~ 25 detector subsystems
  - ~ 5 Readout Technologies
  - ~ 2500 RDOs (on detector/in racks)
  - ~ 110 DAM boards (DAQ room)
  - GTU (with interface boards)
- **Maximum Data Volume**
  - ~ 2 Tb/sec digitized
  - ~ 115 Gb/sec recorded
- **Online Computing (Echelon 0)**
  - ~200 nodes (DAQ Room/SDCC)

* Synchrotron radiation caveats:

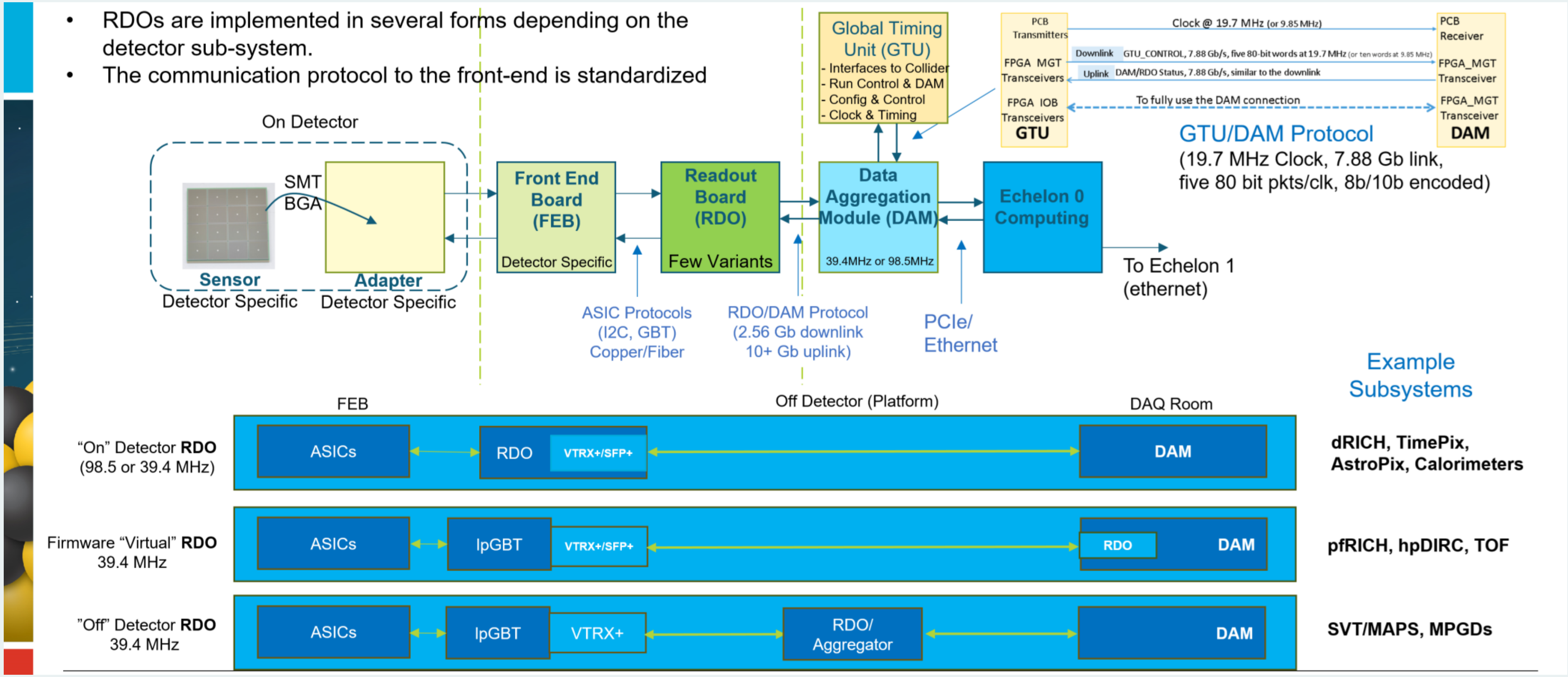
1. Rates are based upon hit rate for all ePIC detectors. In fact, data volumes depend upon specific detector hit (64 bits/hit assumed)
2. Highest Synchrotron radiation / electron beam gas will correspond to lower values for collision signal
3. Plan to analyze by component soon

Fiber Pair (DAQ)
323
160
522
1364
1334
80
289
41
build on
4,113

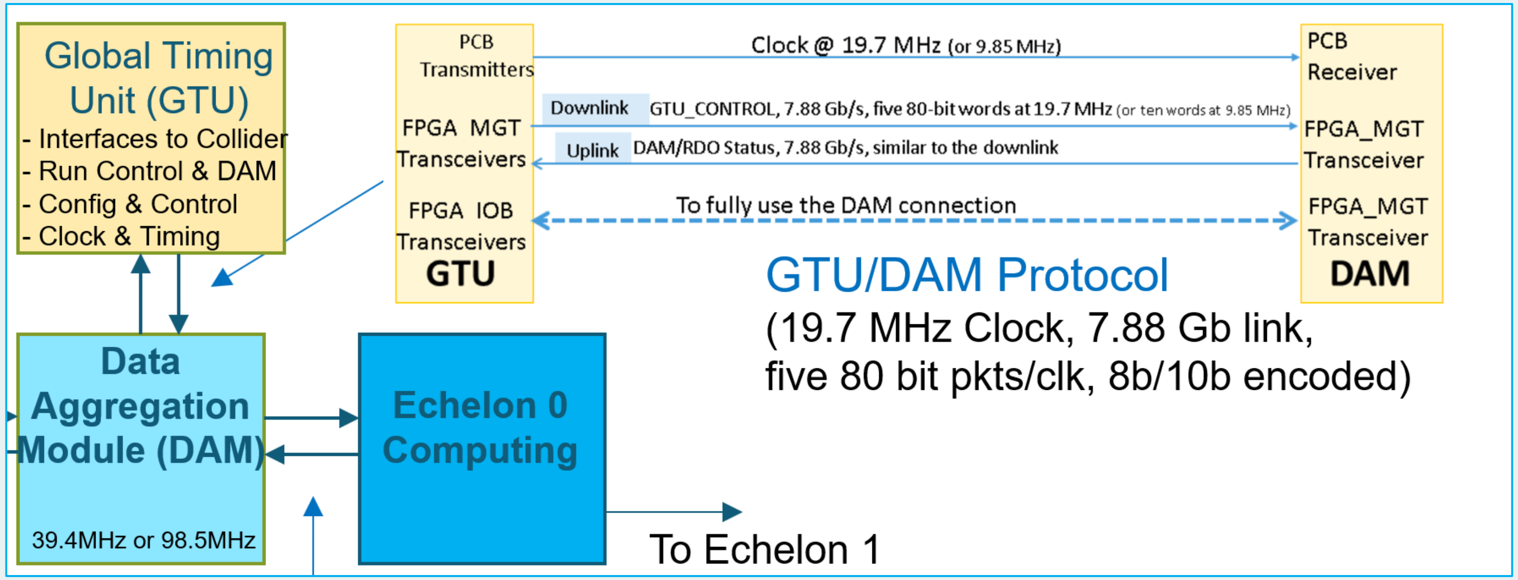
ACRONIMS:

- **RDO** : DAQ readout - FEE interface (aggregator card)
- **DAM** : FELIX-155

DAM control and readout chain options



GTU and DAM communication



Responsibilities and Challenges of the GTU

Multiple Core Functions:

- Acts as the **interface to the machine** to recover the machine clock.
- Handles **Run Control** starts and stops data taking for the DAM.
- Manages **Configuration and Control** of the DAM and/or Front-End Electronics (FEE).
- Provides **Clock and Timing distribution** to ensure synchronized operation across the system.

Key Challenge:

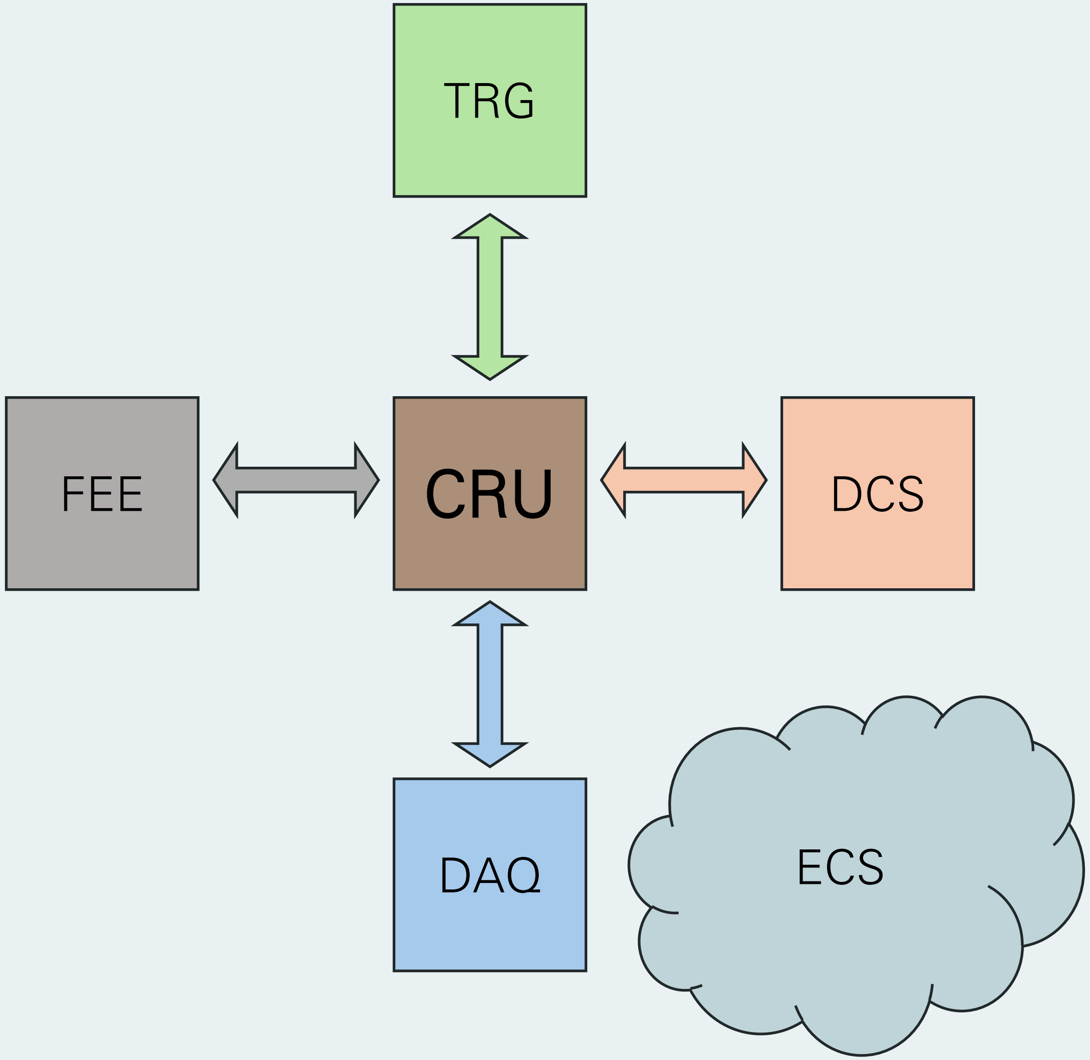
- Concentrating all these critical tasks in a **single entity** increases complexity and risk.
- The GTU's firmware must remain **stable and rarely changed**, since it's responsible for **delivering precise and reliable clock and timing signals** to the entire system.

Who does What?

GTU is a sensitive component in charge to deliver clock and triggers to the whole experiment.
Every changes in the firmware might bring:

- New timing.
- Instability in the system.
- Clock stability is directly connected to the FEE link stability.
- Run control and DAM configuration often requires access to large database.
- It is important that you change this firmware as little as possible.

ALICE central systems



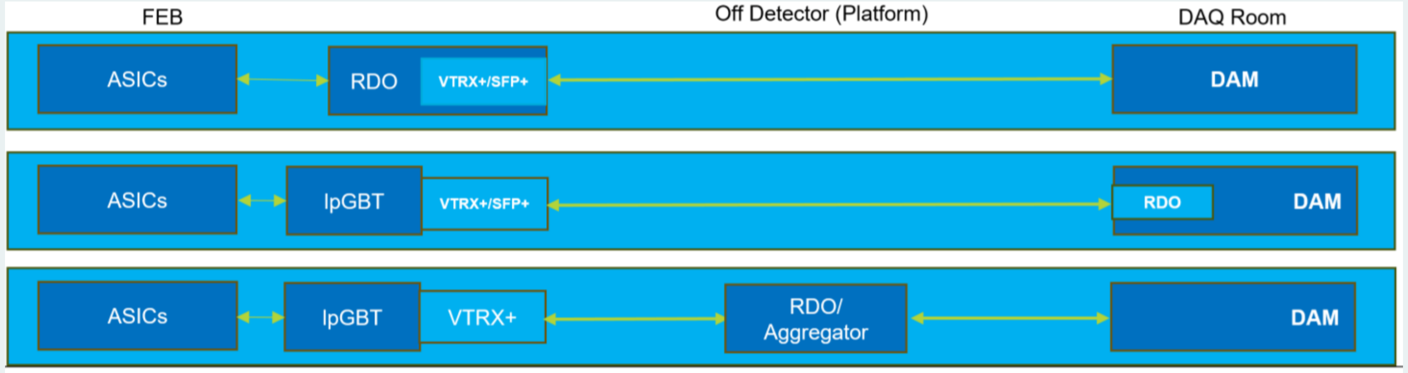
TRG
- Clock and trigger.

DCS
- Slow control information.

DAQ
- Card configuration and data taking.

ECS (Experiment Control System)
- Coordinates all the components to start in the correct order:
  1. DCS (FEE configuration).
  2. DAQ (readout card con.
  3. TRIGGER.
  4. FEE start to generate data.

Readout Configurations



1.

2.

3.

ePIC is evaluating **three different readout configurations**.

Option 2:

The **link protocol is clearly defined.** It uses **lpGBT** or an **FPGA-based implementation** on the readout card. The **connection with the readout system** is therefore well established.

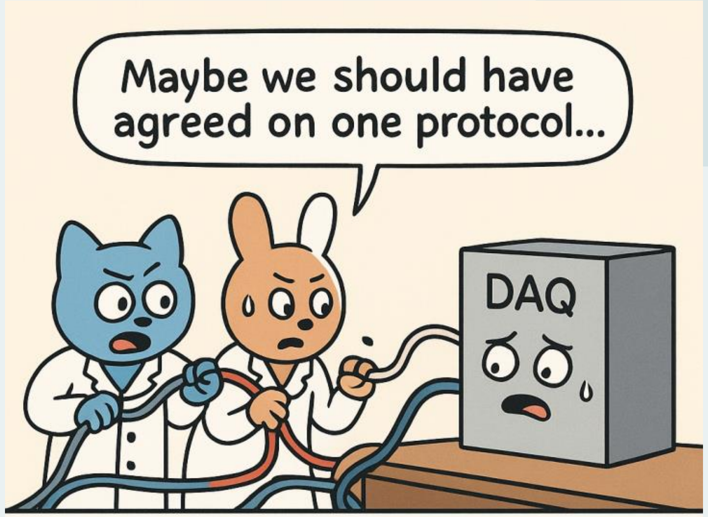
Already provides **protocols for data delivery, slow control, and trigger communication** between the FEE and the readout card.

Options 1 and 3:

The **link protocol is not yet defined**.

This uncertainty will have a **major impact** on implementing other essential protocols, such as **slow control** and **trigger information transfer**.

Impact of Link Protocol Flexibility



High flexibility in link protocols introduces several challenges:

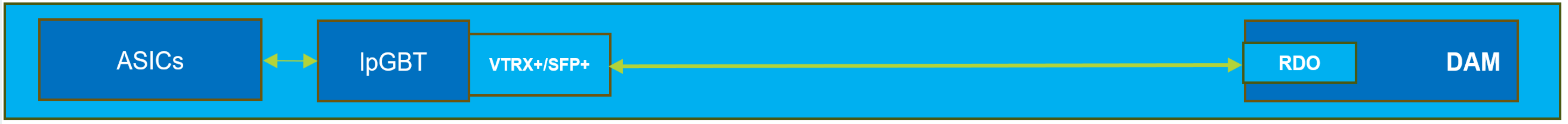
- Increases implementation complexity.
- Reduces issue reproducibility and complicates code maintenance.
- Affects FPGA resource utilization across different designs.

Recommendation:

Standardize communication protocols between the FEE and DAQ as much as possible.

Adopt different or custom approaches only when specific requirements justify the deviation.

Flavors of firmware

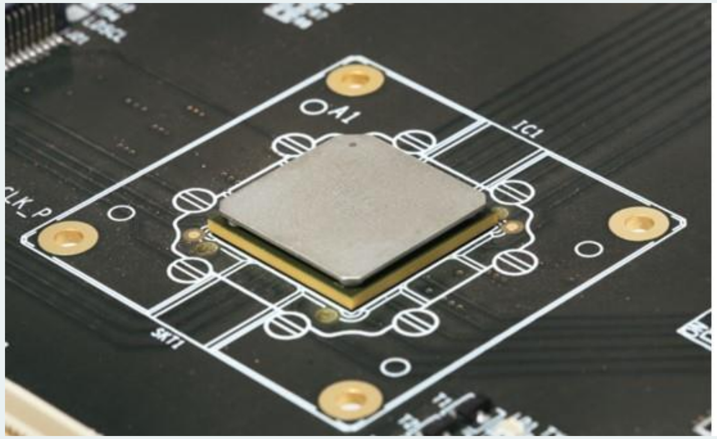


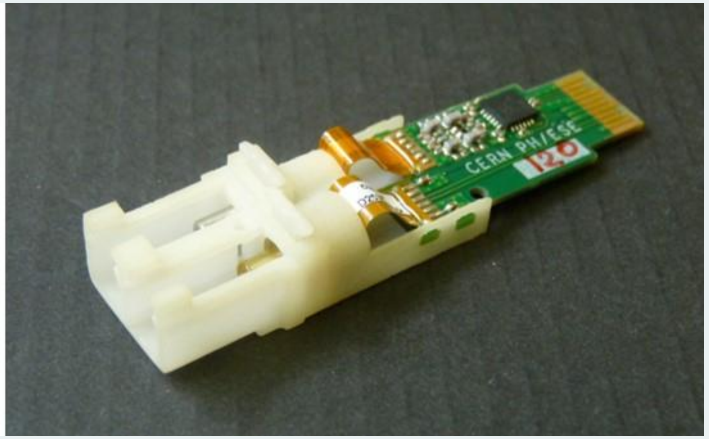
The DAM FIRMWARE is YOUR responsibility !!!!

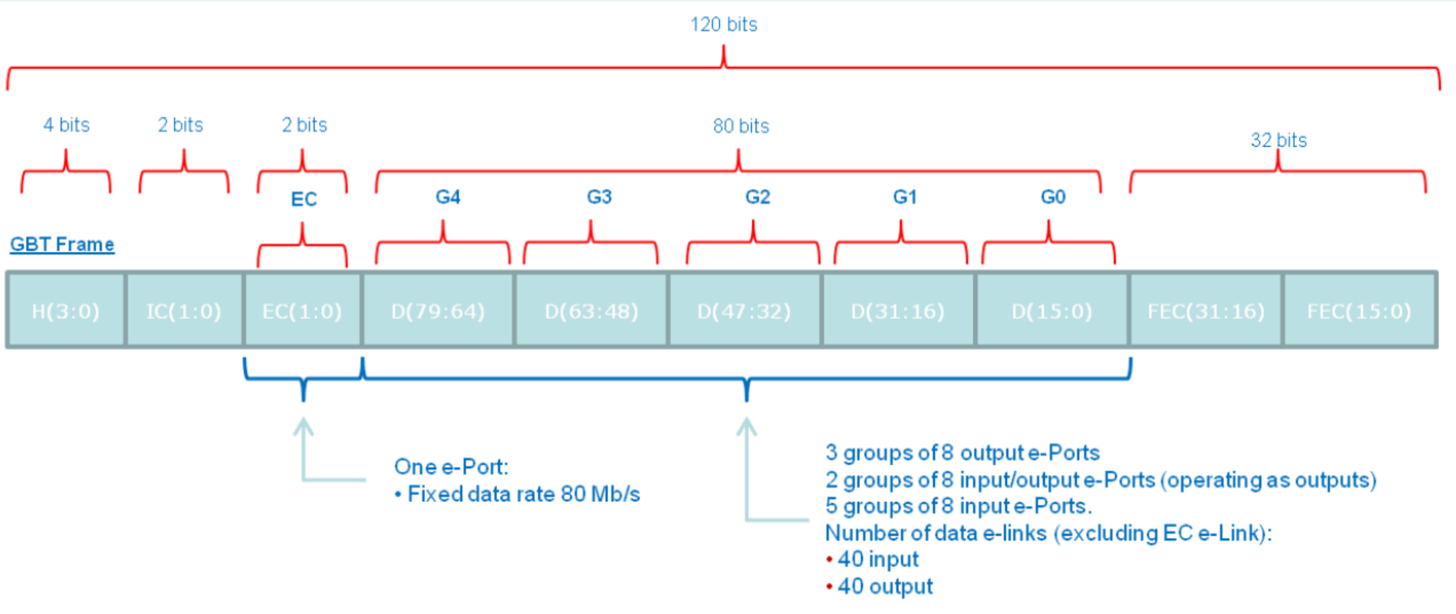
The RDO in the DAM implies that detector firmware will be implemented in the general framework of the DAM. You need to put in place a strategy to compile and test the different firmware flavors:

- Git submodules.
- Fw versions to compile (different versions can generate different results).
- Timing errors !!!

DAQ protocols (GBT VTRX)



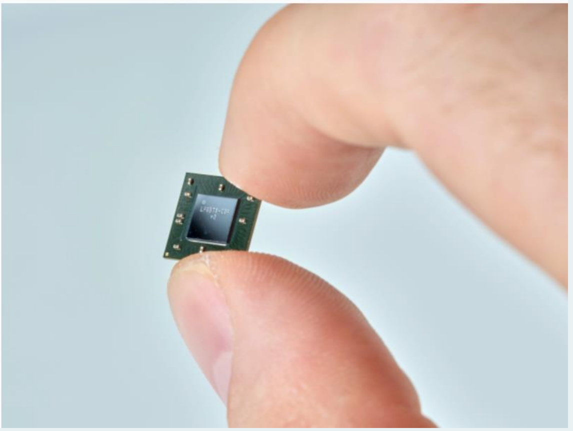


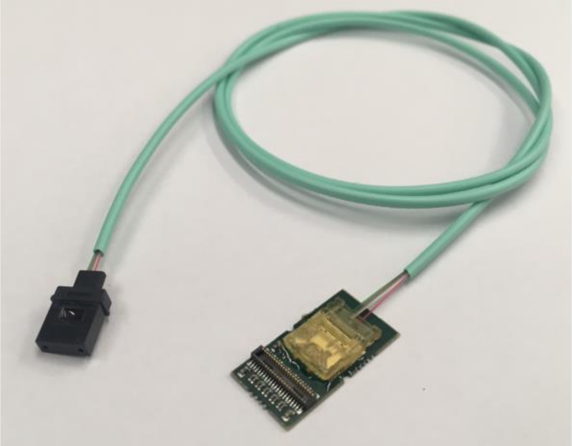


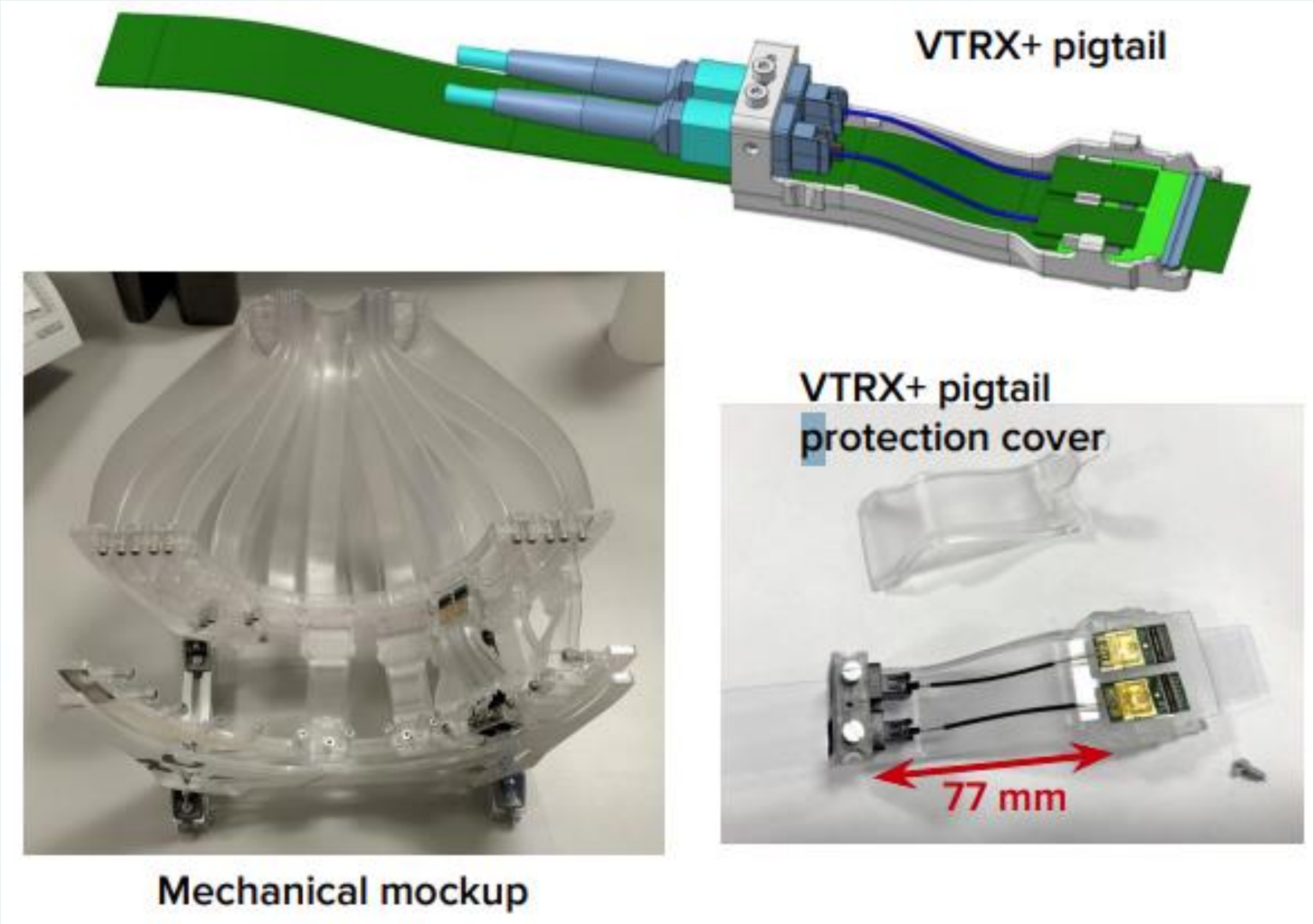
Line rate 120 bit @ 40MHz = 4.8 Gb/s

- 80 bit * 40 MHz = 3.2 Gb/s
- 112 bit * 40 MHz = 4.48 Gb/s
- 4 bit of SC (IC/EC)
  - IC : used to configure the GBT chip.
  - EC : requires SCA chip (provides general I/O and I2C interfaces).
- ALICE SWT protocol (80 bit of DATA are used).

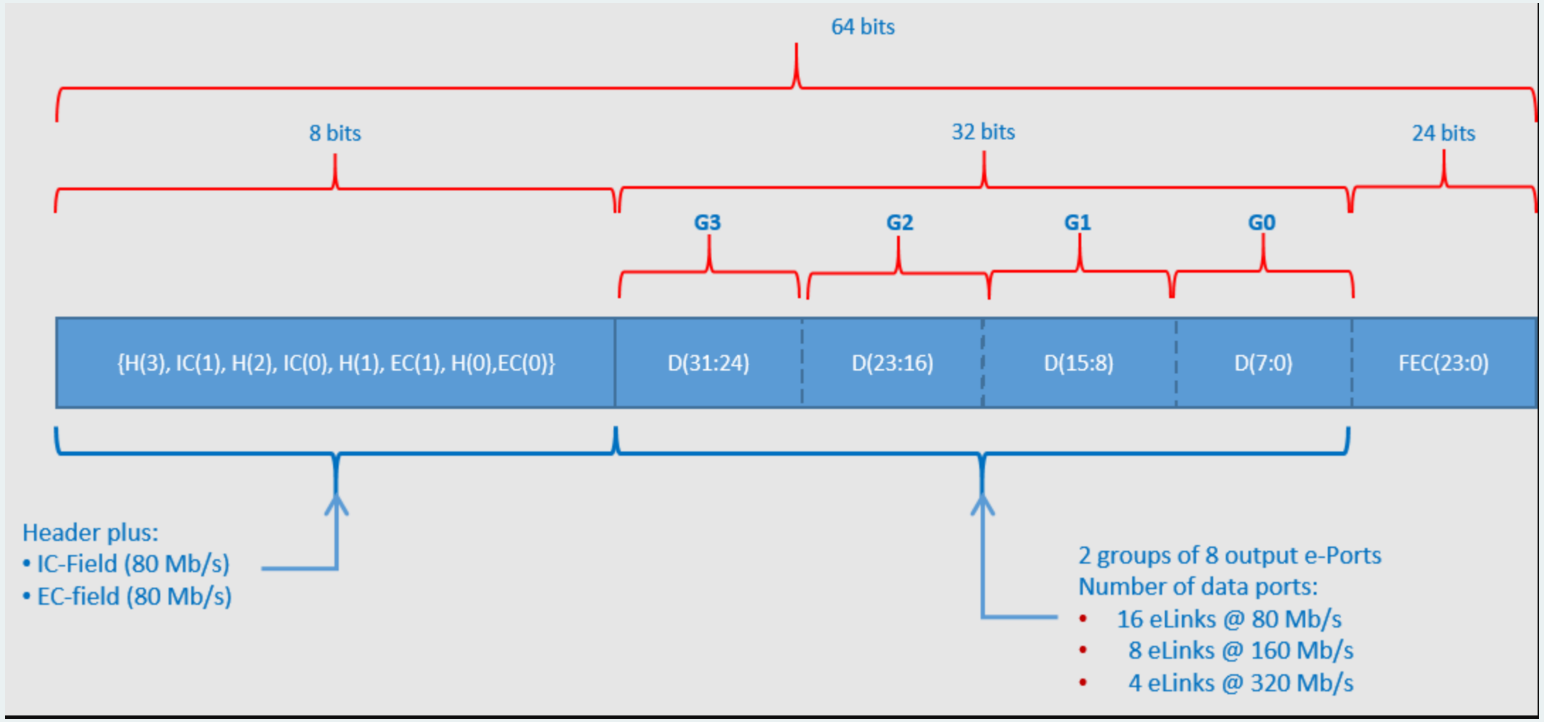
DAQ protocols (lpGBT VTRX+)







DAQ protocols (DAM to RDO)



Line rate 64 bit @ 40 MHz = 2.560 Gb/s
DATA rate 32 bit @ 40 MHz = 1.280 Gb/s

DAQ protocols (RDO to DAM)

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

ASYMMETRIC LINK RATE !!!

A lot of options available, do you need all of them?
Reducing the choice will simplify the implementation in FPGA and the sw to configure the cards.

GBT / lpGBT

	GBT	Data width	lpGBT	Data width
Upstream	3.2 Gb/s	80 bit	1.280 Gb/s	32 bit
Downstream	(GBT) 3.2 Gb/s	80 bit	(5Gb/s FEC12) 3.84 Gb/s	96 bit
	(WB) 4.48 Gb/s	112 bit	(5Gb/s FEC5) 4.48 Gb/s	112 bit
			(10Gb/s FEC12) 7.68 Gb/s	192 bit
			(10 Gb/s FEC5) 8.96 Gb/s	224 bit

HARDWARE SELF TEST !!!

In the CRU, we implemented several **self-test features** by placing the links in loopback mode. Since the TX and RX link rates were identical, the transmitted data could be read back and verified.

This allowed us to:

- **Read back the trigger stream.**
- **Send data (simulating detector output) and read it back** – useful for stressing and validating the full dataflow.
- **Verify the GBT test stream** – including counter and constant pattern checks.

These capabilities were extremely valuable to:

- Validate fiber installation.
- Check firmware functionality.
- Confirm proper FEE operation and clock recovery.

Limitations with lpGBT

With lpGBT, most of these loopback-based features are no longer available, as TX-to-RX loopback is not supported.

Therefore:

Robust link and dataflow validation tools are essential. when failures arise, it becomes more challenging to isolate whether the issue originates from the readout card firmware or the detector FEE.

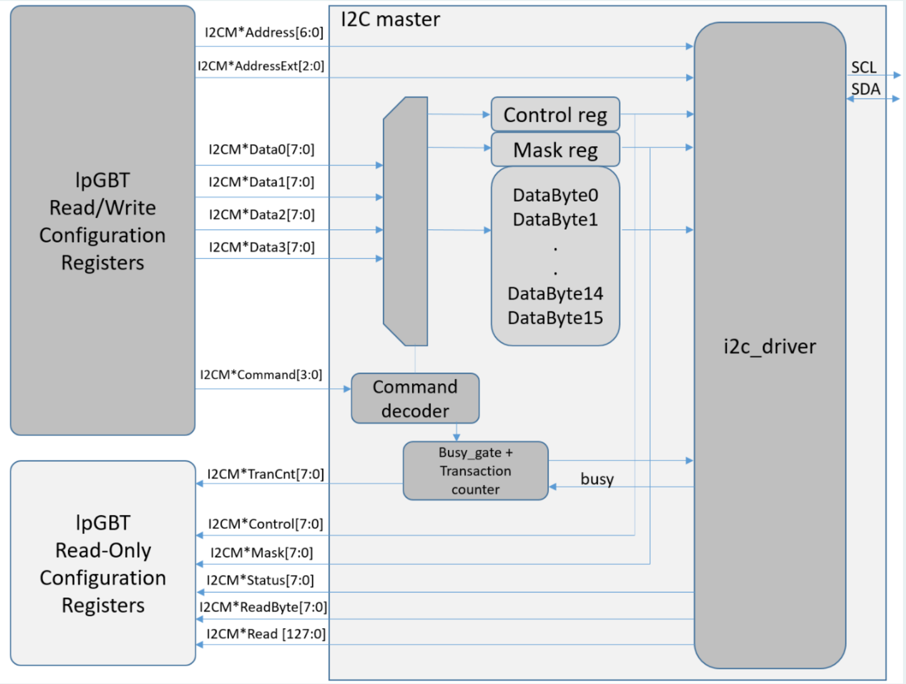
Slow control protocol

The main benefit in using GBT-family protocol is the possibility to send different streams at the same time through 1 fiber:

- Clock.
- Data.
- Slow Control.

To use the SC capability of the GBT/lpGBT protocol you need to have the ASIC on the FEE.
The FPGA implementation is a “simple” parallel to serial interface.

Virtual Vs Real world (HDL Vs ASIC)

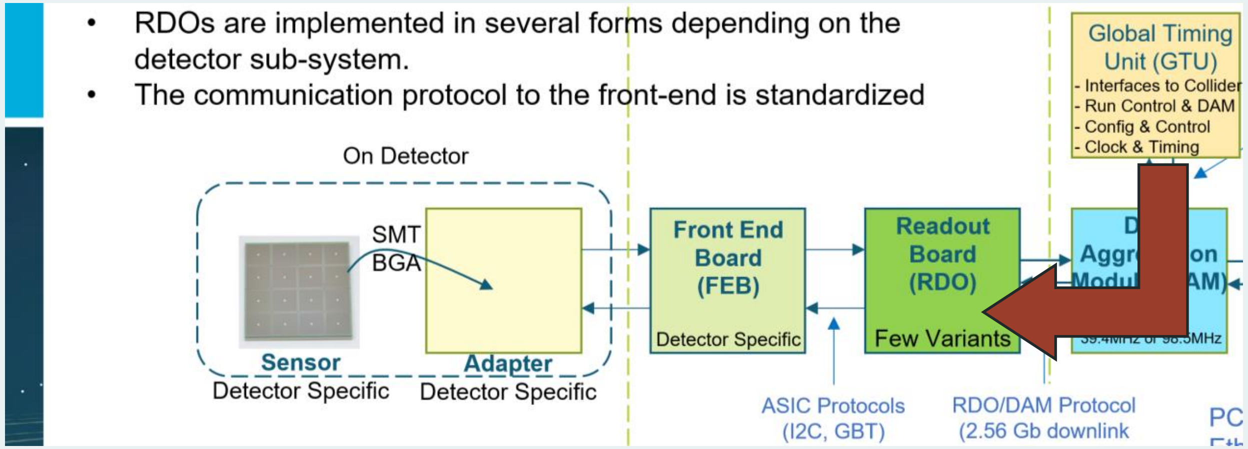



```vhdl
--------------------------------------------------------------------------------
-- gbt_wrapper at base address 0x4_00_0000
--------------------------------------------------------------------------------
cmp_gbt_wrapper : lpgbt_wrapper
    generic map (
        g_CLK_FREQUENCY  => g_CLK_FREQUENCY,
        g_LINKS_PER_BANK => g_LINKS_PER_BANK(15 downto 0),
        g_NUM_GBT_LINKS  => g_NUM_GBT_LINKS
        )
    port map (
        -- User global clock
        ttc_clk240         => ttc_clk240_i,
        ttc_tick           => TICK,

        -- Reset
        gbt_reset_tx       => gbt_reset_tx,
        gbt_reset_rx       => gbt_reset_rx,

        -- Transceiver signals
        mgt_bank_refclk_i  => gbt_refclk(3 downto 0),
        serial_rx_i        => gbt_rx(g_NUM_GBT_LINKS - 1 downto 0),
        serial_tx_o        => gbt_tx(g_NUM_GBT_LINKS - 1 downto 0),

        -- GBT Downlink (CRU -> FE)
        gbt_tx_ready_o     => s_gbt_tx_ready(g_NUM_GBT_LINKS - 1 downto 0),
        gbt_tx_bus_i       => s_gbt_dl_bus(g_NUM_GBT_LINKS - 1 downto 0),

        -- GBT Uplink (FE -> CRU)
        gbt_rx_ready_o     => s_gbt_rx_ready(g_NUM_GBT_LINKS - 1 downto 0),
        gbt_rx_bus_o       => s_gbt_ul_bus(g_NUM_GBT_LINKS - 1 downto 0),

        -- Avalon-MM Slave - PCIe BAR Read/Write access
        s0_clk_i           => SYSCLK,
        s0_reset_i         => CORE_RESET_2CK,
        s0_waitrequest_o   => sx_waitreq(4),
        s0_address_i       => sx_addr(4)(23 downto 0),
        s0_read_i          => sx_rd(4),
        s0_readdata_o      => sx_rddata(4),
        s0_readdatavalid_o => sx_rdval(4),
        s0_write_i         => sx_wr(4),
        s0_writedata_i     => sx_wrdata(4)
        );
```

lpGBT chip provides
- I2C masters
- General Purpose I/O

lpGBT FPGA is a TX/RX SERDES interface.
The IC protocol used to communicate with the lpGBT ASIC works if you have the ASIC on the other side.

Trigger protocol/path (ALICE example)



ALICE trigger information consists of 3 fields

- TTYPE = 32 bit
- BC = 16 bits
- ORBIT = 32 bits

The current assumption is that trigger information will follow the path GTU -> DAM -> RDO -> FEB.
How large is ePIC trigger information?
In ALICE we use the GBT link from CRU to FEE to deliver clock and trigger.

- The trigger format relies on the protocol used to communicate with the FEE.
- GBT and lpGBT payloads (upstream) are different (32 bit Vs 80 bits), so changes in the trigger protocol for the lpGBT detectors are required.

Continuous readout (triggerless) ...

If ALICE is continuous readout (triggerless) why do we talk about triggers?

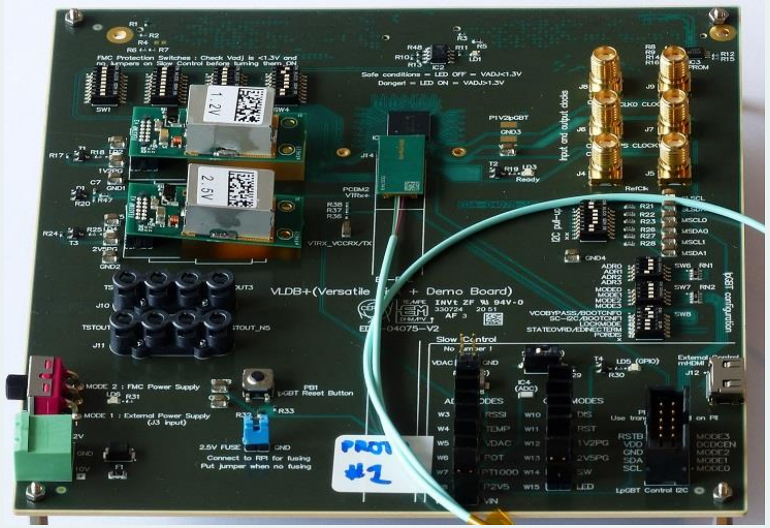
For the dataflow we still need time markers to put data together:

- SOR (Start of Run)
- ALICE marks data between 2 ORBITS with a timestamp so we can put together data from different detectors generated at the same time. (1 ORBIT is 3564 bunch crossing)

ALICE trigger information consists of 3 fields

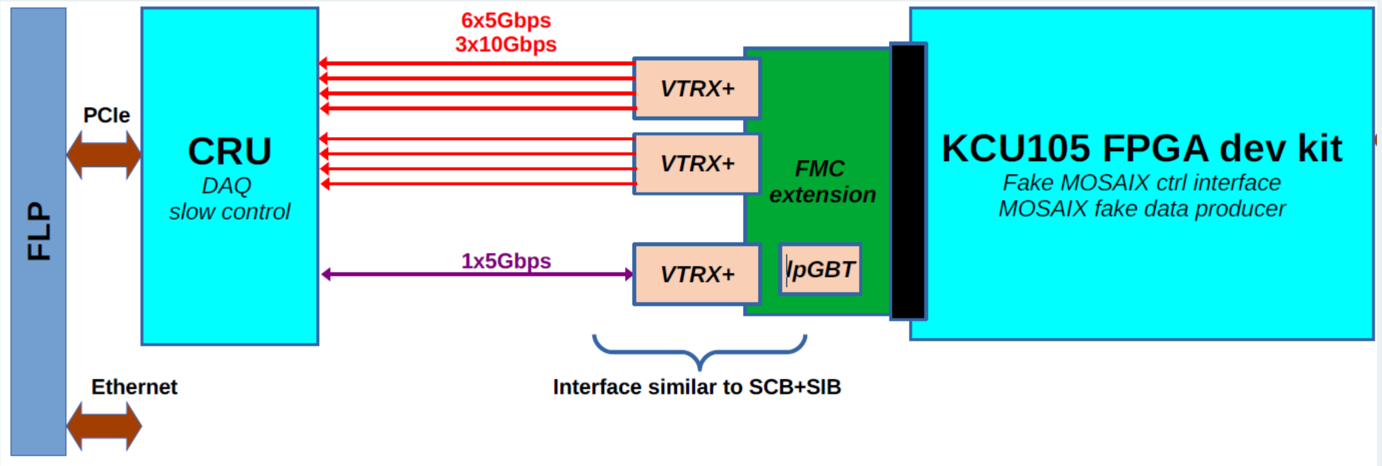
  - TTYPE = 32 bit
  - BC = 16 bits
  - ORBIT = 32 bits

Test bed systems

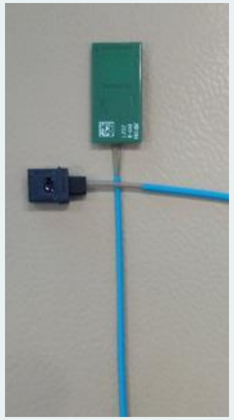


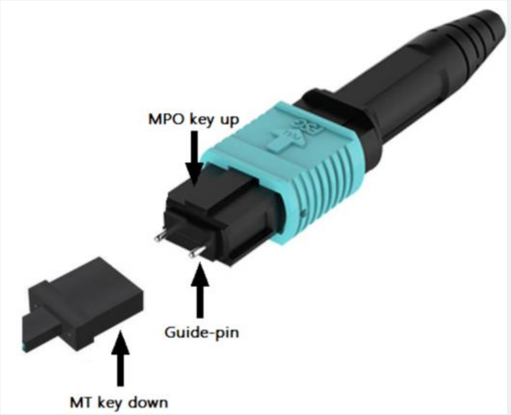
VLDB+ (CERN – ESE)
https://vldbplus.web.cern.ch/

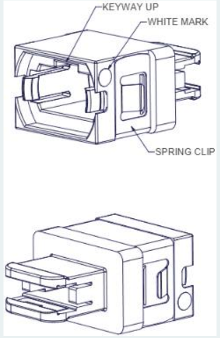
KCU105 + FMC card (GRENOBLE)

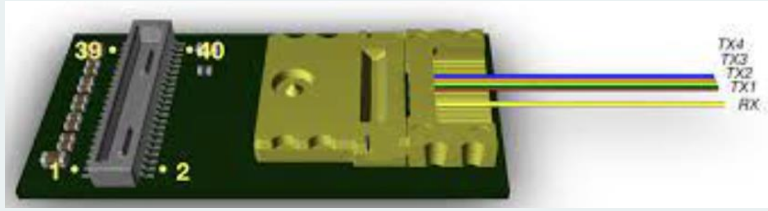


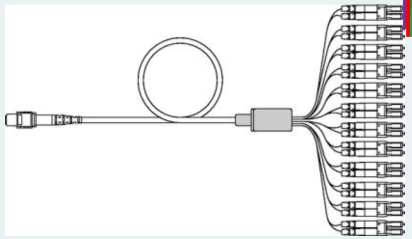
Fiber connections

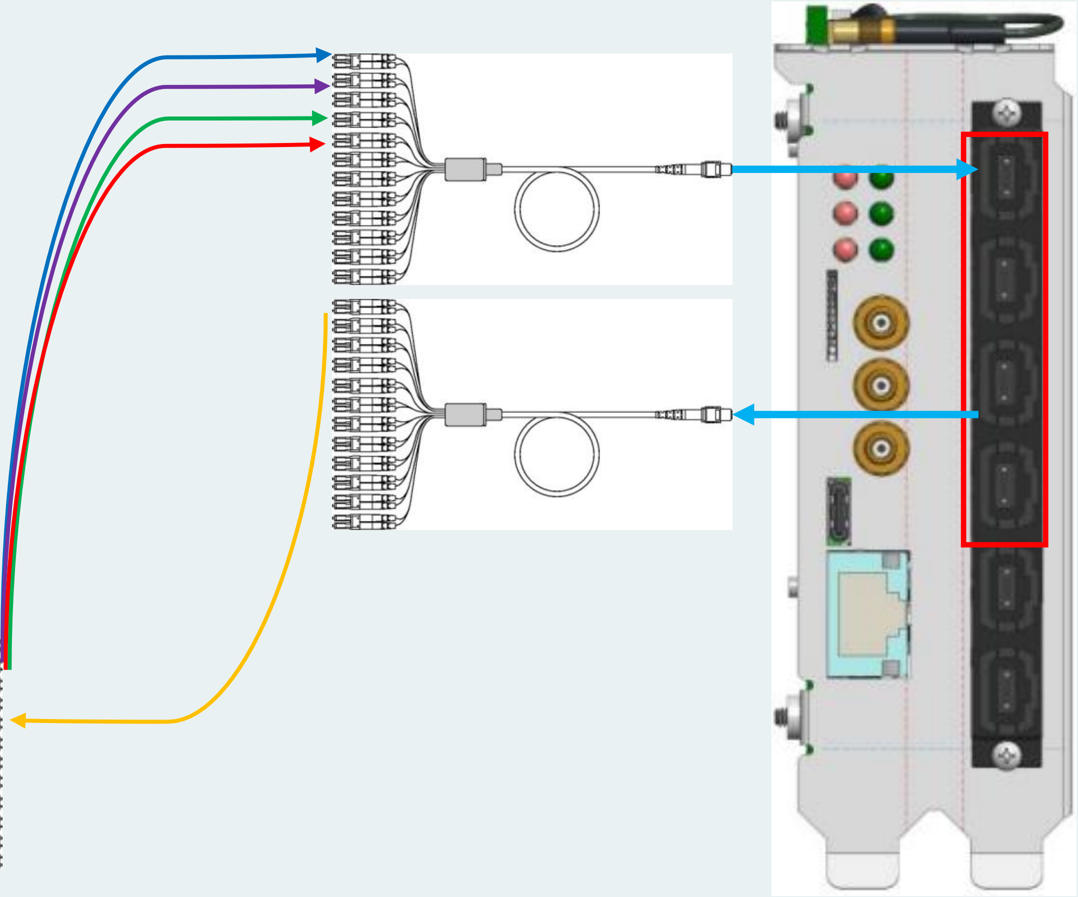


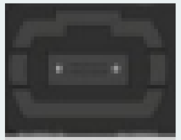












12 ch unidirectional

FPGA resources utilization

FPGA utilization

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

VERSAL premium 1552 production year 2019

CRU Firmware Resource Usage (focal_tb branch, 24 lpGBT link)

Flow Status	Successful - Thu Sep 4 17:19:26 2025
Quartus Prime Version	18.1.0 Build 222 09/21/2018 SJ Pro Edition
Revision Name	cru
Top-level Entity Name	top_cru_lpgbt
Family	Arria 10
Device	10AX115S3F45E2SG
Timing Models	Final
Logic utilization (in ALMs)	147,442 / 427,200 (35 %)
Total registers	269588
Total pins	370 / 960 (39 %)
Total virtual pins	0
Total block memory bits	20,572,652 / 55,562,240 (37
Total DSP Blocks	0 / 1,518 (0 %)
Total HSSI RX channels	41 / 72 (57 %)
Total HSSI TX channels	41 / 72 (57 %)
Total PLLs	59 / 144 (41 %)

24 lpGBT +
16 PCIe +
1 PON

35%

Fitter Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	[A] ALMs used in final placement	Combinational ALUTs	Dedicated Logic Registers
1	|	182264.8 (3.5)	235470 (7)	269584 (5)
1	|auto_fab_0|	3246.5 (1.0)	3301 (2)	6171 (0)
2	|corecmp|	179014.8 (8.9)	232162 (9)	263408 (23)
1	|busmux|	157.2 (157.2)	261 (261)	155 (155)
2	|cmp_bsp|	3069.2 (0.0)	4367 (0)	4198 (0)
3	|cmp_datapath0|	19078.4 (374.7)	21618 (665)	33236 (762)
4	|cmp_datapath1|	19265.0 (377.1)	21618 (665)	33580 (777)
5	|cmp_gbt_wrapper|	74897.0 (22.6)	104028 (36)	100092 (54)
6	|cmp_gbtsc_w|	24211.3 (643.4)	26393 (54)	36390 (2208)
7	|cmp_pciedma0|	16124.2 (0.0)	22919 (0)	23680 (0)
8	|cmp_pciedma1|	16077.7 (0.0)	22745 (0)	22654 (0)
9	|ttcpon_comp|	6125.7 (152.6)	8204 (187)	9391 (350)

ALMs = 74897 / 427200 (17.5%)
ALUT8s = 104028 / 427200 (24.3%)
FFs = 100092 / 1708800 (5.9%)

Implemented lpGBT features:

- Dynamic 5.12 / 10.25 Gbp switch
- Fixed FEC12

ARRIAX production year 2013

CRU firmware development (common)

- Firmware VHDL
- Test tools Python
- Production tools C/C++
  - Driver in C and C/Python library to access the card
- Central GIT repository (firmware and software)
  - https://gitlab.cern.ch/alice-cru/cru-fw.git
  - https://gitlab.cern.ch/alice-cru/cru-sw.git
- Synthesis and firmware file generation via cmd line (make)
- Gitlab issues to keep track of new features
- Branching:
  - Master/develop branch
  - New feature, new branch from develop
  - When feature is tested branch is moved back to develop
  - When ready, develop is merged back to master and then tagged

CRU firmware development (common)

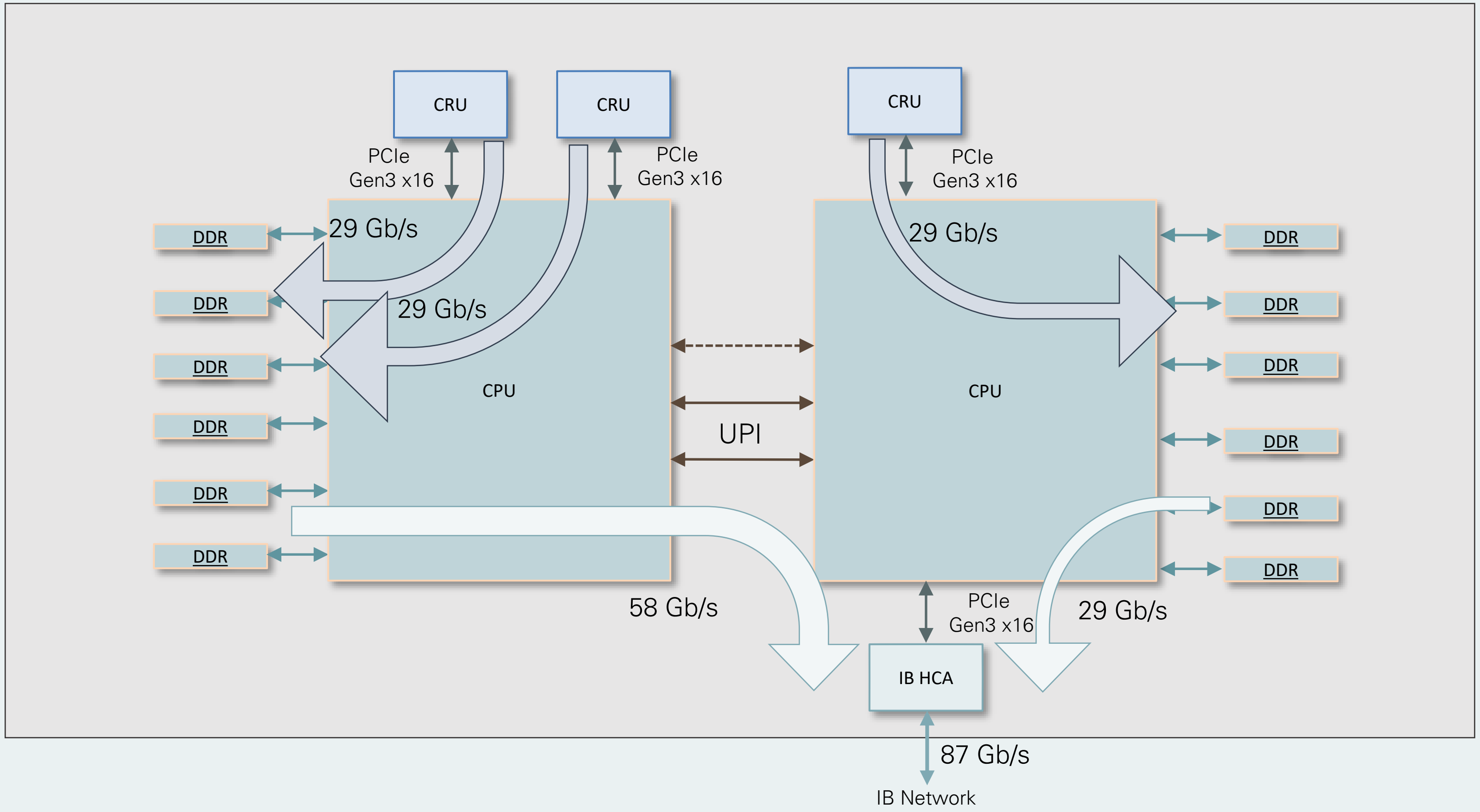
```
roc-list-cards
=====================================================================================
  #   Type    PCI Addr    Serial    Endpoint    NUMA   FW Version       UL Version
-------------------------------------------------------------------------------------
  0   CRU     af:00.0     0277      0           1      v3.19.2          4e41b845
  1   CRU     3b:00.0     0612      0           0      v3.19.2          4e41b845
  2   CRU     b0:00.0     0277      1           1      v3.19.2          4e41b845
  3   CRU     3c:00.0     0612      1           0      v3.19.2          4e41b845
=====================================================================================
```

bifurcation

Common logic

Detector logic

Memory access



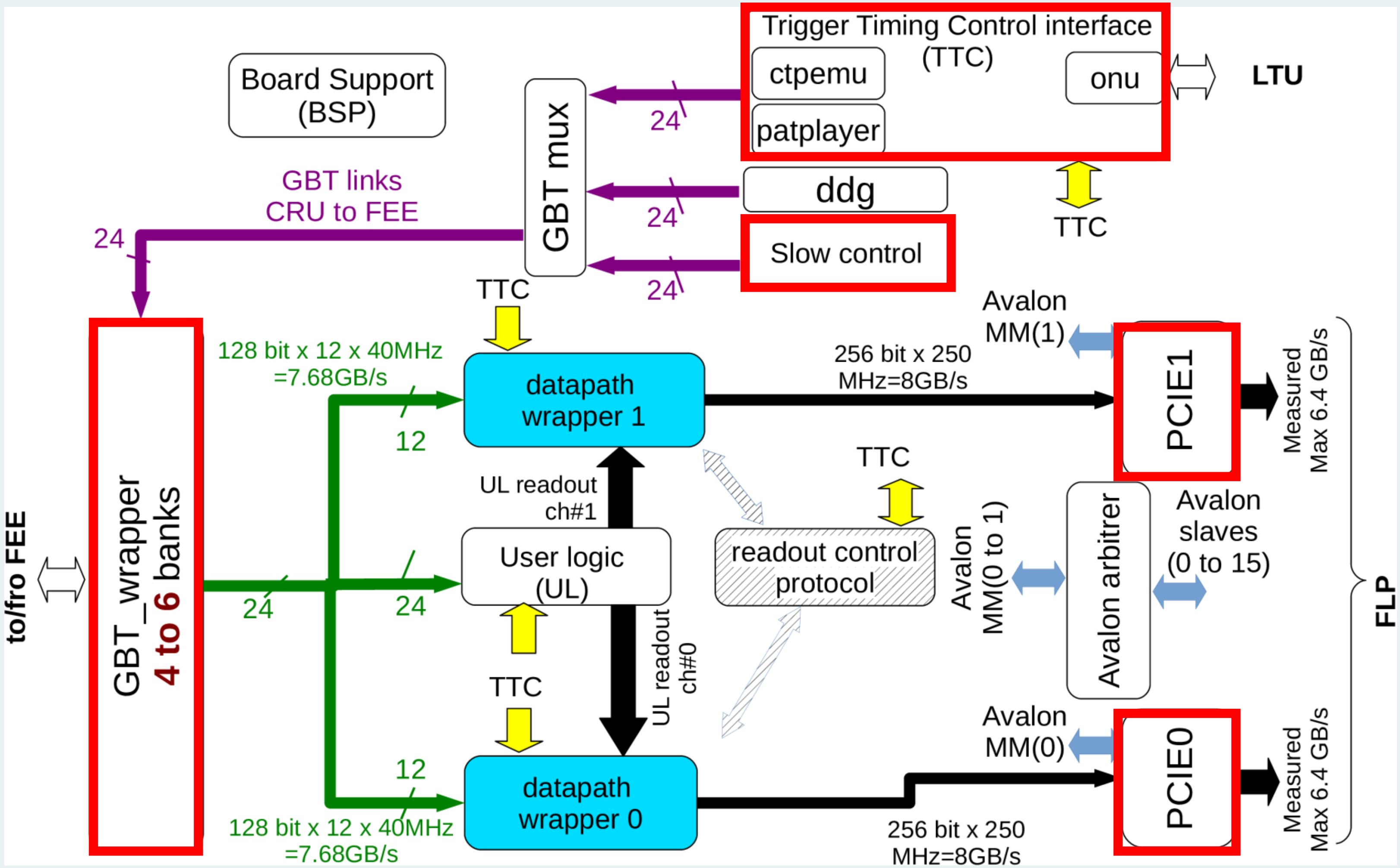
Card position and memory channels equipped in the server, have an impact on the overall performances of the dataflow.

CRU firmware development (detector)

- DETECTOR LOGIC provided in GIT-SUBMODULE.
- CENTRAL firmware compiled including the DETECTOR LOGIC.
- Development flow:
  - Detector experts develop logic and perform test in their lab.
  - Central team compiles the firmware and checks timing results.
  - Collaboration with detector experts is needed in case of errors in timing or dataflow.

```
DETECTOR-UL/
├── CTP
│   ├── hdl
│   └── manifest.qsf
├── DUMMY-UL
│   ├── hdl
│   ├── ip-cru
│   ├── manifest.qsf
│   └── sim
├── ITS
│   ├── CHANGELOG
│   ├── common_logic_hdl
│   ├── doc
│   ├── hdl
│   ├── ip
│   ├── Makefile
│   ├── makefile_vbinfo.mk
│   ├── manifest.qsf
│   ├── quartus
│   ├── README.md
│   ├── requirements.txt
│   ├── scripts
│   ├── sim
│   └── tb
├── MFT
│   ├── hdl
│   └── manifest.qsf
├── MID
│   ├── CHANGELOG.md
│   ├── doc
│   ├── hdl
│   ├── ip
│   ├── manifest.qsf
│   ├── ReadMe.md
│   ├── sim
│   └── software
├── README.md
├── TOF
│   ├── hdl
│   └── manifest.qsf
└── TPC
    ├── cru_tpc_ul.sdc
    ├── hdl
    ├── ip
    ├── Makefile
    ├── makefile_vbinfo.mk
    ├── manifest.org_qsf
    ├── manifest.qsf
    ├── manifest.tcl
    ├── quartus
    ├── README.md
    └── sim
```

Firmware components



ESE:
- GBT/lpGBT.
- TTCPON.
- Slow control.

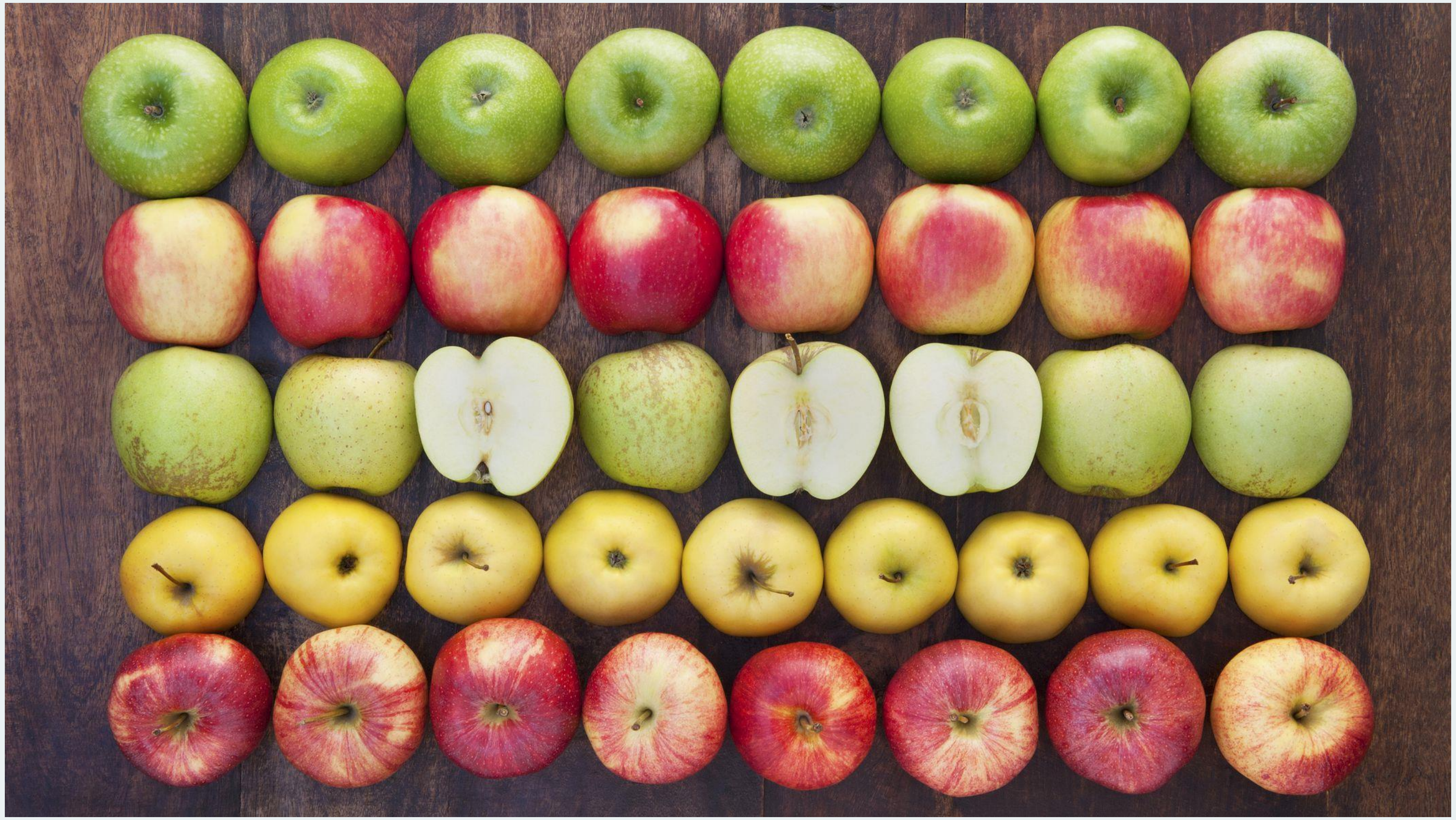
ALTERA/XILINX:
- DMA CORE.

All the other components have been specifically designed to satisfy ALICE data format requirements.

Data processing on the readout card

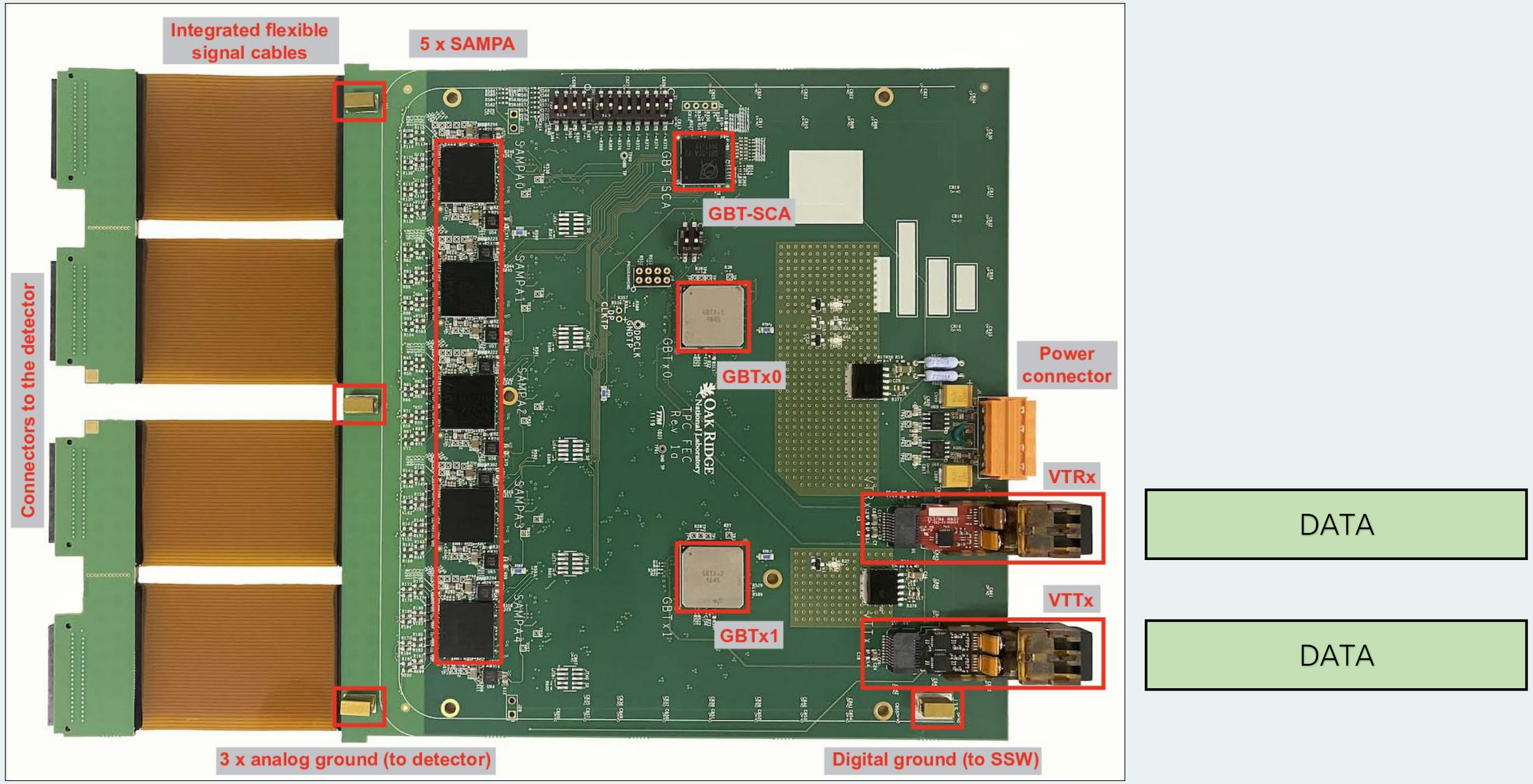
The following results represent my implementation-based assessment of optimal strategies for managing the ALICE dataflow, derived from practical experience rather than a universal reference model.
While other experiments may employ different approaches, these reflect design choices suited to their specific architectures and requirements, not incorrect solutions.

Data processing on the readout card

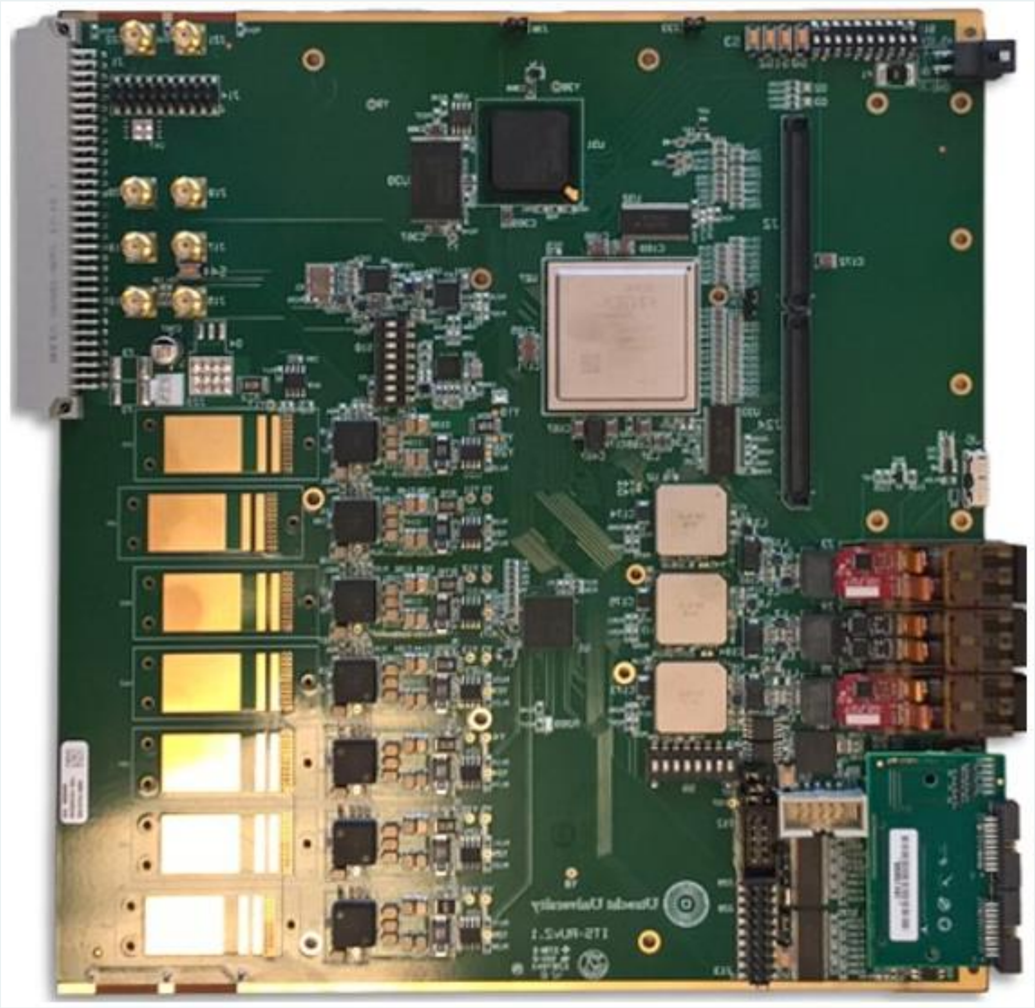


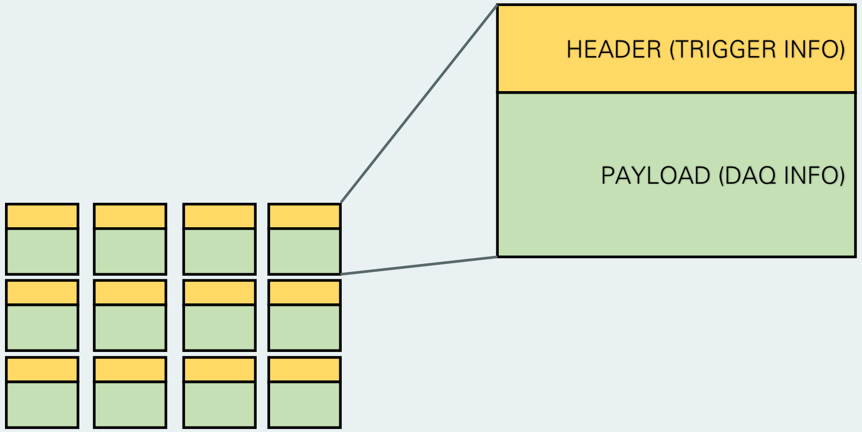
Every detector in ALICE has a different FEE, that are readout by the same card

FEE with ASIC/s (streaming data)

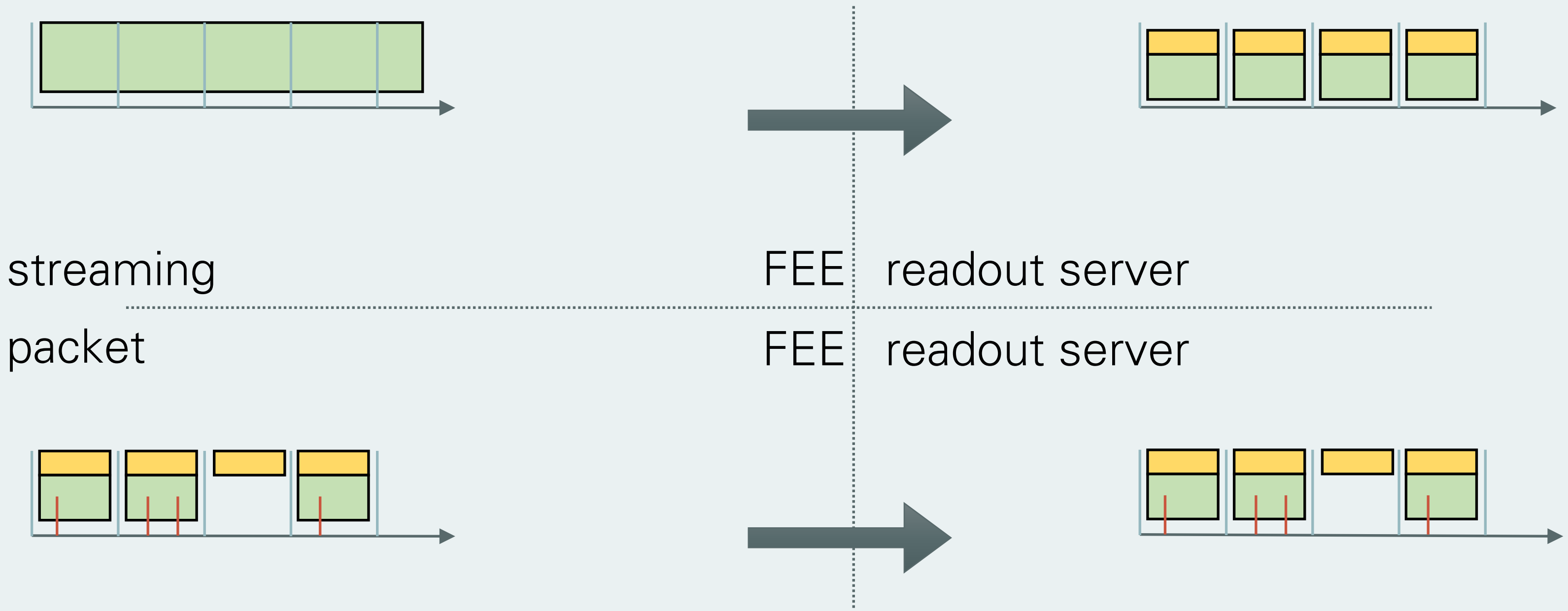


FEE with FPGA/s (packet data)

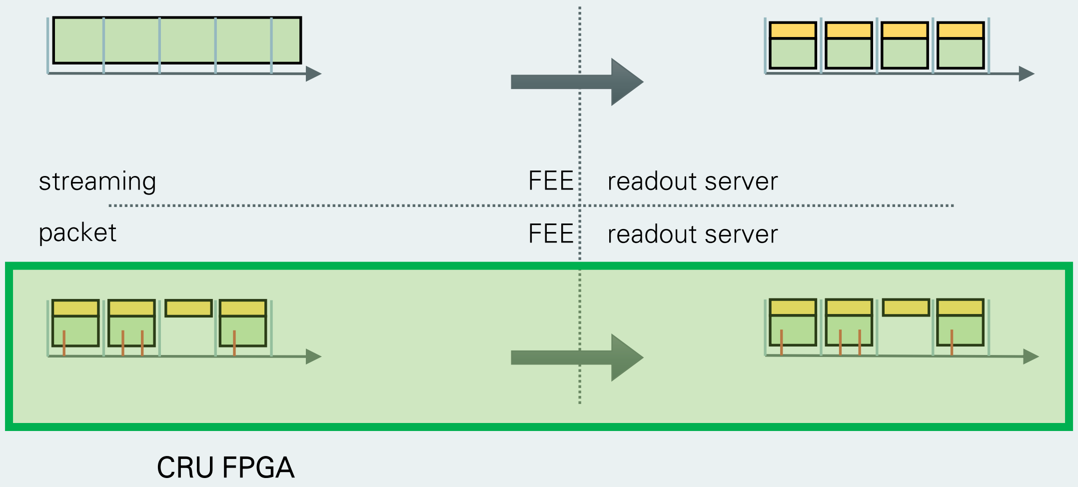




FEE with FPGA/s (packet data)

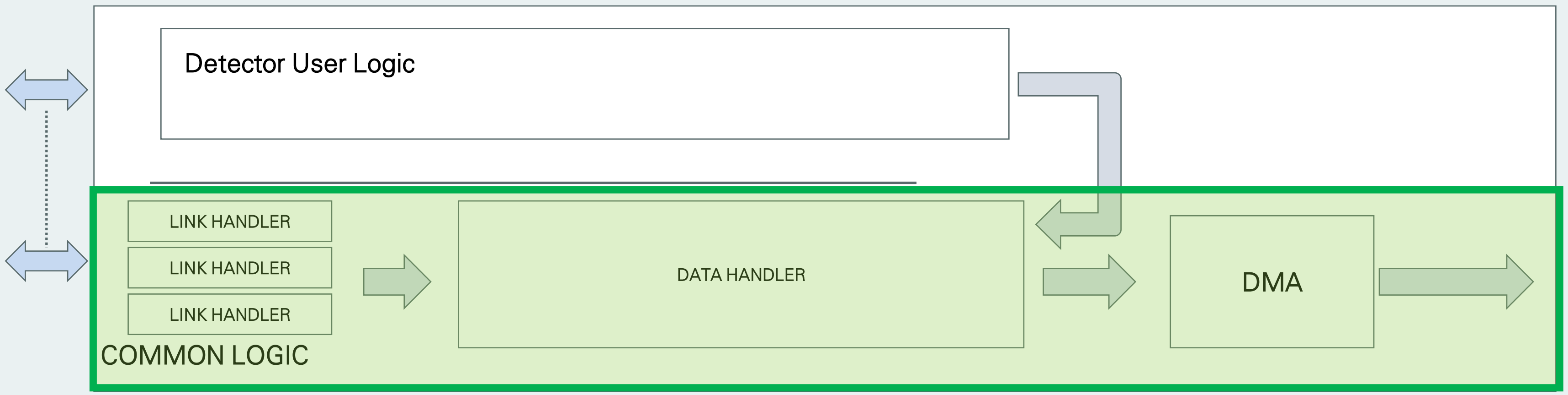


FEE with FPGA/s (packet data)

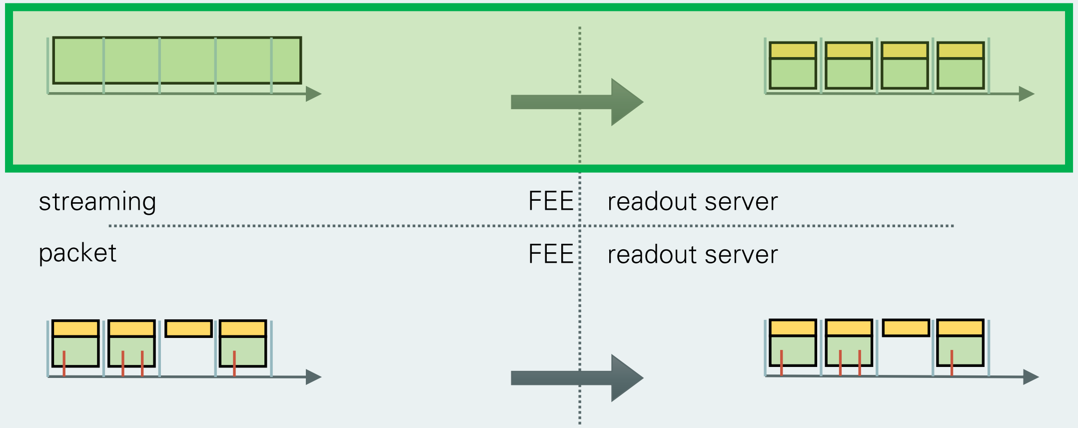


FIRMWARE in VHDL code.
Operations on DATA:

- Check of protocol requirements.
- Data flow balancing.
- Monitoring.
- DMA.

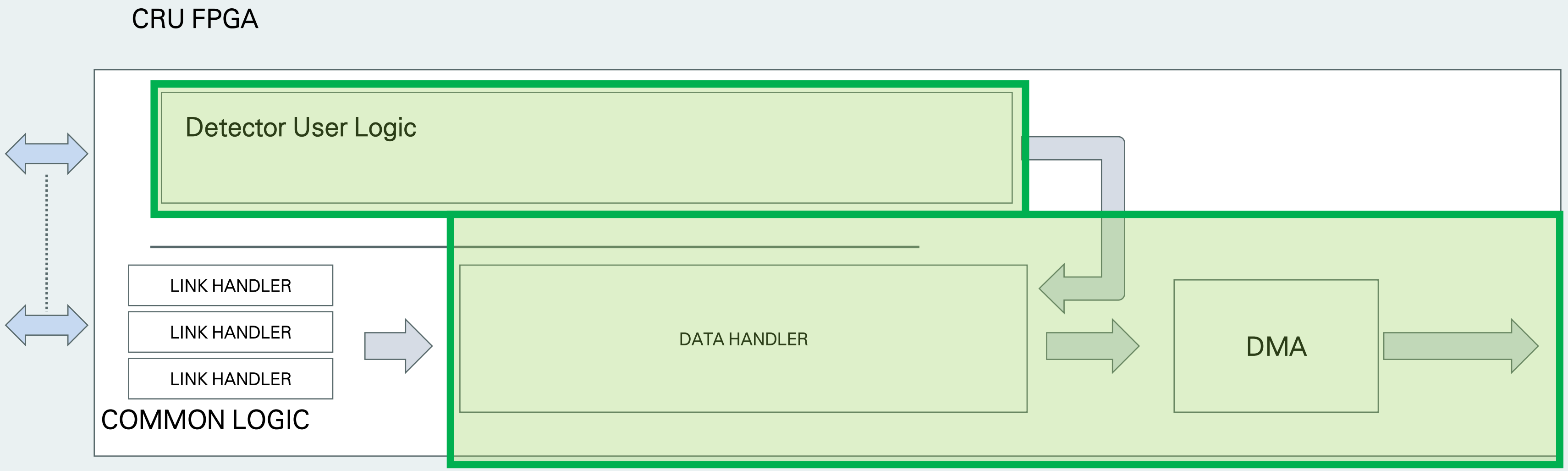


FEE with FPGA/s (streaming data)



FIRMWARE in VHDL code.
Operations on DATA:

- Detector specific code.
  - Zero suppression.
  - Data alignment/synchronization.
  - … data rate reduction.



Use of the DRAM

CRU doesn't have external buffer; the data flow relies on the memory of the server (easily accessible through DMA).

FELIX-155 is equipped with external RAM … should you use it?

Use of the DRAM

- Data selection on FPGA?
- Data buffering?
- … what else

REMEMBER :

- sw is faster to develop/maintain/debug than firmware
- Readout server is usually equipped with large amount of memory (cheaper and easy to access)

Final tips & takeaways

- STANDARDIZATION
- SEPARATION OF PROTOCOLS
- TEST BED
- HARDWARE SELF TEST

A few words of wisdom

- The best is the enemy of the good.
    - Move fast and break things (and fix it soon). Do not wait too much for the perfect feature.
    - Test is asap with the detectors and find out what works and what not.
- Invest time and money on testing facilities (STAGING).
- To ensure early issue detection, shared expertise, and system stability, all experts must begin using the available DAQ system as soon as possible and rely on the same readout chain rather than developing isolated, non-reproducible solutions on custom hardware.

Thank you

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