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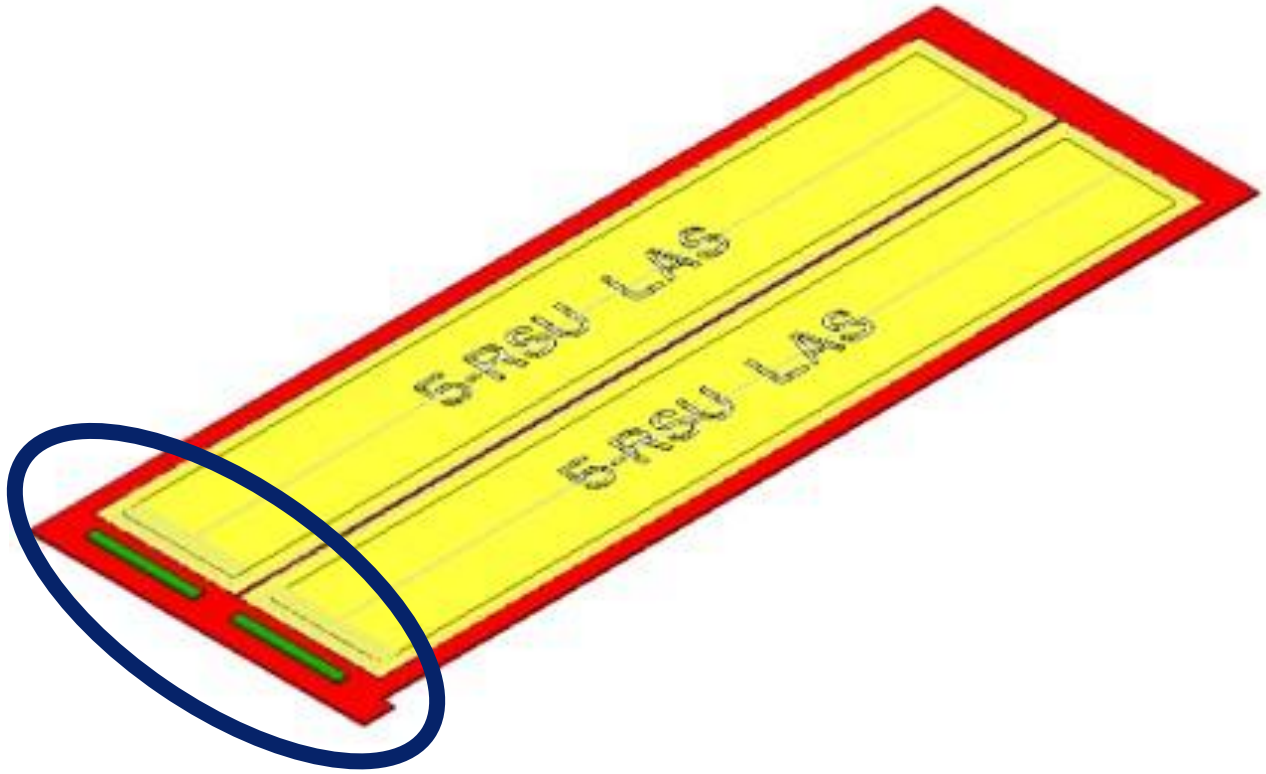
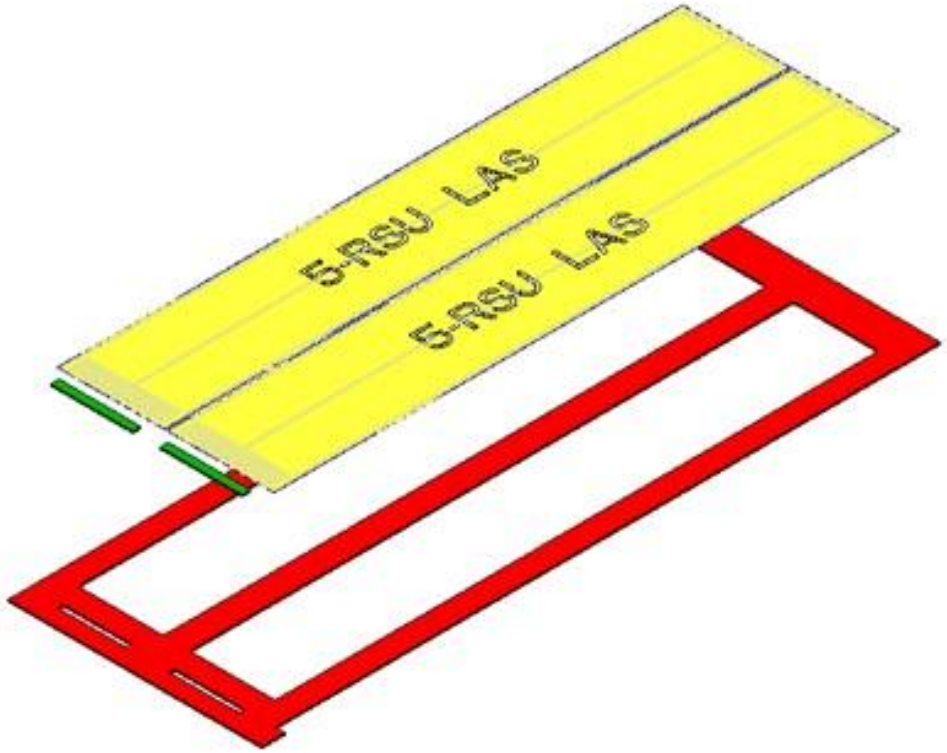
Notes on bridge FPC: Towards a new iteration + AncAsic layout

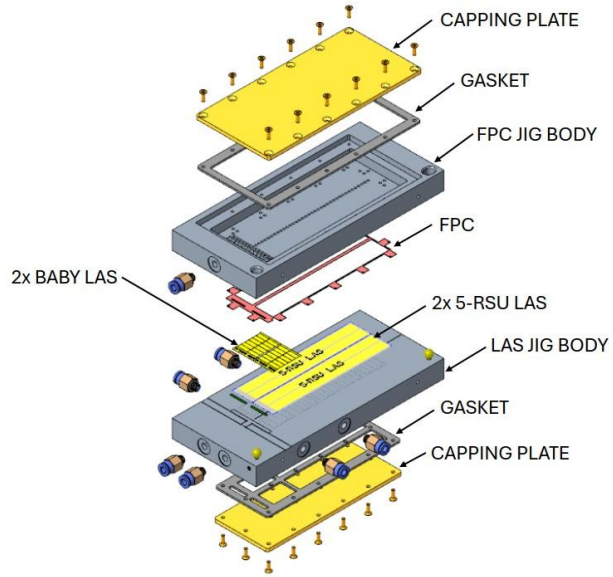
M.Borri

Target module design to date





Reference: James' talk on interconnection considerations:
https://indico.bsnl.gov/event/25702/contributions/99824/attachments/58780/100945/24-11--6_FPC_AncAsicPlacement_Bonding_JJG_ET_r3.pdf



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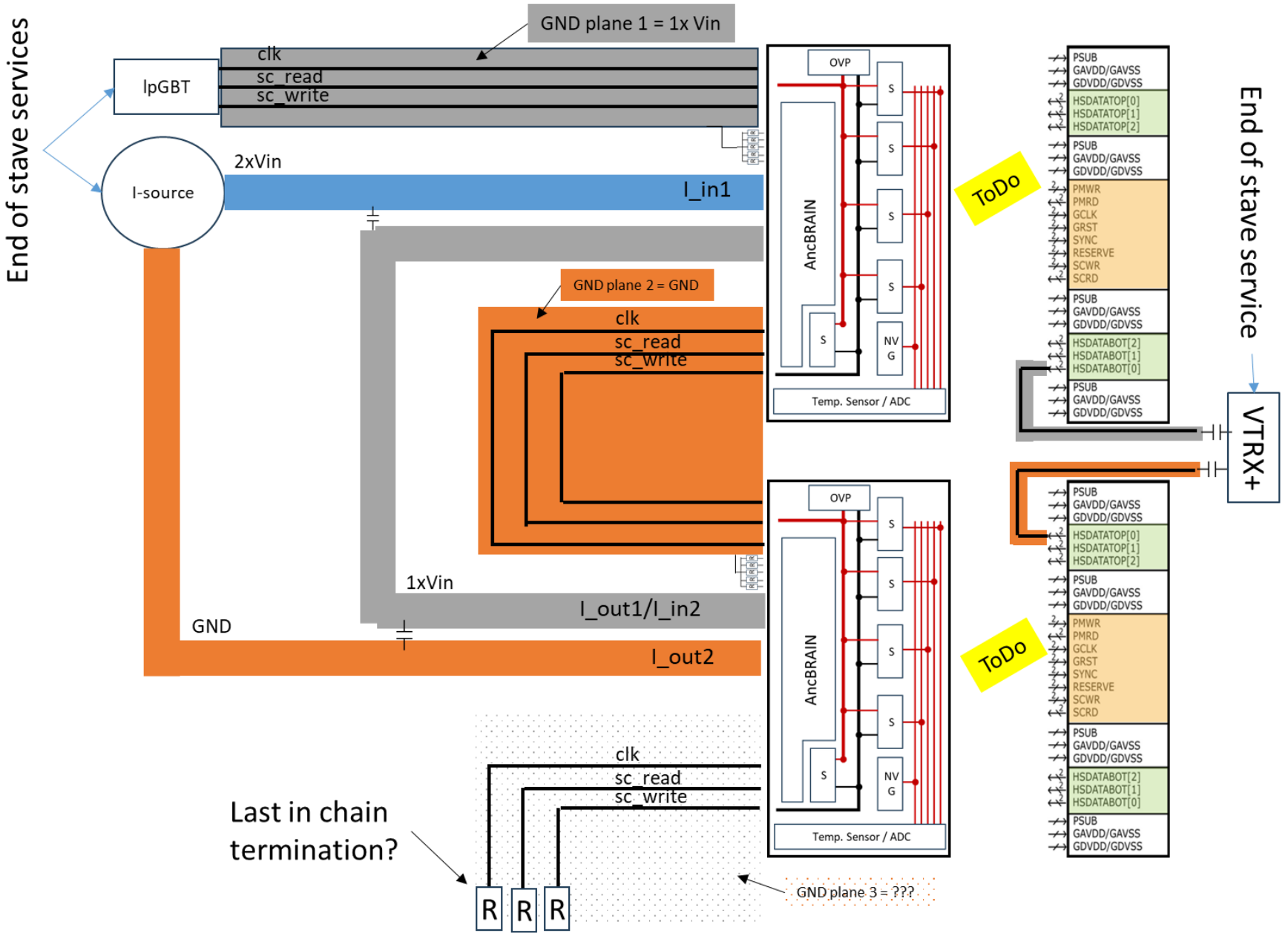
Sanity check on the “end of stave side” of B-FPC

I_in = const

clk, sc_read, sc_write:
AC or DC coupled?



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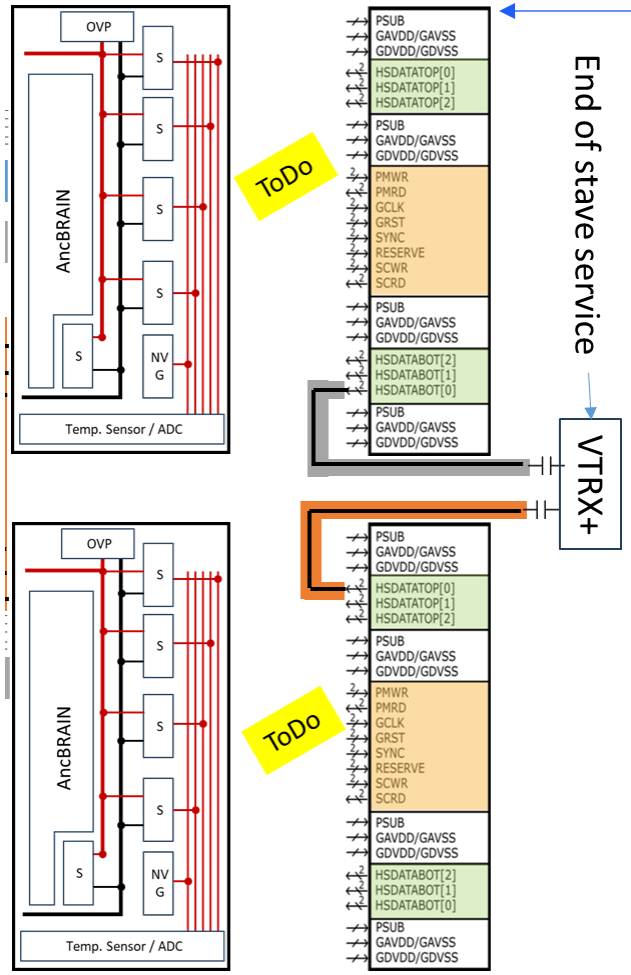
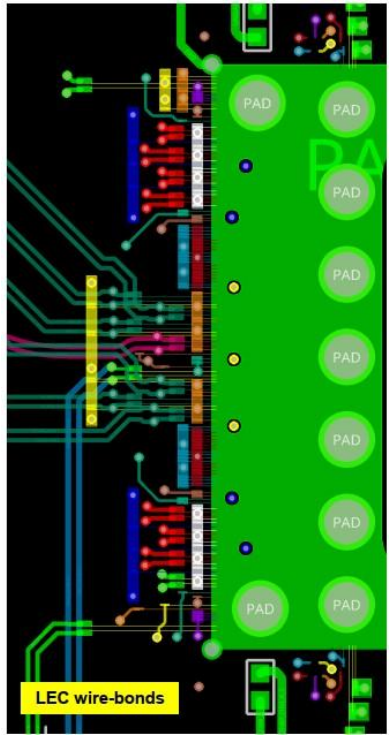
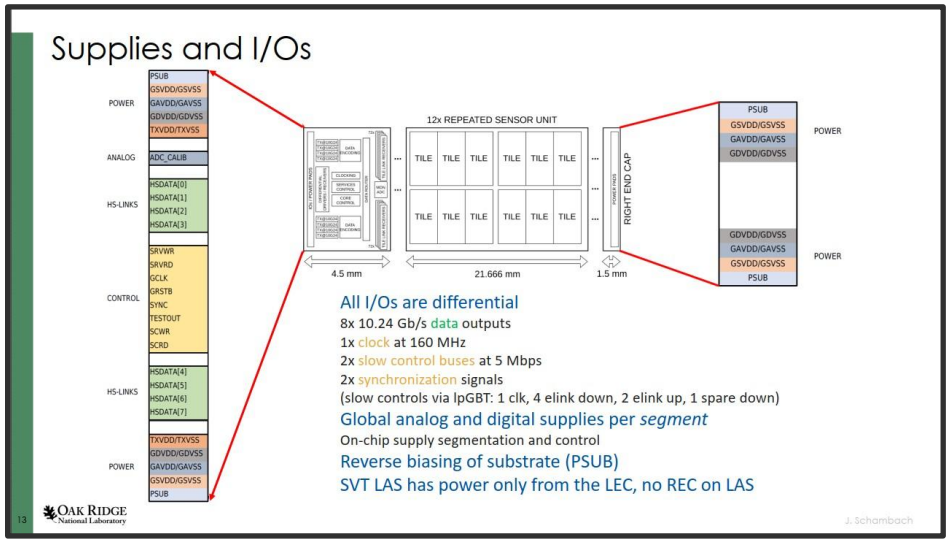
Sanity check on the “LAS side” of B-FPC

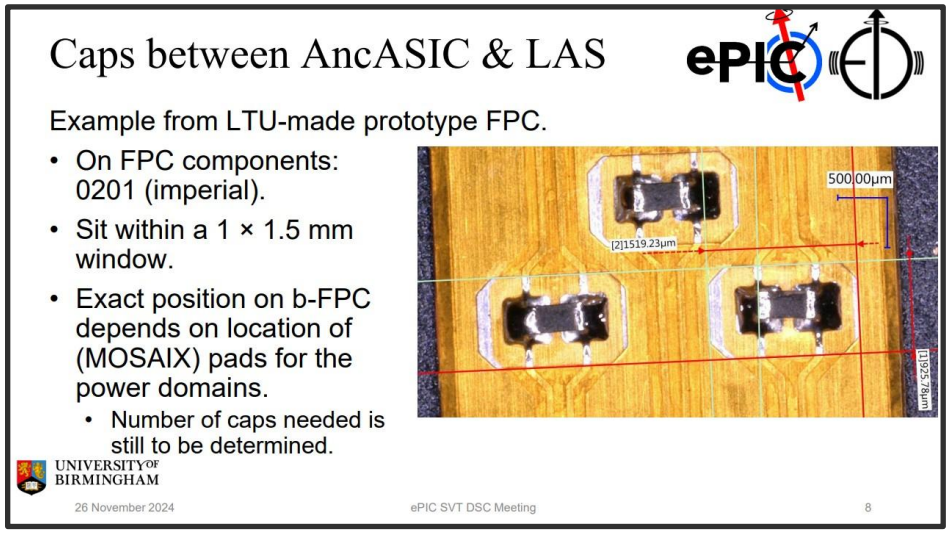


To access real pin out?

M.Borri does not have access to the CERN MOSAIX web page.







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Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analogue	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serialisers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

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Thank you

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