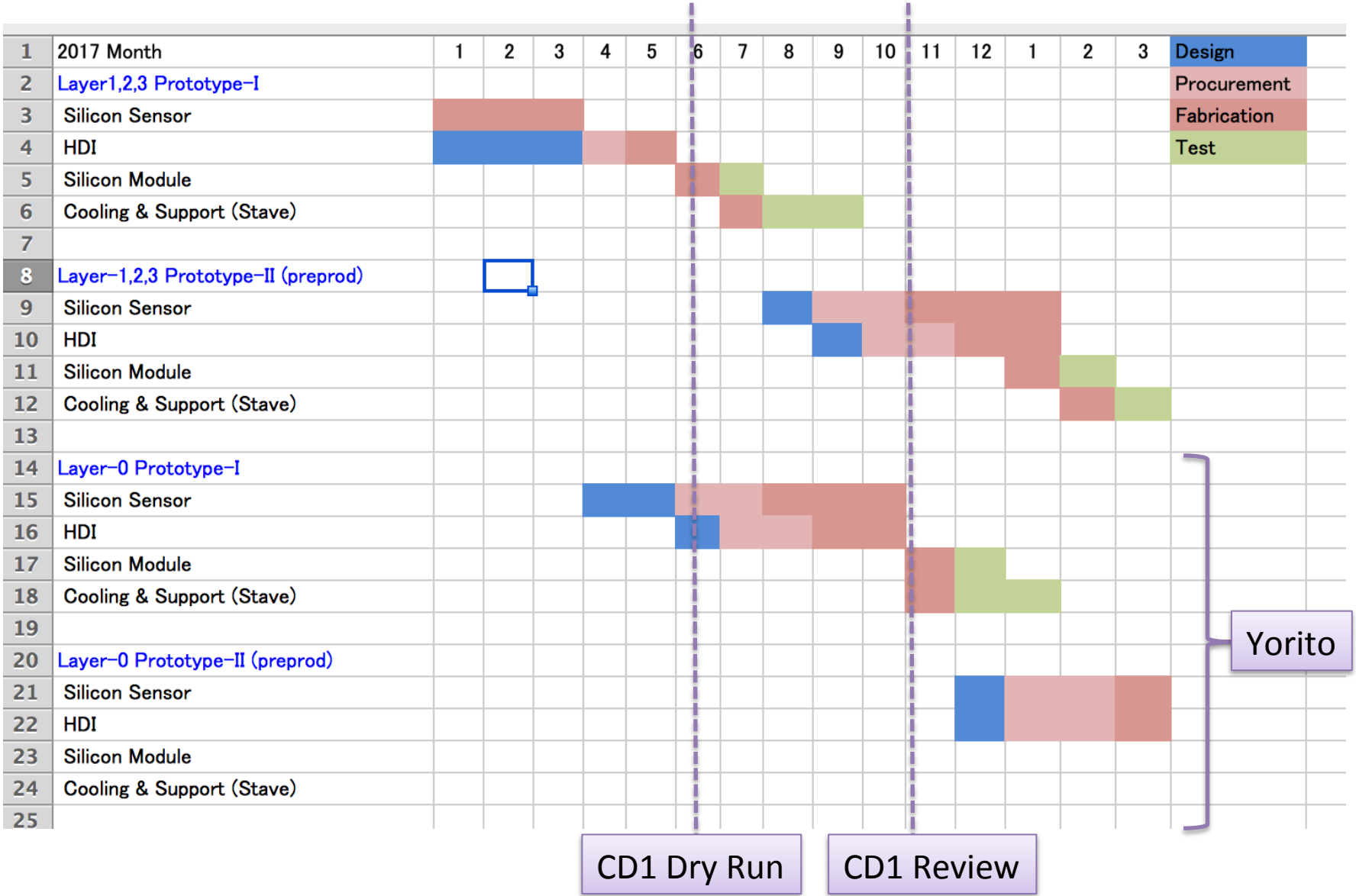
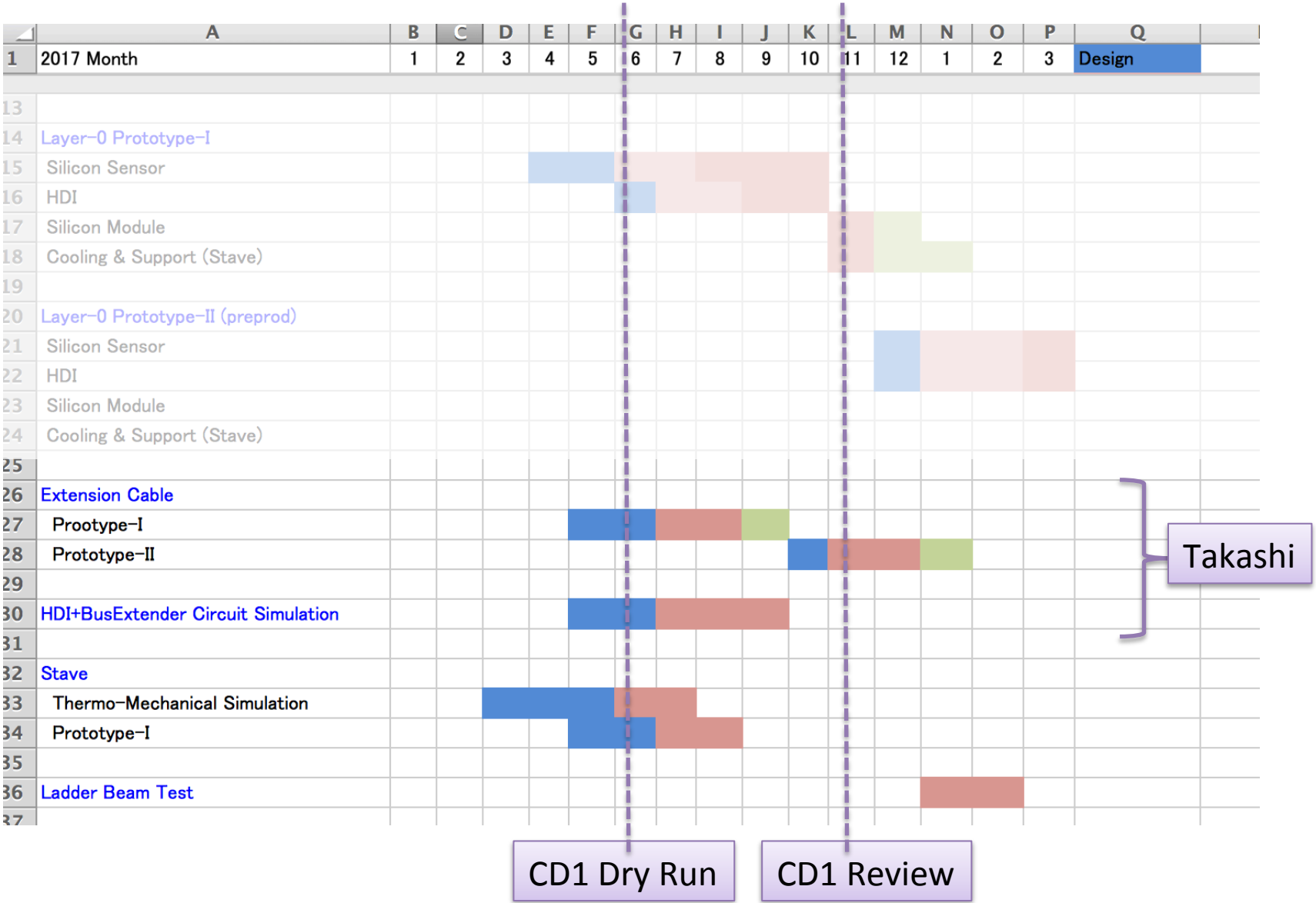
INTT Schedule Update

Itaru Nakagawa
RIKEN

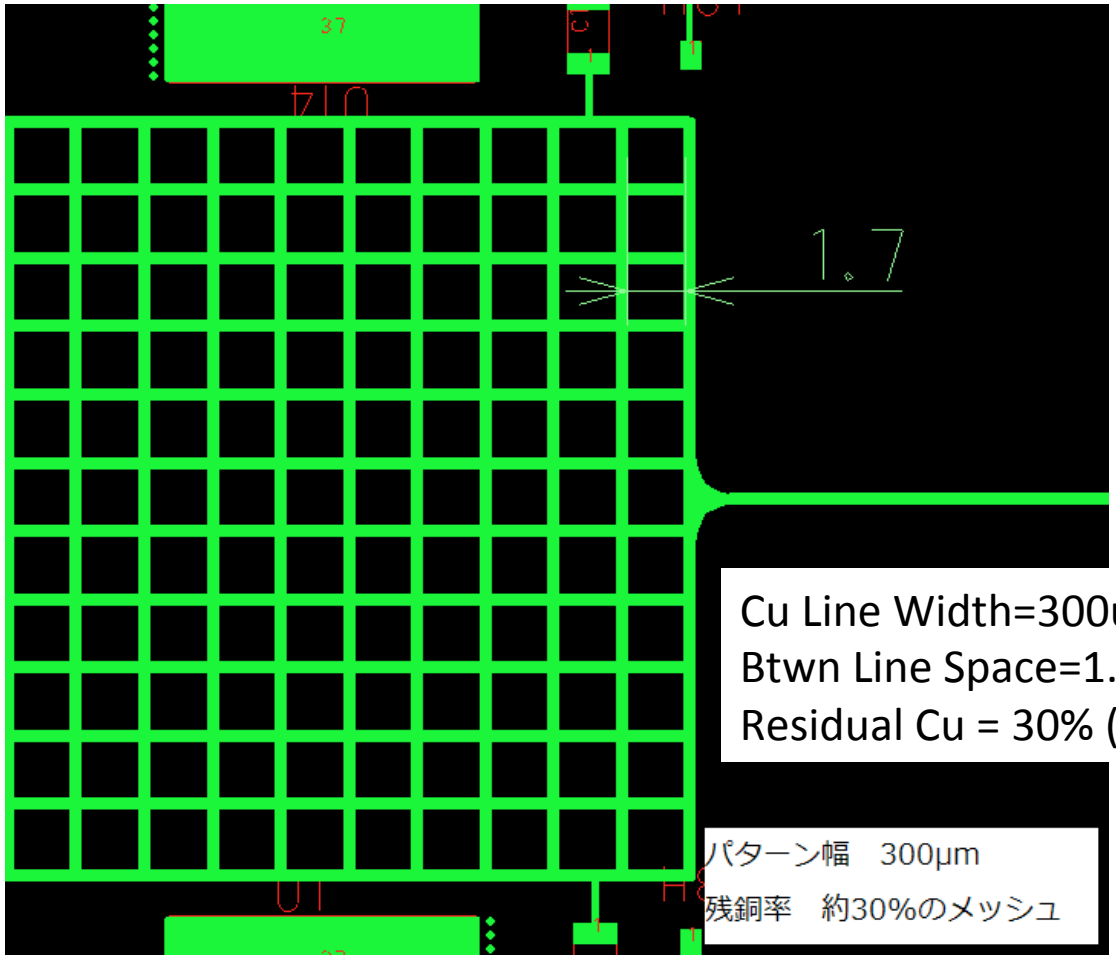
Schedule1: Silicon Module



Schedule1: Bus Extender + Stave



Mesh Ground Design



Cu Line Width=300um
Btwn Line Space=1.7mm
Residual Cu = 30% (10% not feasible)

Residual Cu	10%	30%
HDI Radiation Length	0.76%	0.86%

Worry about mesh

Subject: Re: mesh design of HDI
From: Hubert van Hecke <hubert@lanl.gov>
Date: 2017/04/01 9:49
To: Itaru Nakagawa <itaru@bnl.gov>

I'm not an expert on this. Our problem was not layer-to-layer noise, but the noise in the
environment getting into the cables and completely overwhelming the signal from the
silicon.

Perhaps it is time to do a test with a mesh to see how deep signals penetrate through a
give mesh size (which could be big for the test)?

Why don't you just do a thin, solid shield plane?

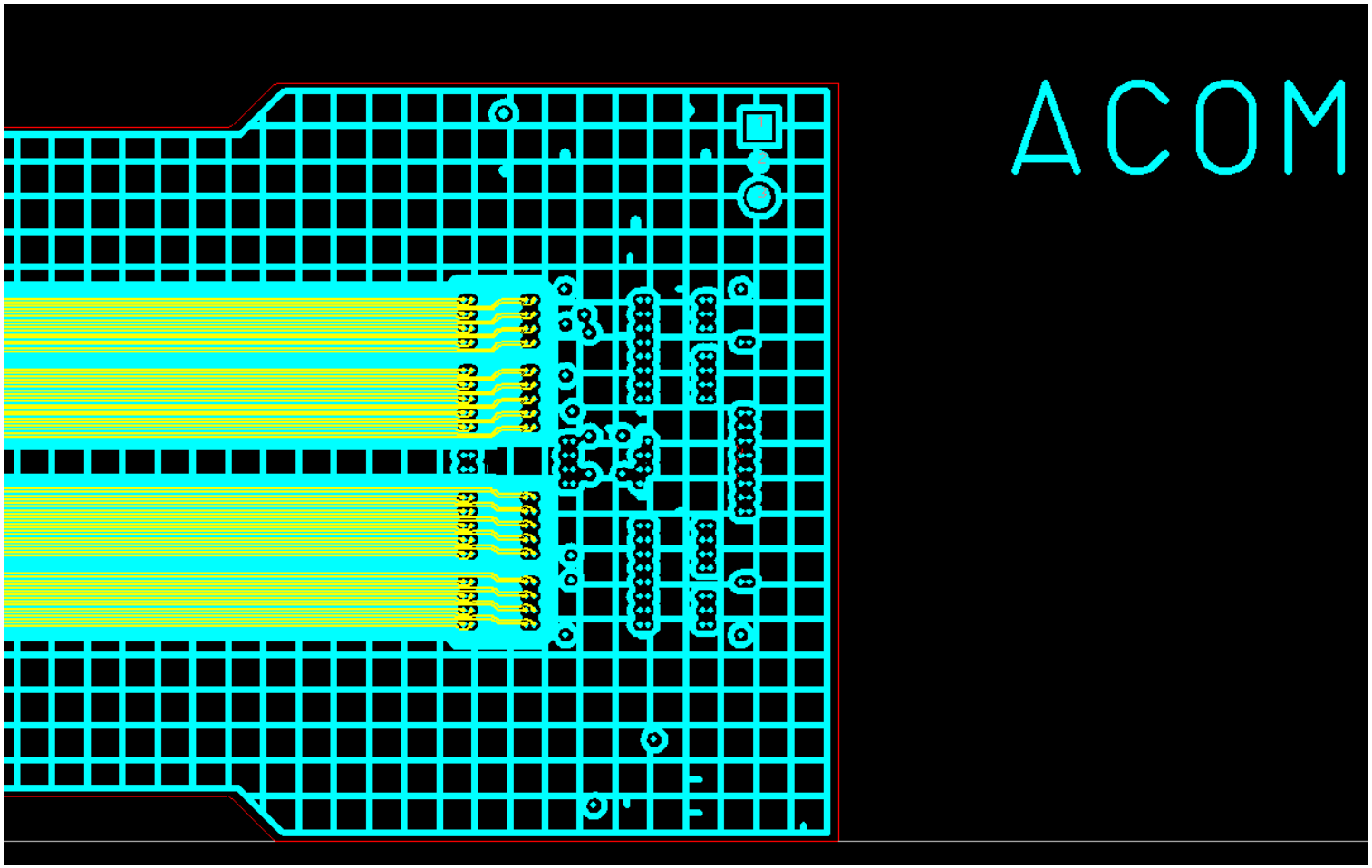
Hubert

On 3/31/17 5:21 AM, Itaru Nakagawa wrote:

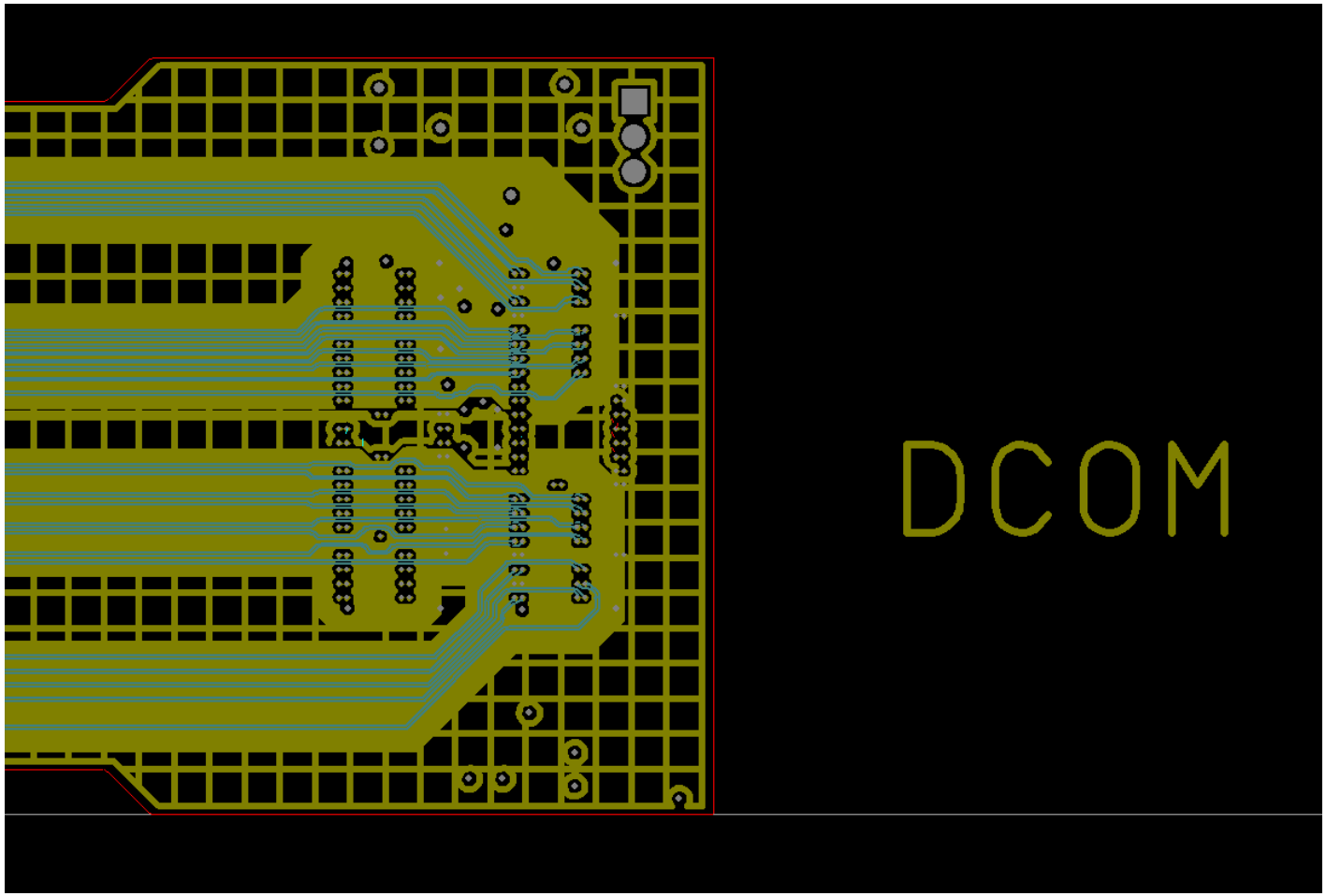
> Hi Hubert,
>
> Frankly, I don't have a feeling how the mesh design let noise to penetrate in depth. Do you know if there is a good reference about this? I guess the noise effect generated in the signal layer to the other layers can be simulated by a simulator. However, we won't be able to simulate the noise effect comes from external source since we don't know the its distribution...
>
> -itaru

We need circuit simulation work on this. Any volunteer?

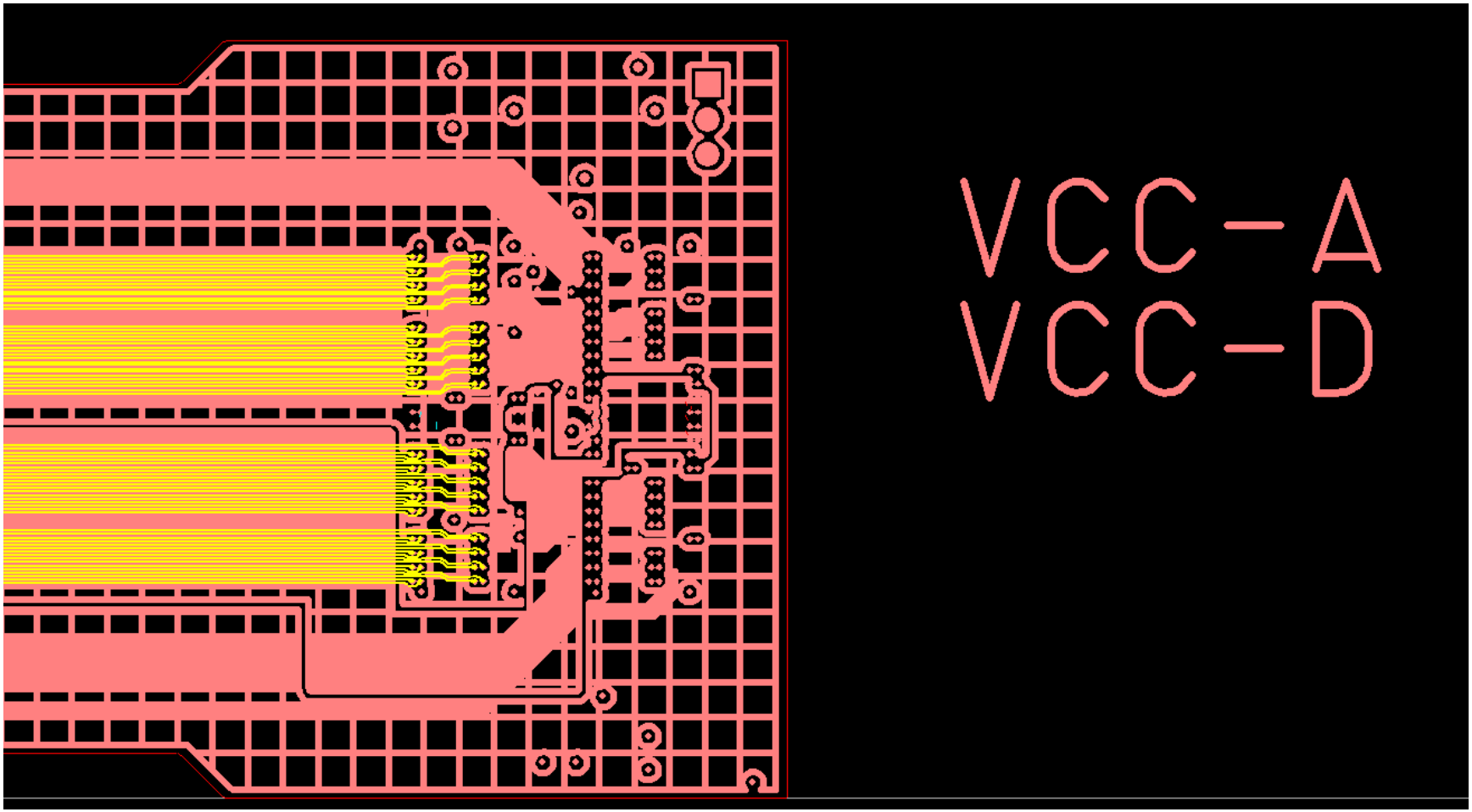
Mesh Design : ACOM



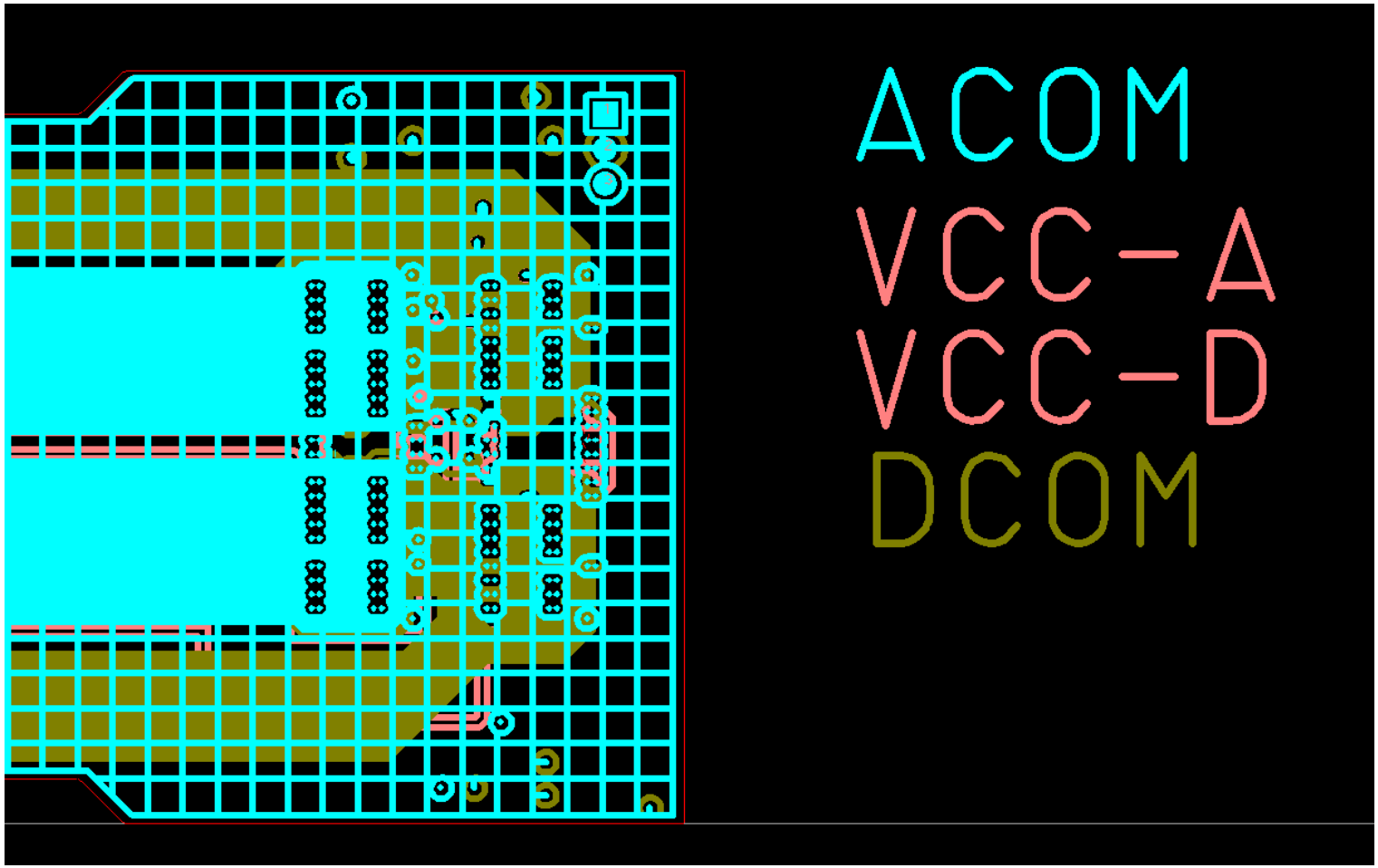
Mesh Design : DCOM



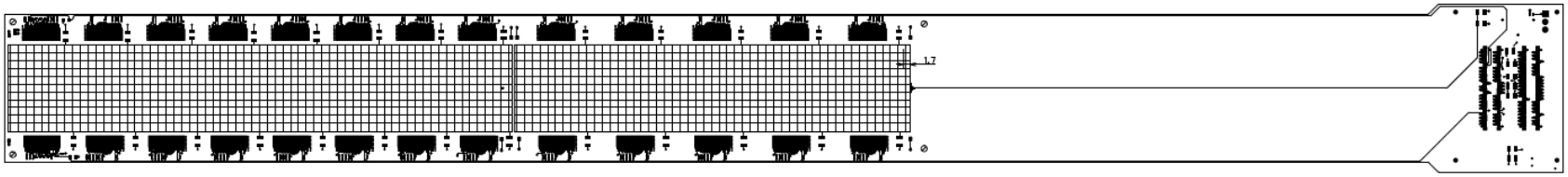
Mesh Design : VCC



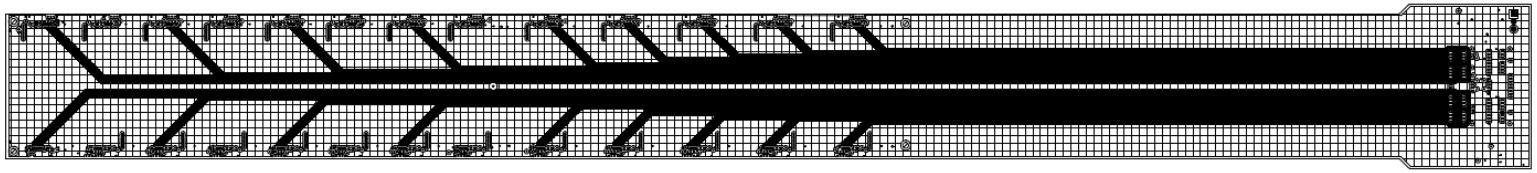
Mesh Design : Multi-Layers



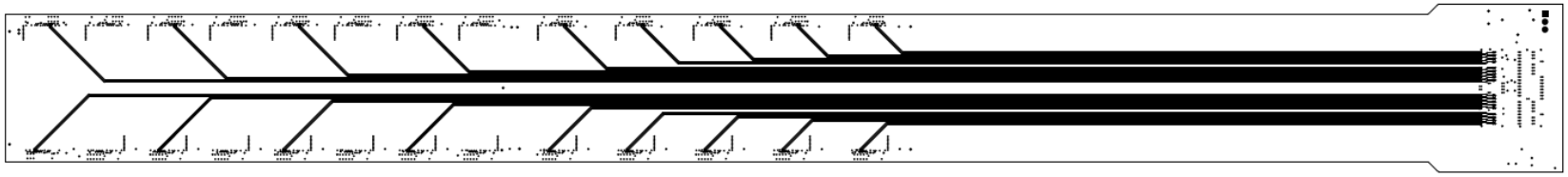
Layer-1



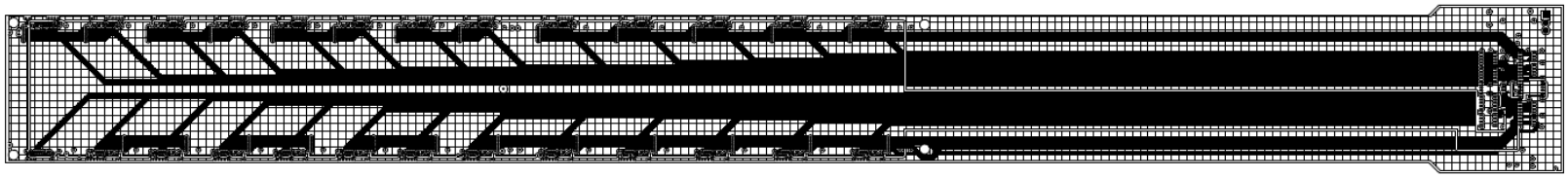
Layer-2



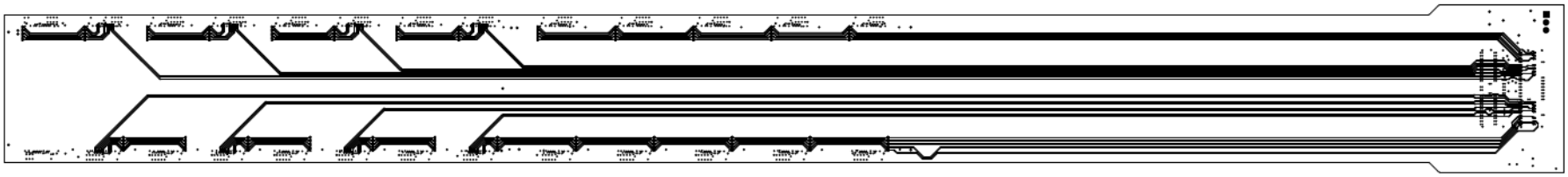
Layer-3



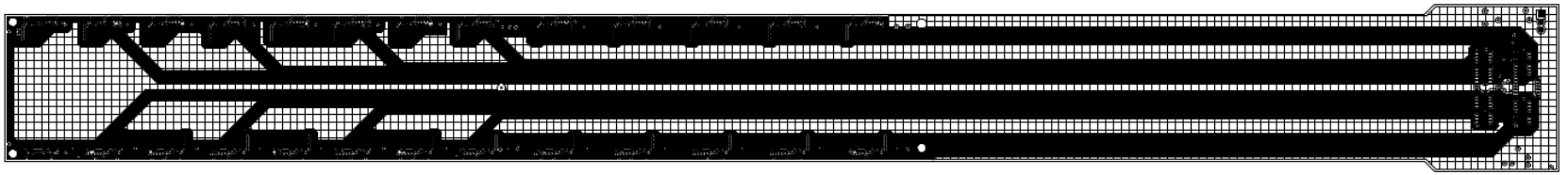
Layer-4



Layer-5



Layer-6



Layer-7

A few cm (not covered by ground layer)