FCFD Pre-FEB for HRPPD

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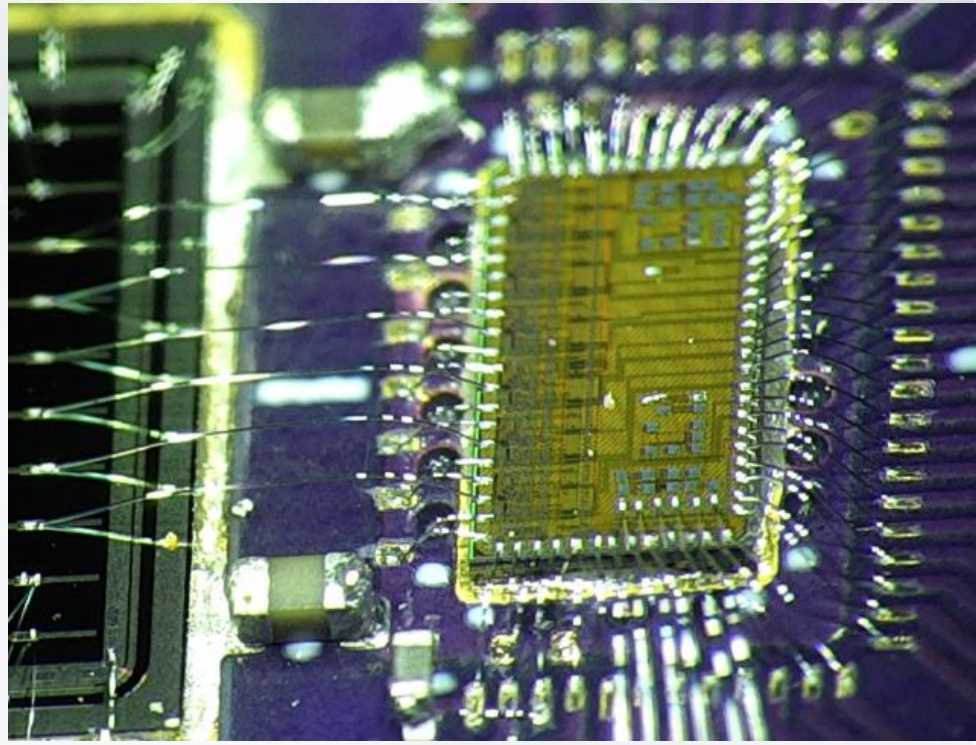
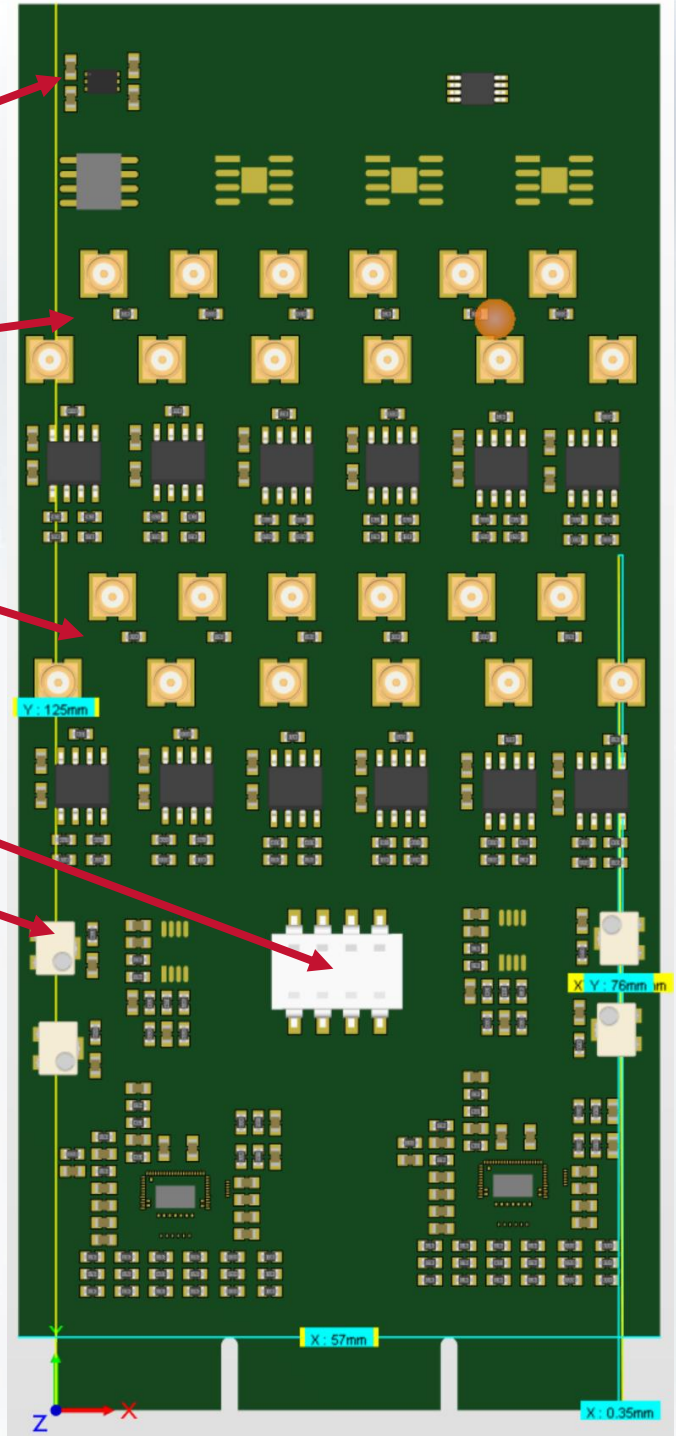
Board Overview

- FCFD = Fermilab Constant Fraction Discriminator
  - Prototype Front-end ASIC designed by Fermilab for the AC-LGAD sensors
- Each ASIC can monitor 6 input channels
- Each input has an analog output and a digital CFD output
- Maximum dynamic range = 100 fC
- Board is designed to monitor a 12 pad (3x4) rectangular area of the anode pads
  - Board is compatible with current HRPPD backplane



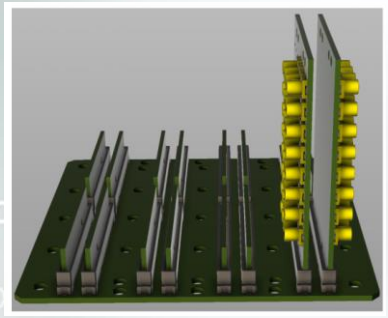
Board Picture

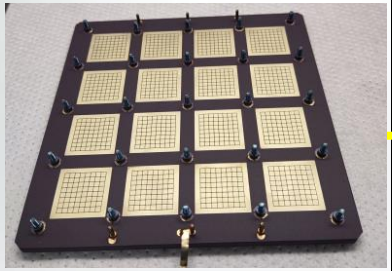
- 3 pin input power: ±5 and GND
- MMCX connectors for analog outputs and CFD outputs
- User adjustable switches
- User adjustable trimpots
  - For tuning ASIC settings
- Dimensions: 125 x 57 mm
  - Original board dimensions: 76 x 57 mm

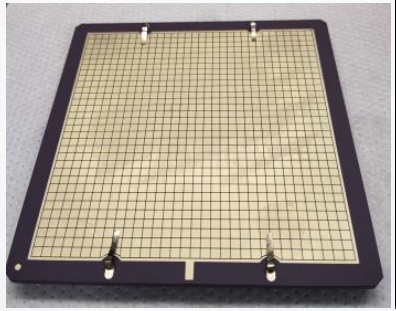


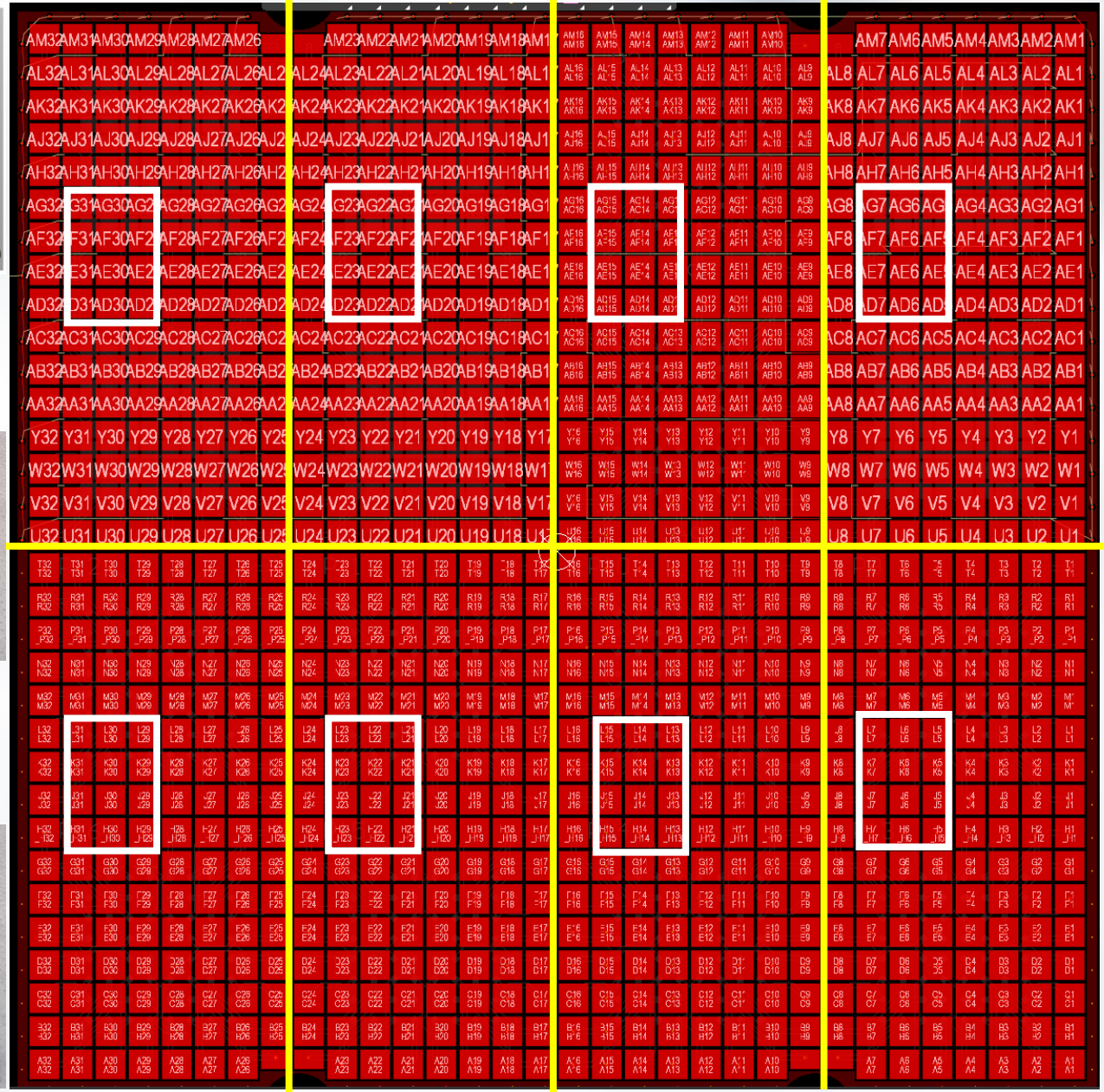
Detection Area

- A single board can monitor a single, fixed 3x4 (12 pad) area
  - Highlighted with white boxes
- This area can be moved into any of the 8 yellow sections by physically moving the card to a different connector on the backplane
  - 8 white boxes = 8 pad areas
- Multiple boards could be used to monitor different sections at the same time





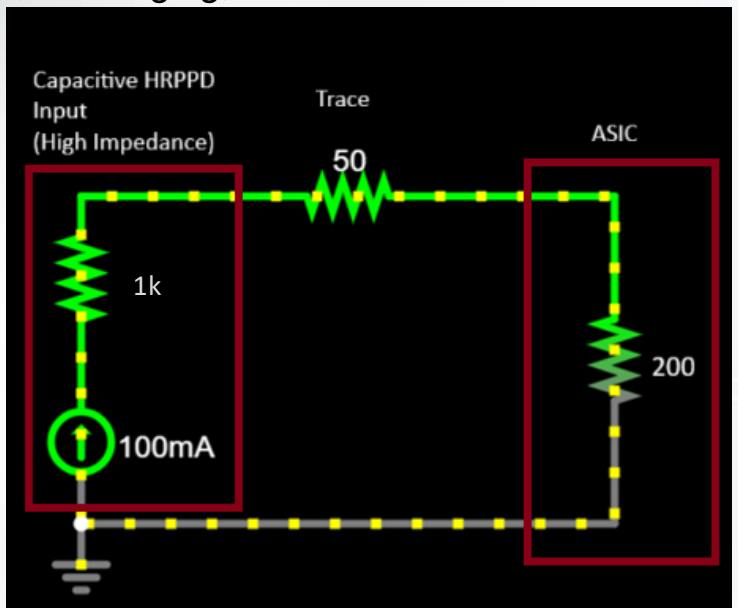




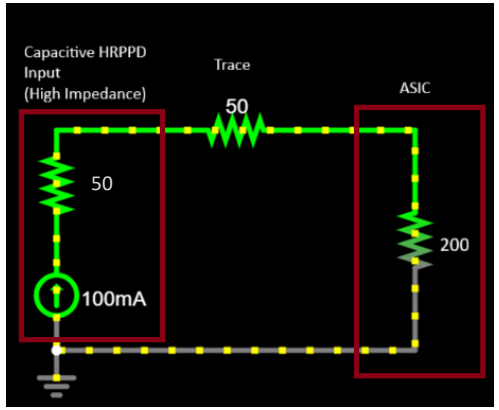
Signal Integrity

- Problem:
  - The HRPPD signal is a fast edge (0.4ns) going over an electrically long distance (~2.2 inches > 0.6in critical length)
  - The HRPPD characteristic impedance (50Ω) does not match the ASIC receiver impedance (~200Ω)
  - The test setups for the HRPPD typically use test equipment with 50Ω matched impedances that avoid this issue

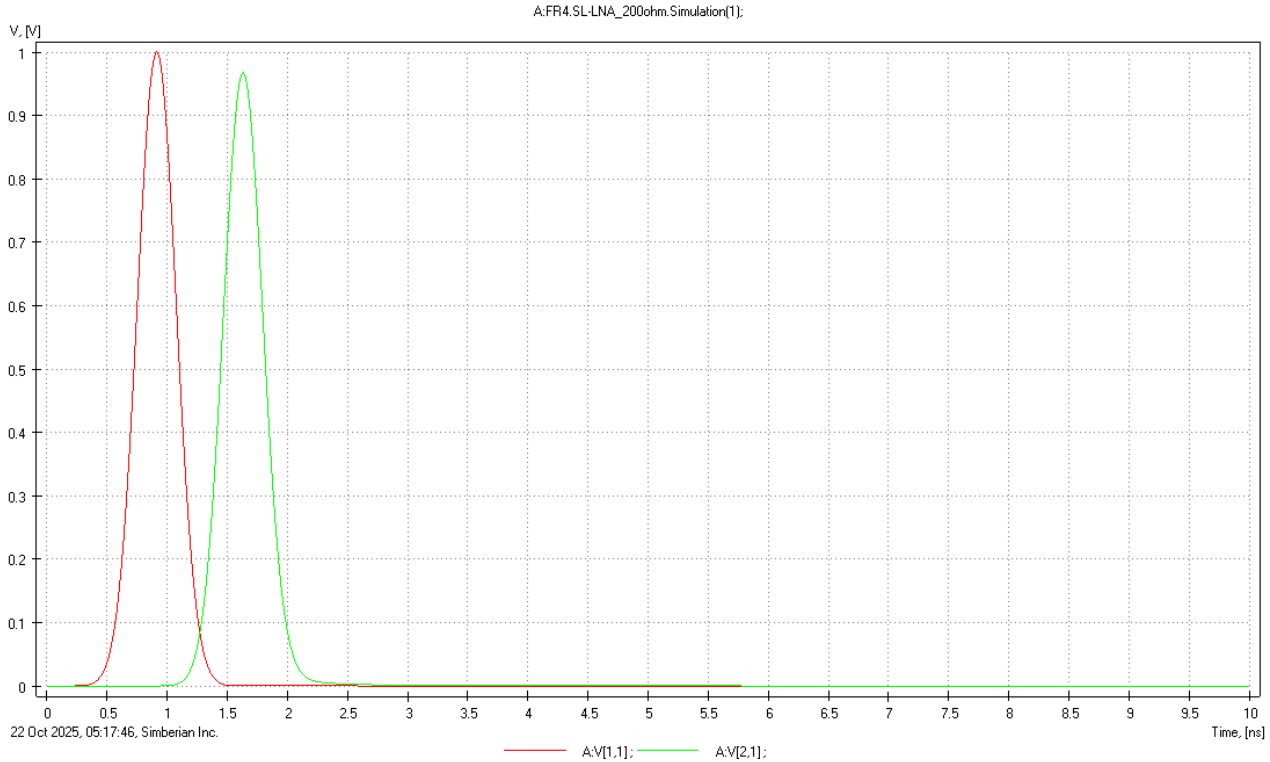
- Why is this a problem?
  - The mismatched, higher impedance of the ASIC combined with the capacitive pads of the HRPPD causes electrical reflections that distort the input signal
  - Reflections cause overshoot, undershoot, and ringing, which can be seen as incorrect charge measured or false pulses



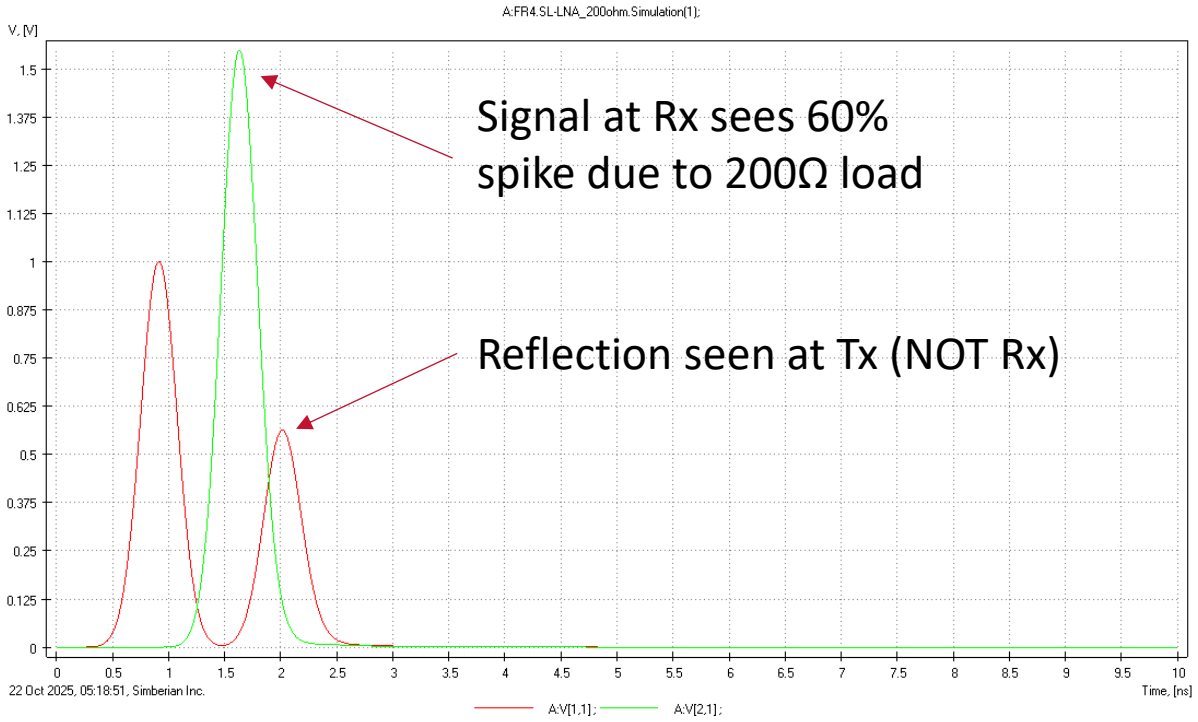
Simulation



2.2 inch trace with proper 50Ω matching

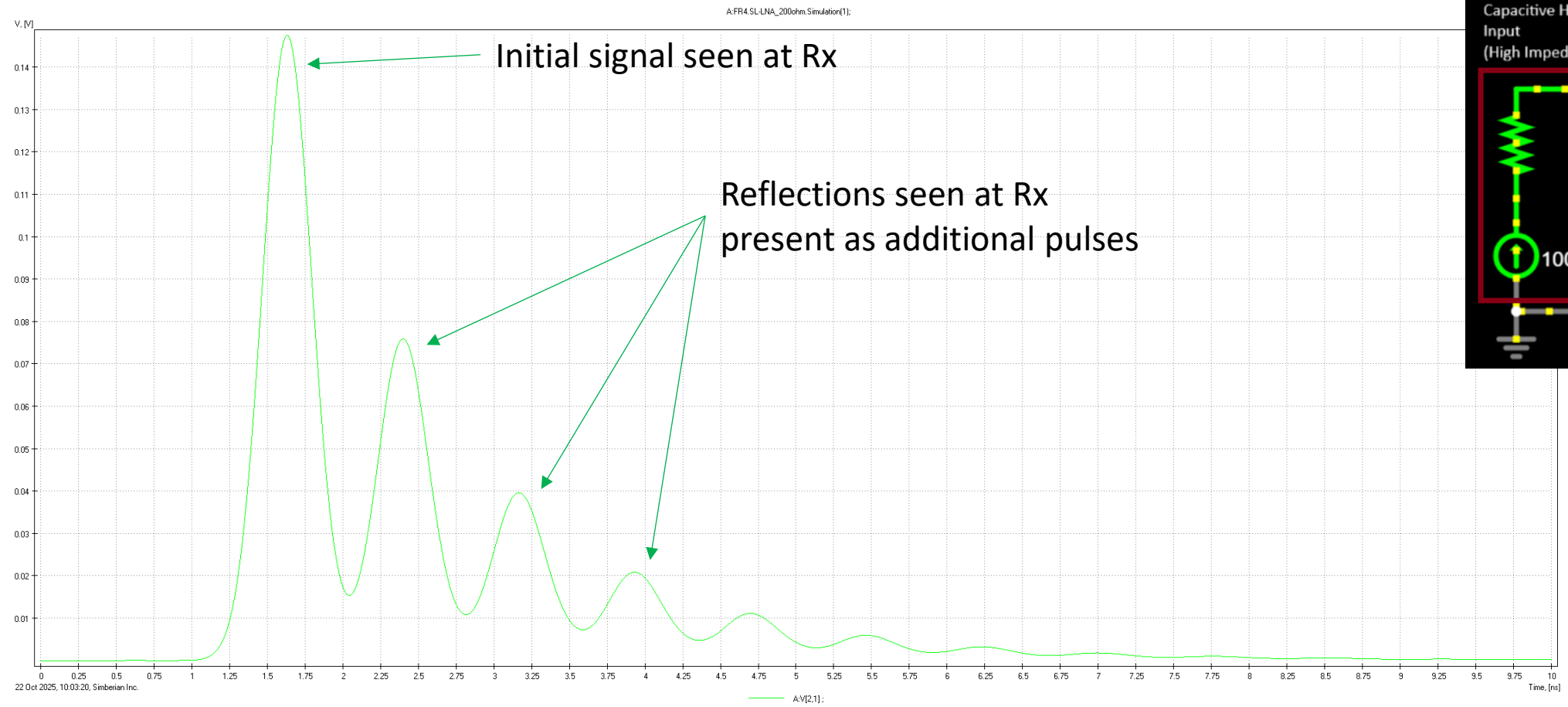


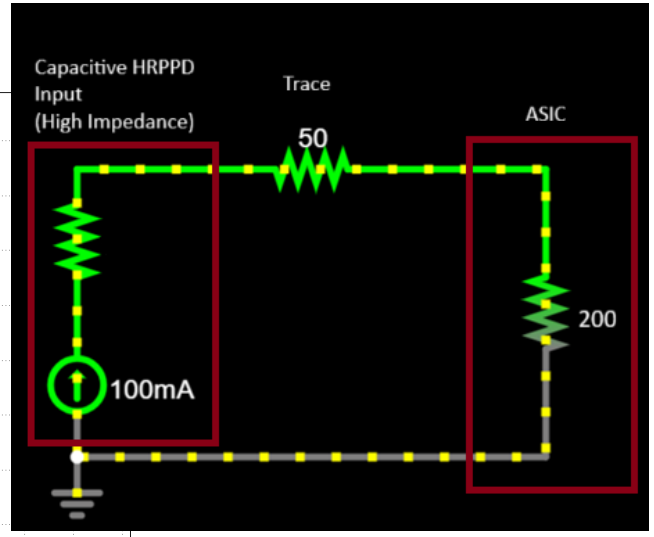
2.2 inch trace with 50Ω source and 200Ω load



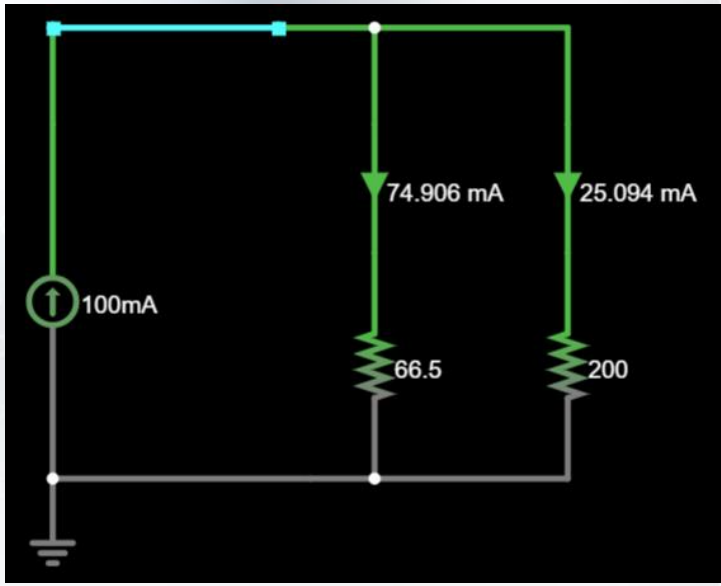
Simulation

2.2 inch trace with 1kΩ input impedance, 2.2 inch 50Ω transmission line, 200Ω load



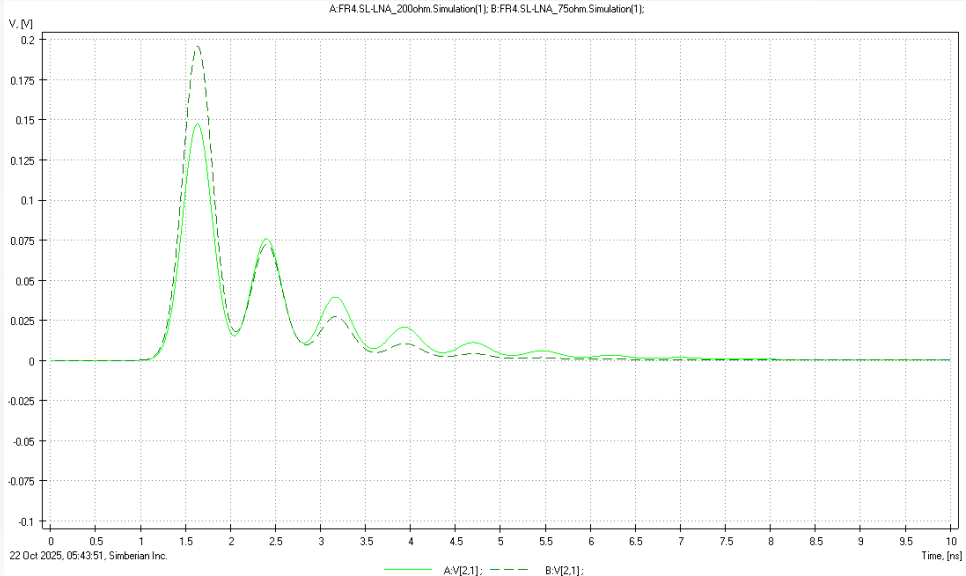


Next Steps

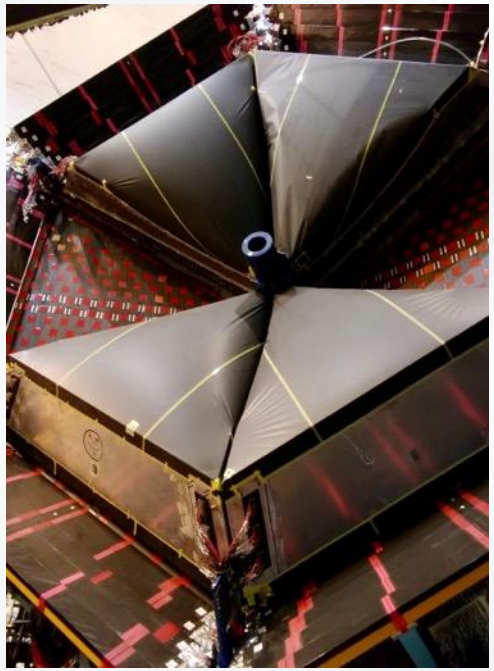


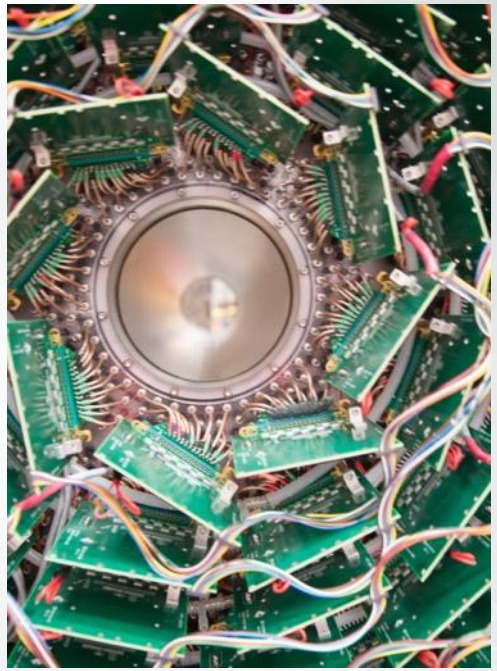
Potential solutions:

- Add parallel termination resistor at input of FCFD
  - The typical way to solve these problems
  - Causes current to divert into termination resistor instead of FCFD, resulting in 25% of current going into FCFD, 75% current lost
  - Signal shape preserved but attenuated
  - If HRPPD charge is 160fC @ 10^6 gain, FCFD would receive 40fC
  - **This resistor is testable on the prototype board**
- Increase characteristic impedance of HRPPD and PCBs
  - Could achieve ~73Ω with 2 mil trace width and 20 mil plane spacing top / bottom
    - This would affect the location of the center signal layers, and potentially the thickness of the HRPPD
  - Does not significantly impact reflections
  - If a termination resistor is needed, 37.5% of current would enter FCFD
  - **Significant design change to HRPPD with low benefit**
- Additionally:
  - Change gain of HRPPD to compensate for signal loss
  - Gain of 1.2E6 would compensate for signal loss, but result in 4x aging



Appendix





User Adjustments

These settings are user adjustable for each ASIC on the board:

- ThrSet trimpot - Threshold for the CFD timewalk adjustment
- ArmThr trimpot - threshold charge for the arming comparator
  - 1.05V sets to 7 fC
- ISel switches – sets bias current for input transistor of
  - Adjusting this can reduce jitter
- DSel switches - Selects transfer delay of the discriminator
  - Adjusts delay of the CFD, but doesn't have much effect per the designer
- Analog outputs require calibration
- Output connectors are MMCX, connect to oscope with 50Ω terminator

Simulation

2.2 inch trace with 1kΩ input impedance, 2.2 inch 50Ω transmission line, 200Ω load