MPW1 Testing Update @ BNL

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SVT Work Meeting

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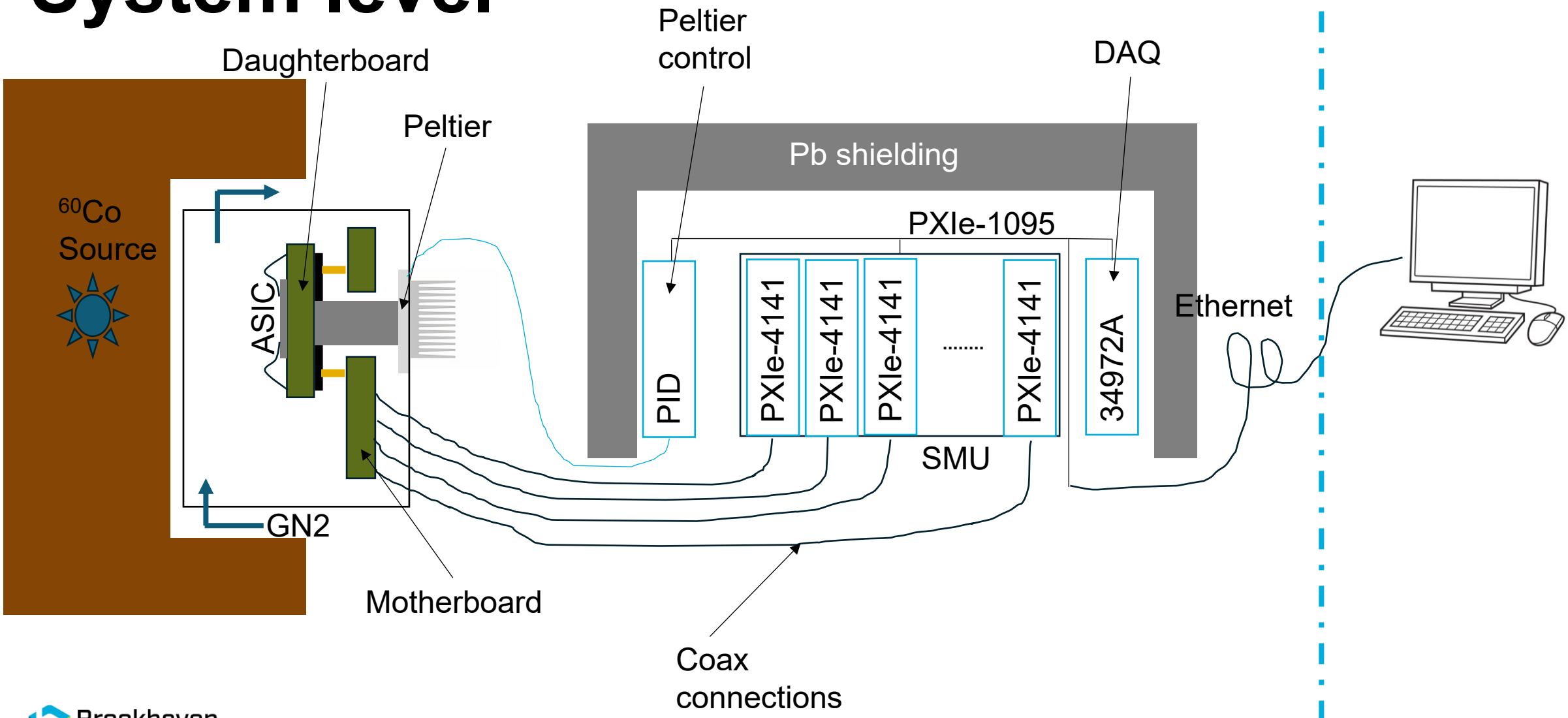
Outline

- Test setup concept
- Test facility
- Test setup status
- Testing strategy
  - NVBG verification
  - Full irradiation testing
- Summary

Conditions and specs

- Irradiating 3 chips per conditions:
  - Temperature= RT, 40 C and 0 C
  - ON and OFF status
- 18 chips to test
- Irradiation rates ~20 krad/h
  - Assuming TID~ 2-3 Mrad
  - 1 Chip <-> 5 days of testing
- Measurements will be live and continues (depending on dose steps)

System level



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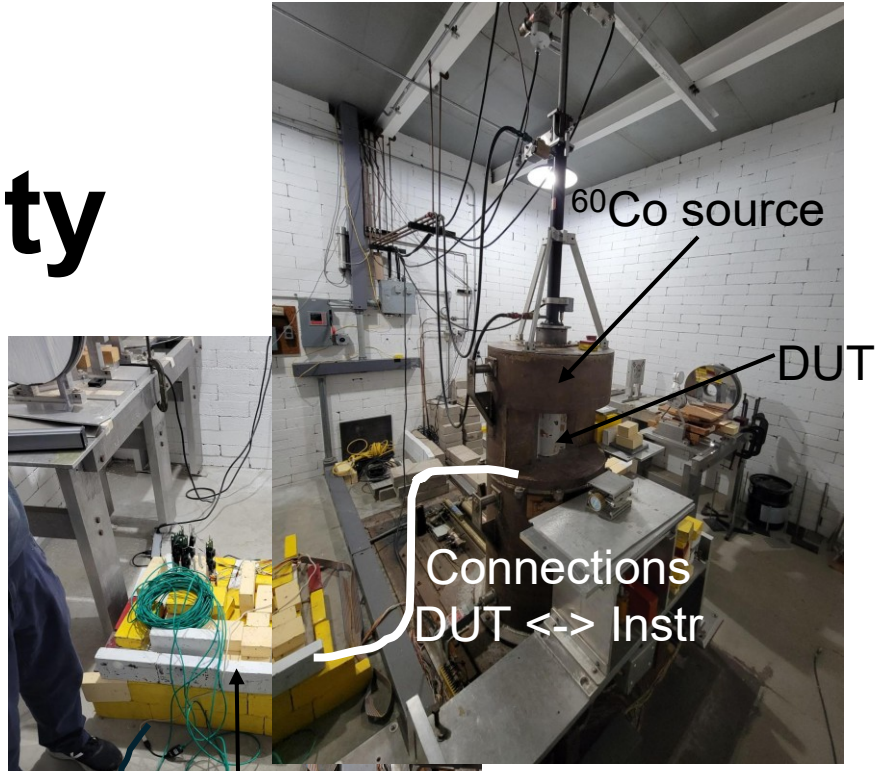
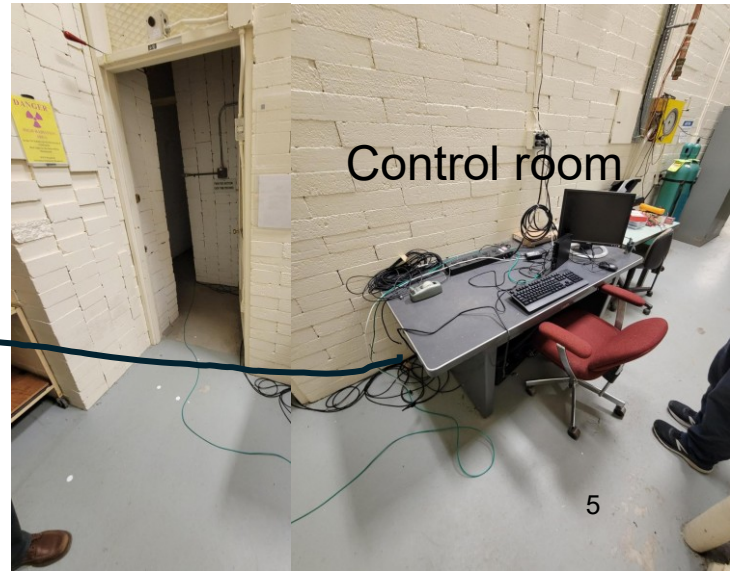
Irradiation Facility

- Three main areas:
  - Irradiation area (1173 keV, 1333 keV)
  - Shielded instruments in irradiation area
  - Control area



Control and data transmission



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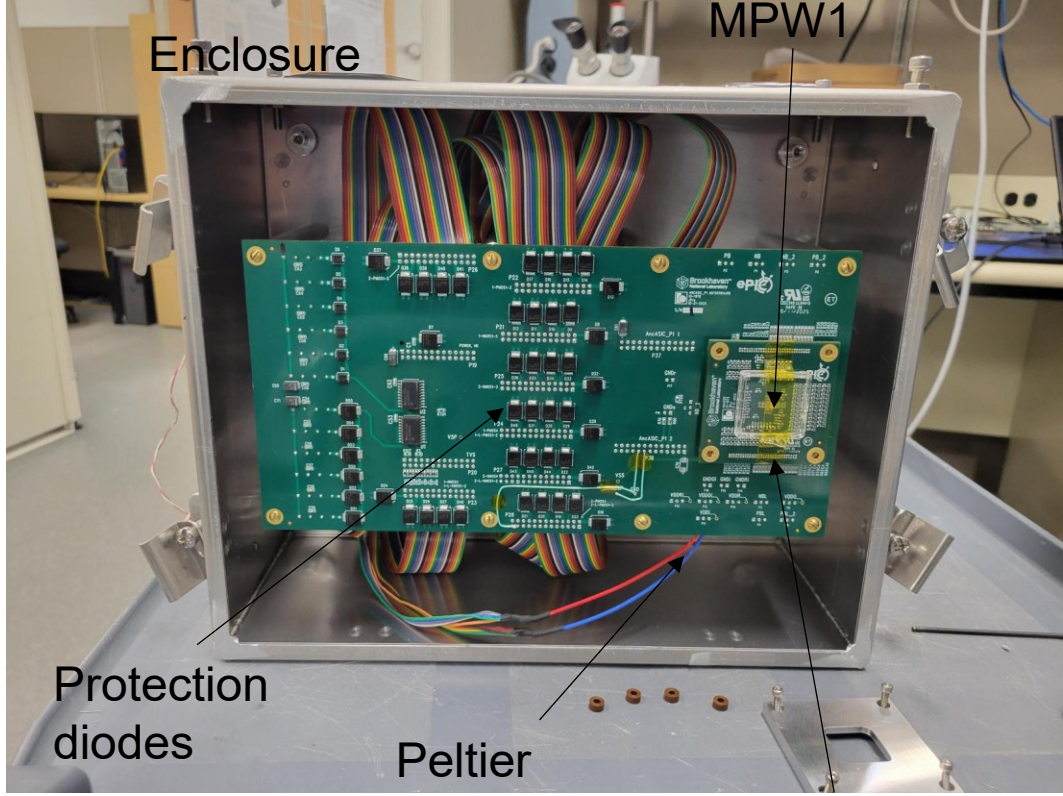
Testing strategy

1. Measurement of NVBG [completed]
2. Irradiation of NVBG block at room temperature up to 3 Mrad [12/17 – 12/22]
3. Measurements of NVBG + test structures [12/23 – 1/6]
4. Irradiation varying conditions [1/7 - …]

Phase 1

Test setup

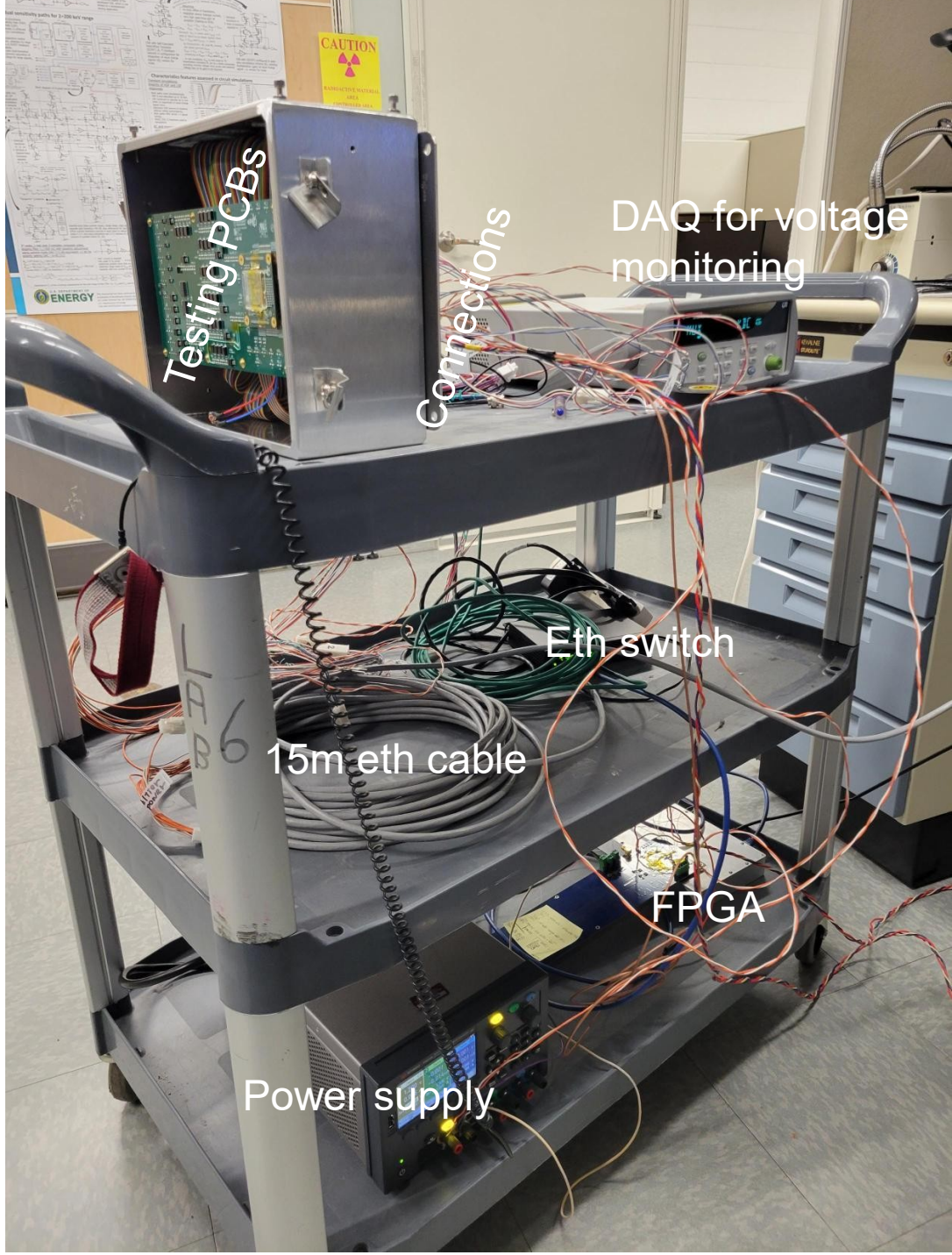
- Motherboard and mezzanine were delivered and populated
- MPW1 chip was successfully installed and wire-bonded
- System has been integrated into the enclosure
- Auxiliary features completed (RTD, PT100, GN2 inlet/outlet,…)



Test setup

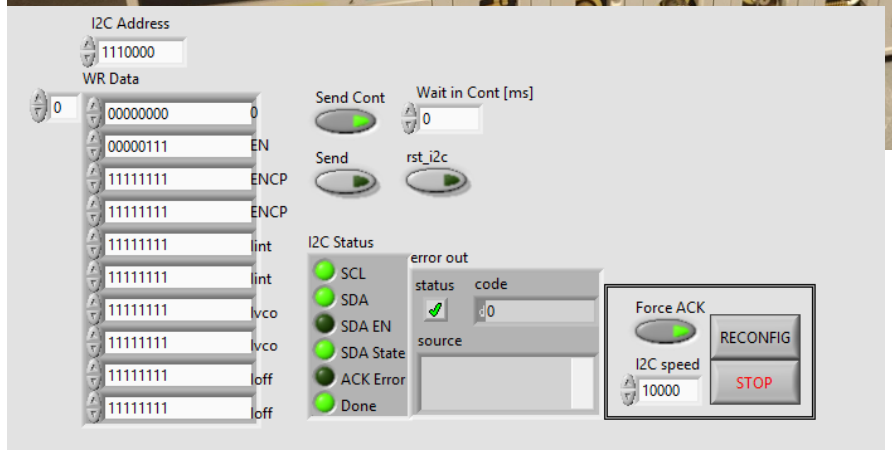
PCB testing has been interfaced with:

- DAQ datalogger to record temperature and NVBG output
- Power supply for 1.2V chip rail
- FPGA (with level shifters board) for I2C communication and 500 kHz clock for NVBG feedback



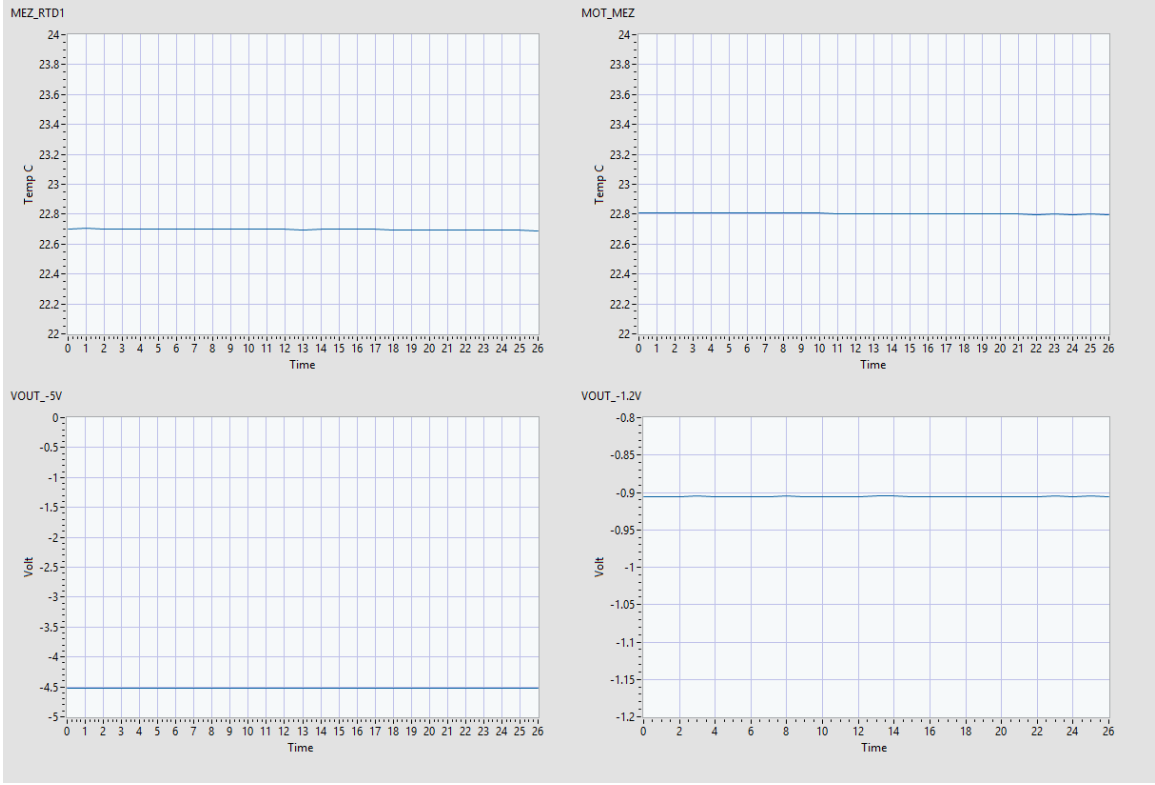
Software: communication

- Developed a program to communicate via I2C to set NVBG registers
- I2C std configuration is ‘0’ → NVBG outputs will be off at startup (safety feature)
- We successfully communicated with NVBG without any issues, and registers were configured successfully



Software: acquisition

- We are using an Agilent 34972A as data logger for temperature sensors and NVBG outputs
- Software for readout complete
- We can successfully readout temperature and NVBG outputs



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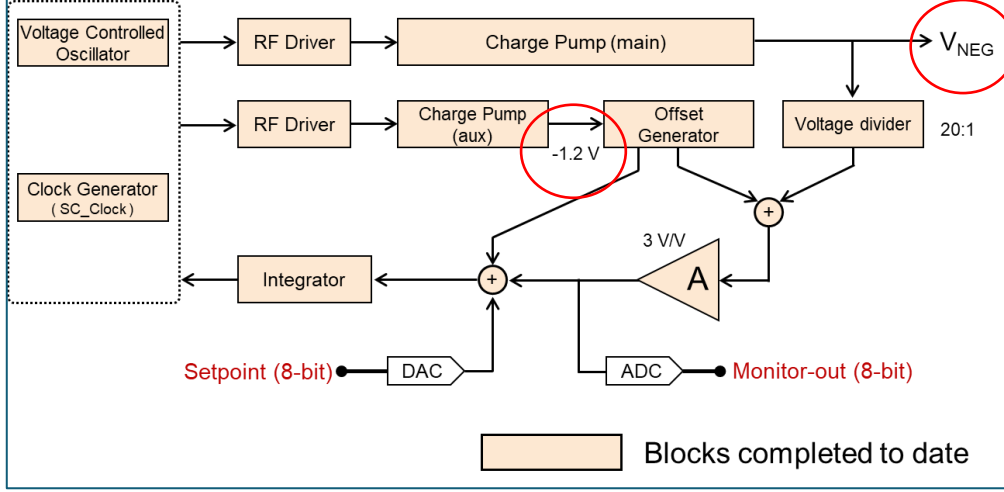
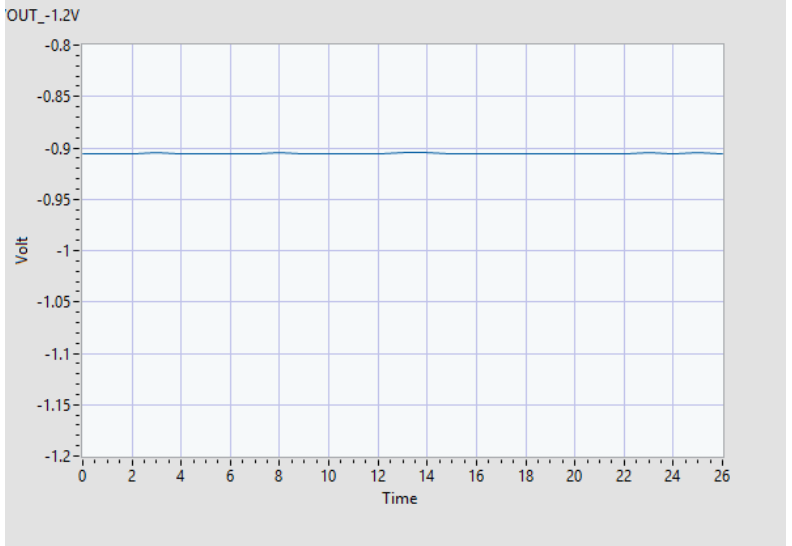
NVBG test

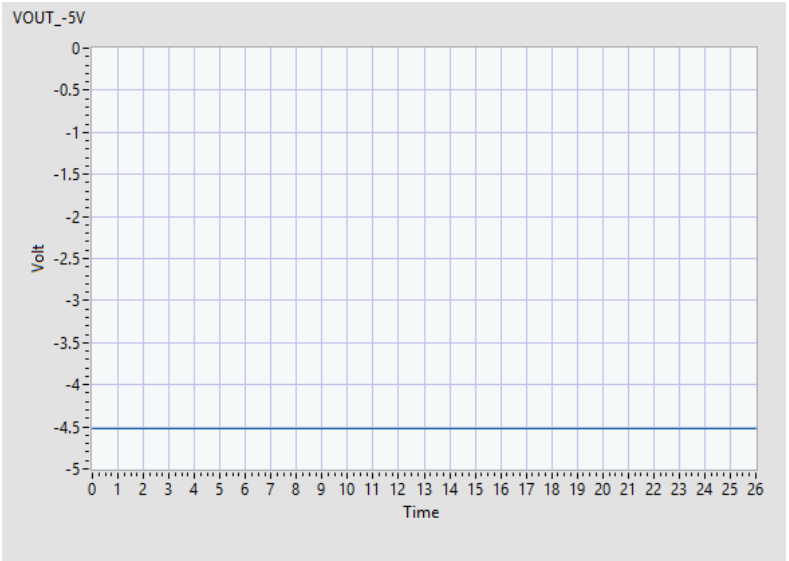
- NVBG has 2 outputs:
  - Auxiliary ~ -1.2 V
  - V_{NEG} down to -5V
- And parameters:
  - EN: enables auxiliary (001) and main charge pump (111)
  - EN_{CP}: enables an increasing number of charge pumps (in parallel)
  - Bias parameters



NVBG test

- We verified that enables registers work as expected and the two branches (aux and main) can be activated independently
- We verified that V_{NEG} output can be modulated varying EN_{CP}
- The Auxiliary output is about -0.9V (expected -1.2V)
- The largest output voltage for V_{NEG} is -4.5V





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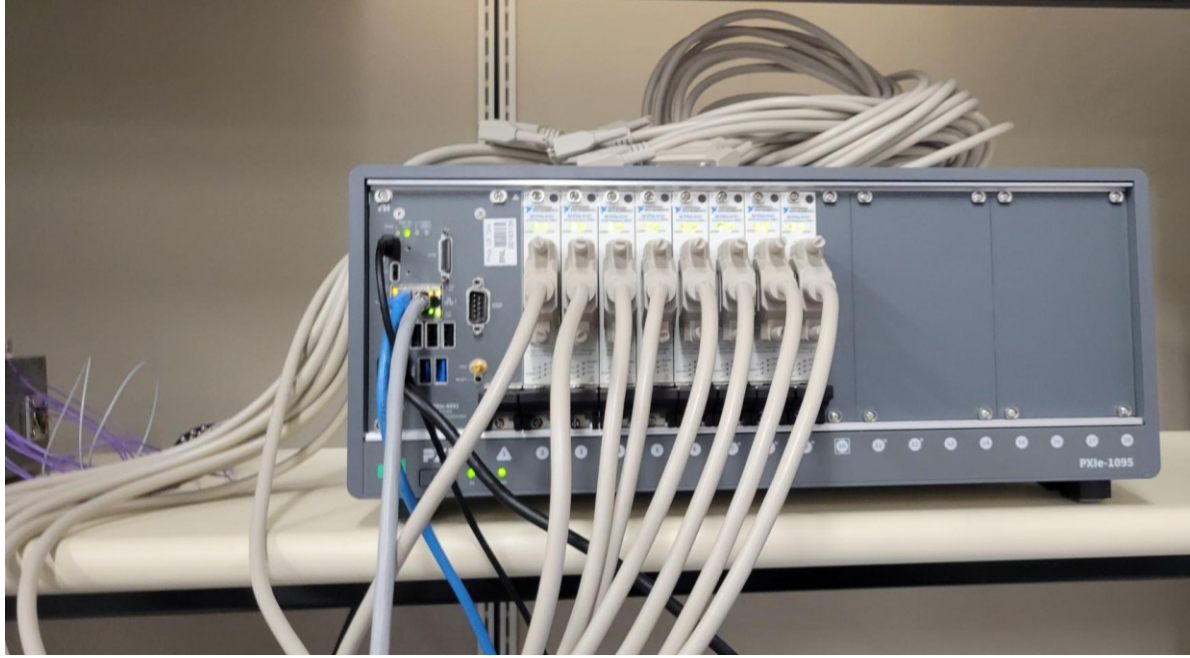
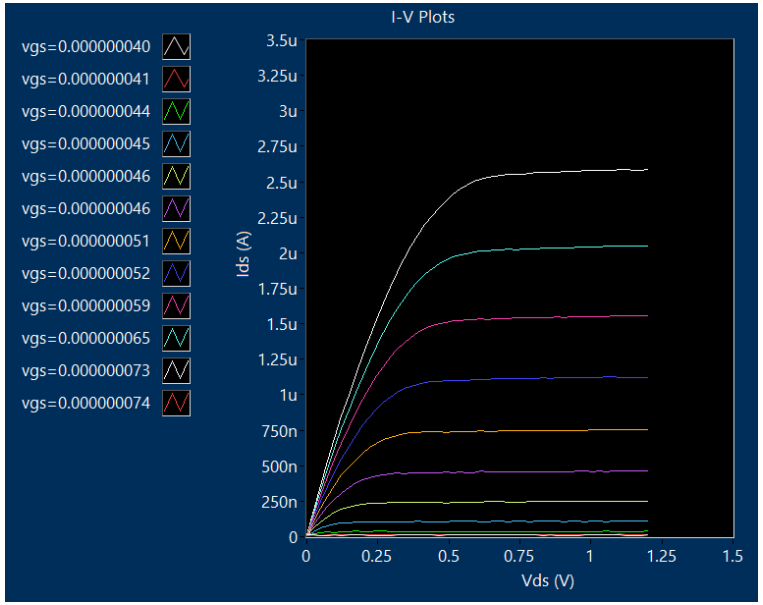
Phase 2

Test structure test

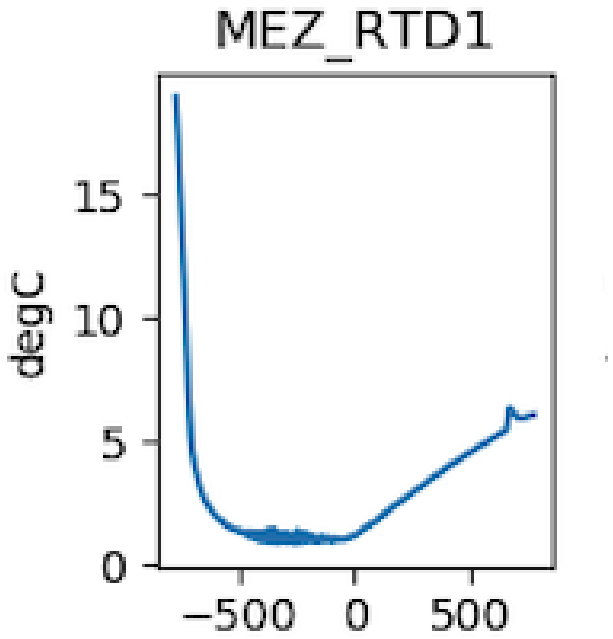
- NI PXIe SMUs are at hand and installed
- The system is plug-and-play with the designed setup
- Software is under development
- A first dry run will be performed with 65nm chip:
  - Bonding scheme defined
  - Chip removed from previous board





Cooling

- A dry run for the cooling system has been performed
- We managed to reach about 0C without any issues
- The box has integrated a Gas N2 inlet/outlet
- The facility provides a regulator and a flow-meter to adjust the flow and avoid ice



Summary

- Today (12/16) the setup will be installed at the Co60 irradiation facility
- We expect irradiation to start tomorrow (🤞)
- We will reach 3Mrad in about 5-6 days
  - There will be continuous monitoring of the output voltage
  - Detailed testing with parameters sweep at a few TID points
- After the first irradiation test, valuable information will be available to the collaboration
- Following, the setup will be integrated with the SMUs to provide test structures characterization
- A dry run with 65nm will be performed
- The setup will be re-installed at the irradiation facility first/second week of January to follow with the testing of chips in 3 different temperature regimes and in ON/OFF state comparison