AncASIC MPW1 Test at LBL

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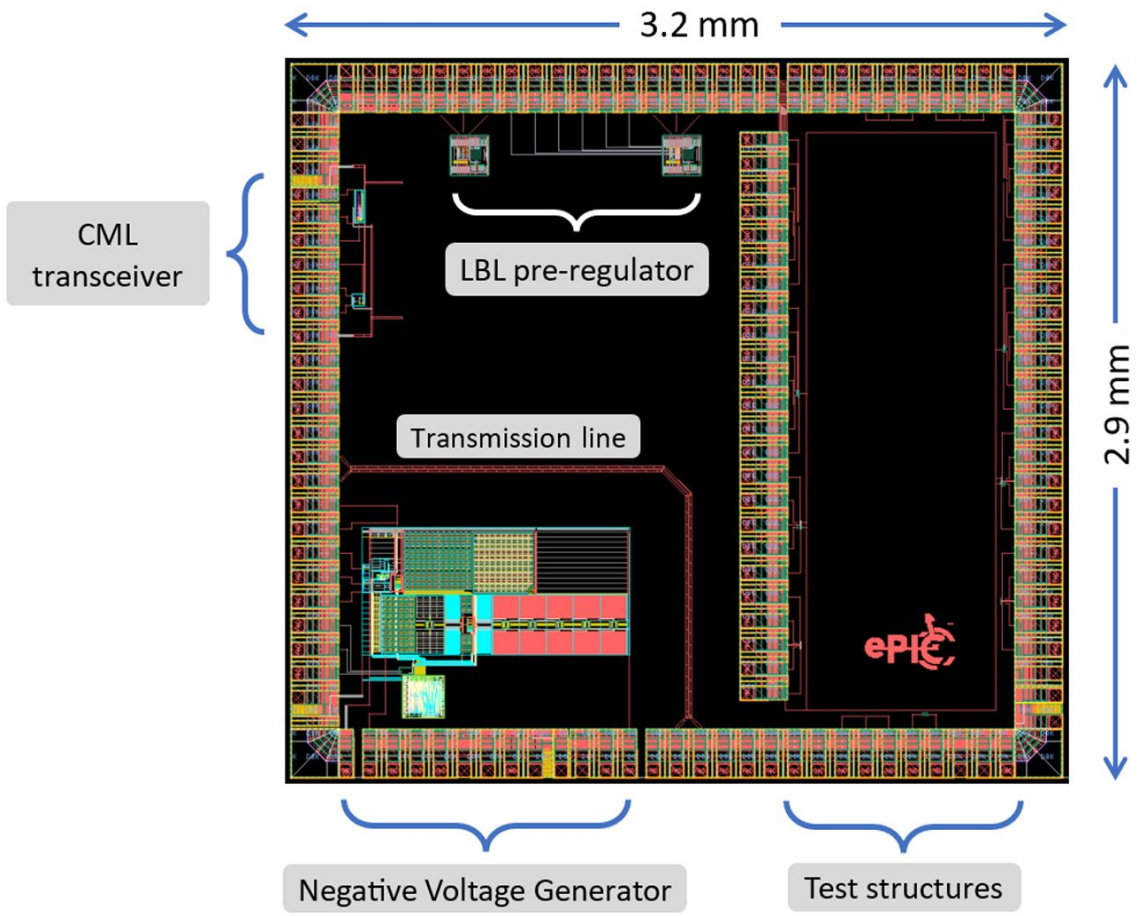
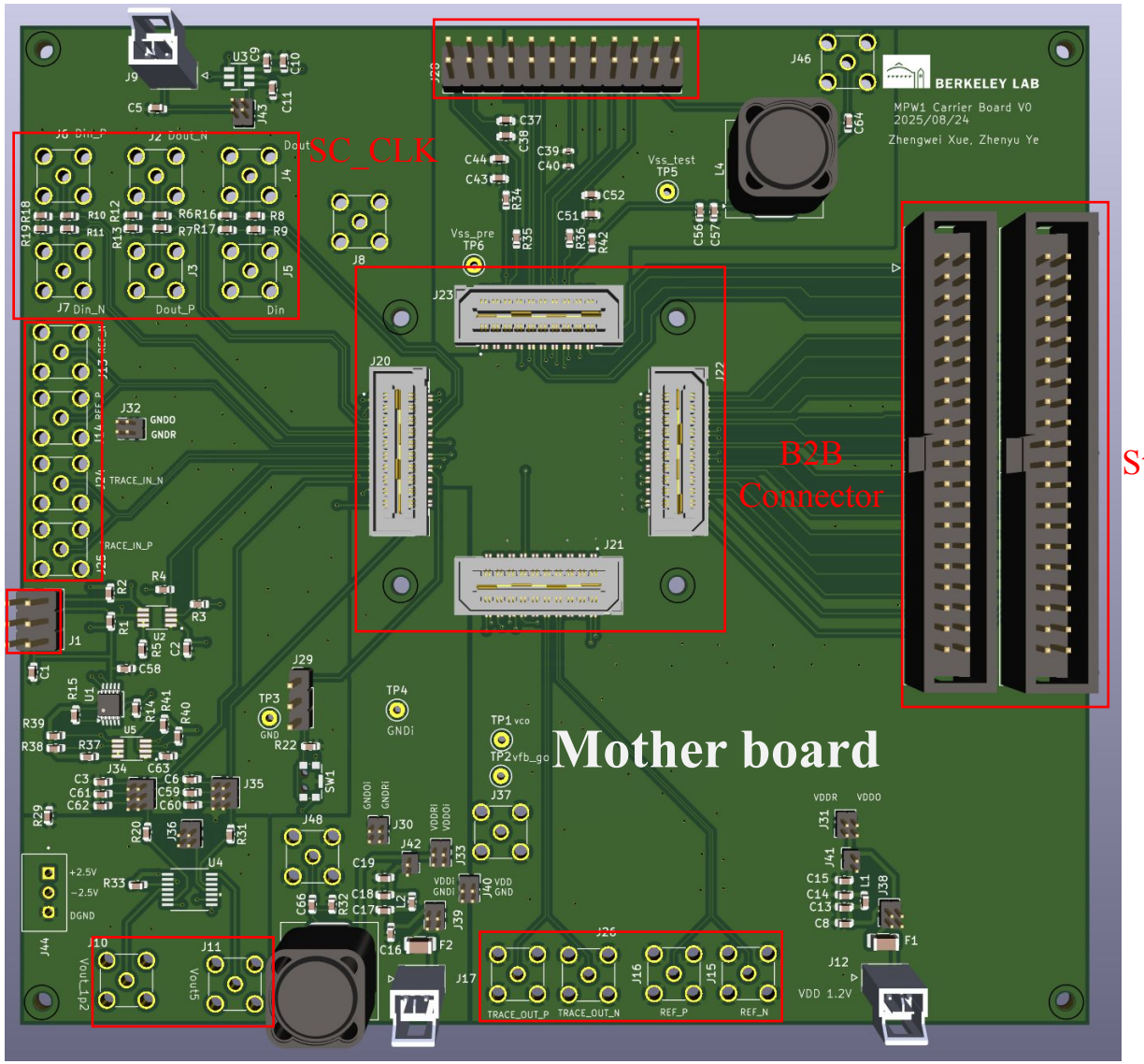
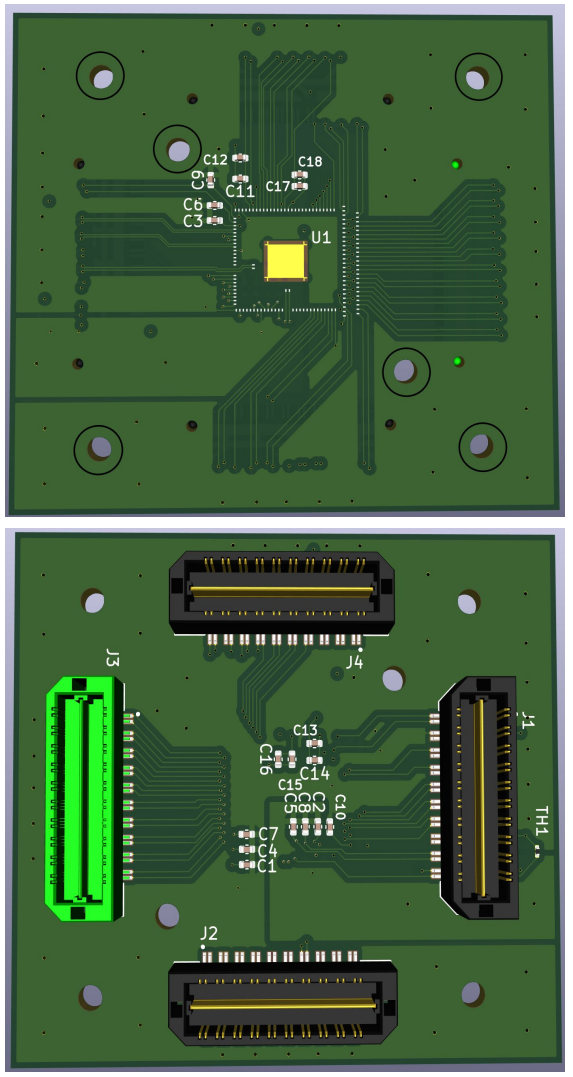
AncASIC MPW1



- A passthrough, differential transmission line
- Current-mode logic (CML) transmitter and receiver
- Pre-regulator designed by LBNL ASIC group
- An I2C controller
- Negative voltage bias generator (NVBG)
- Test devices (MOSFET, BJT, resistor, etc.)

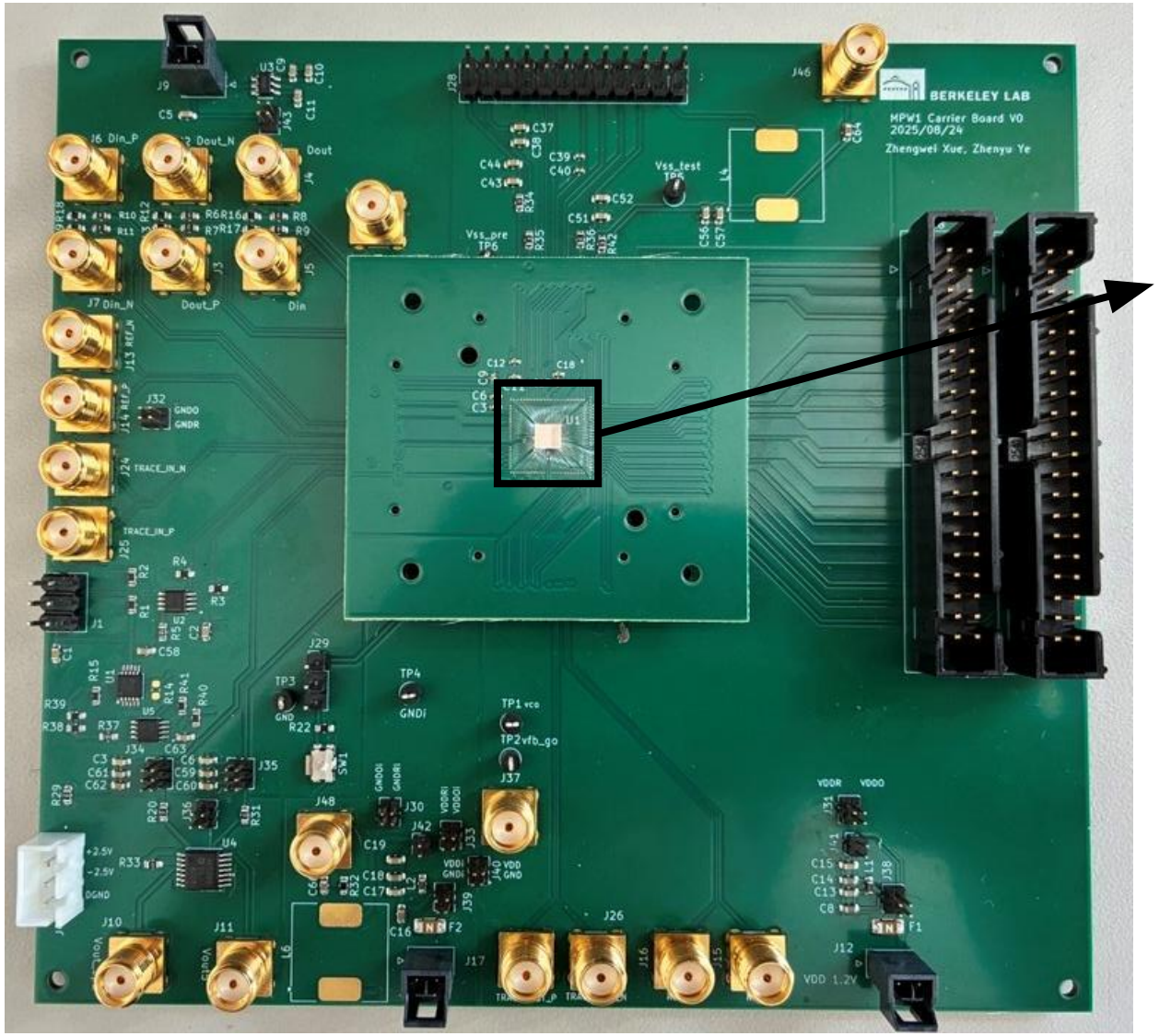
LBNL MWP1 Carrier Board

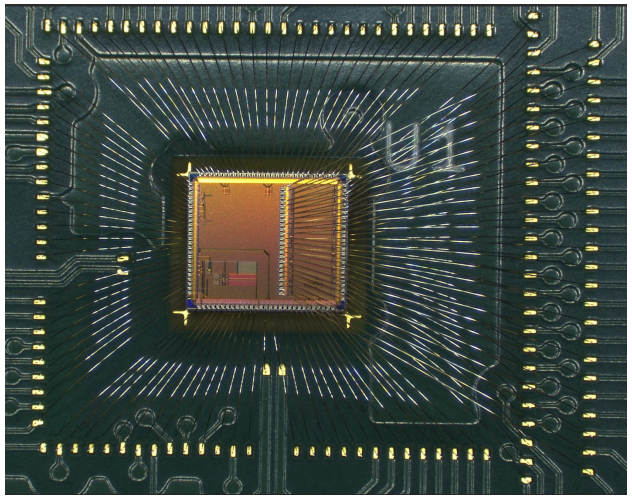


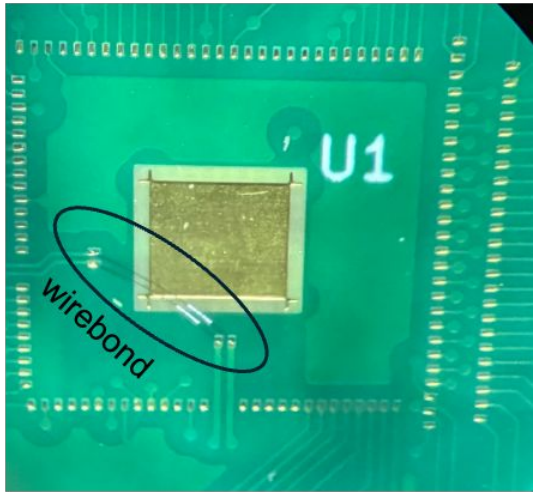


Daughter board

LBNL MWP1 Carrier Board

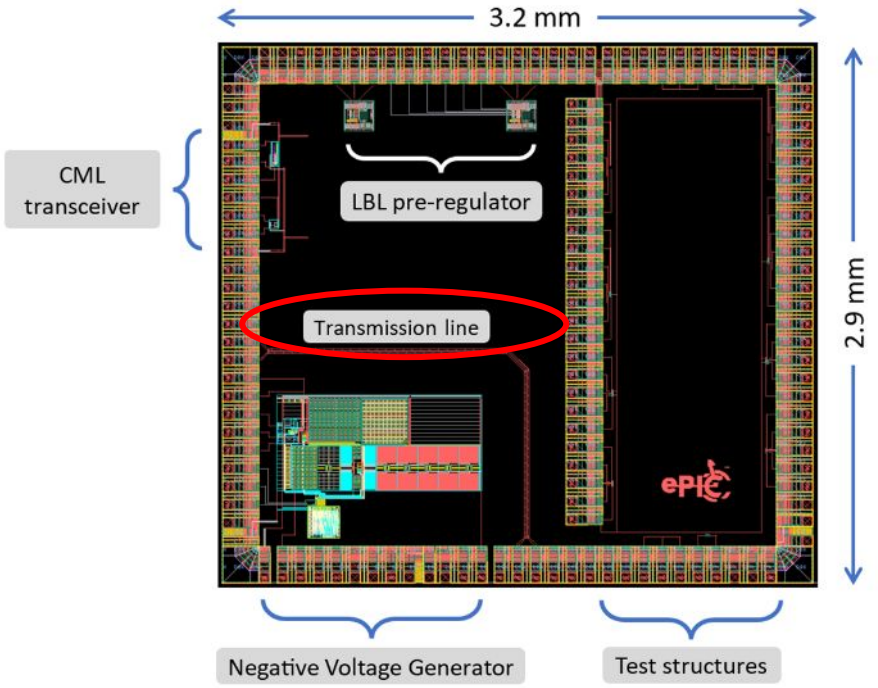




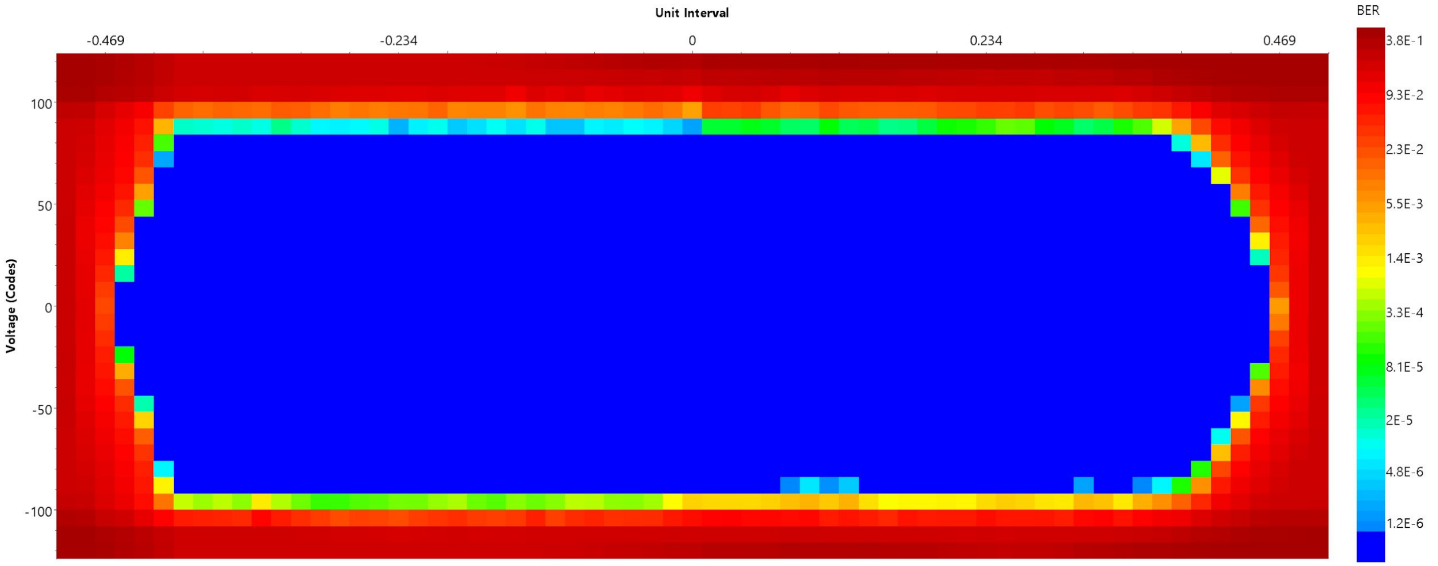


- MPW1 carrier boards (3 mother and 5 daughter boards) delivered to LBL on Oct 24th
- 3 daughter boards with MPW1 mounted, 2 daughter boards with direct wire-bonds (w/o chip)
- 1 set of boards with chip mounted and cables has been sent to BNL on Dec 4th

Transmission line test



- Differential transmission line for testing high-speed data transmission



Summary		Metrics		Settings	
Name:	SCAN_6	Open area:	77248	Link settings:	N/A
Description:	MPW1_D1_1p28Gbps_Ref	Open UI %:	90.77	Horizontal increment:	8
Started:	2025-Nov-11 14:09:26			Horizontal range:	-0.500 UI to 0.500 UI
Ended:	2025-Nov-11 14:09:43			Vertical increment:	8
				Vertical range:	100%

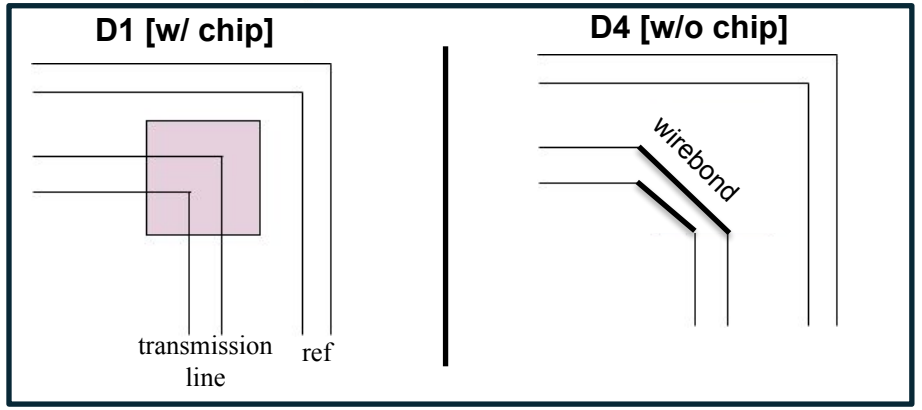
iBERT scan @1.28Gbps

Test Plan:

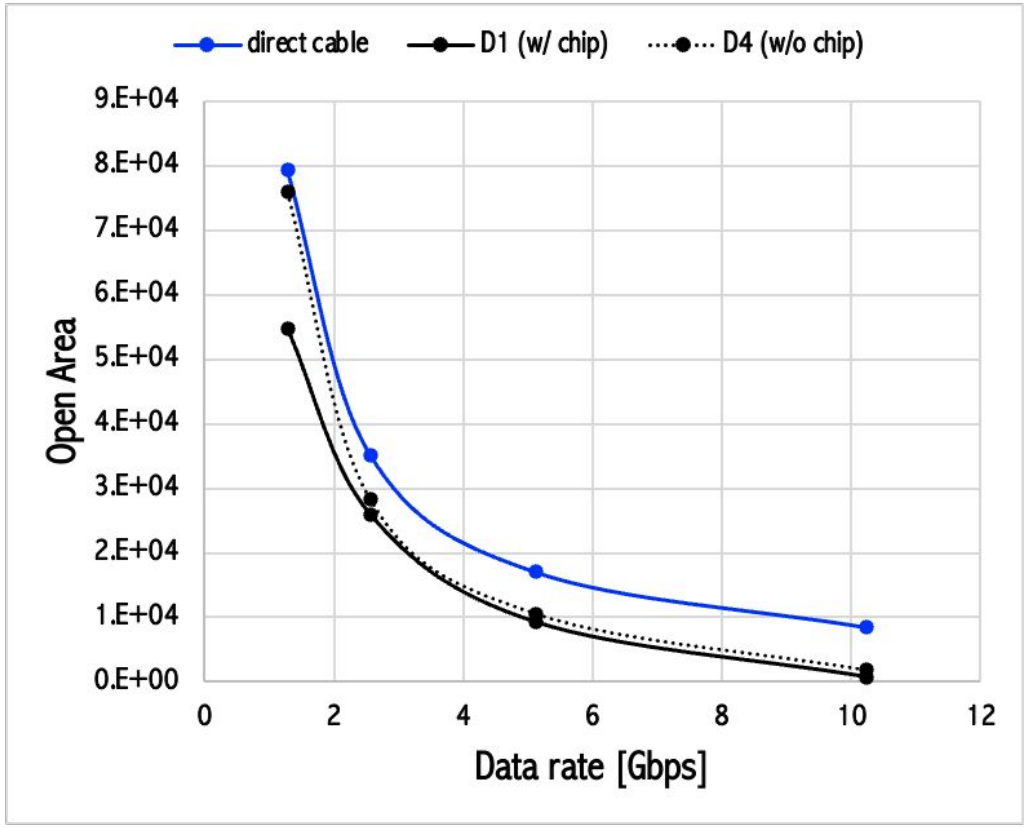
- Eye diagram @different data rates

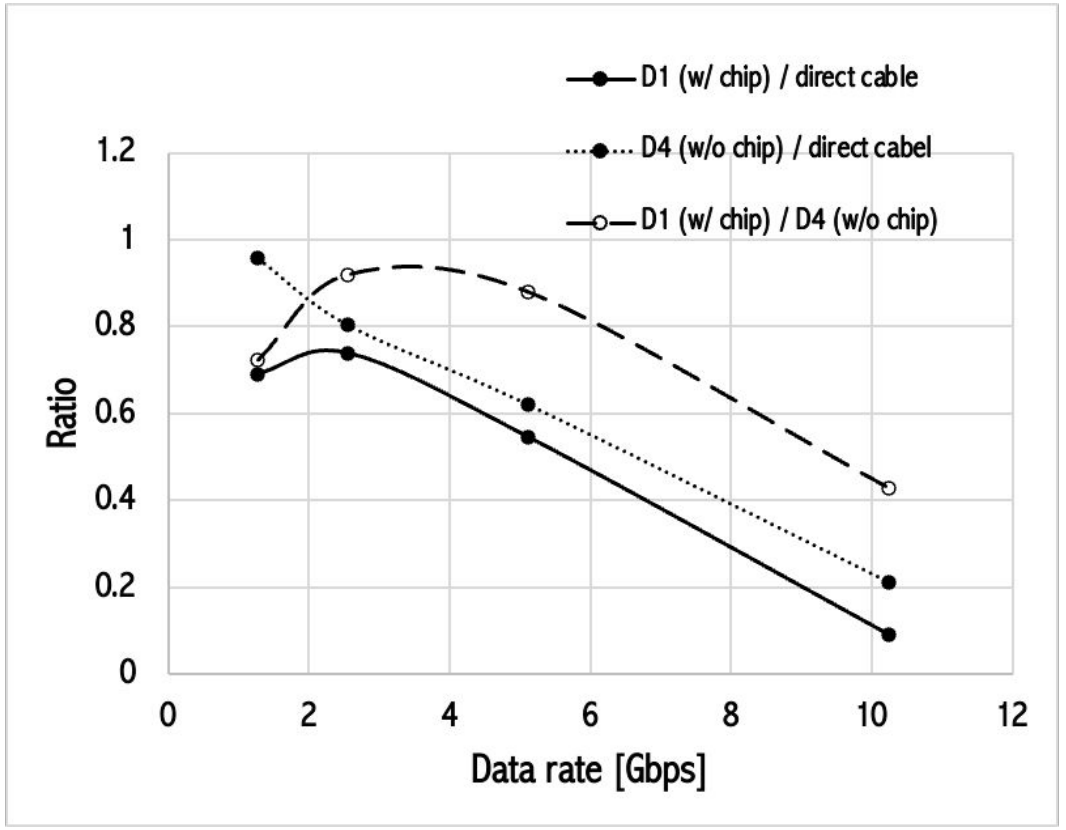
Instrument:

- FPGA for High-speed data generate and eye diagram



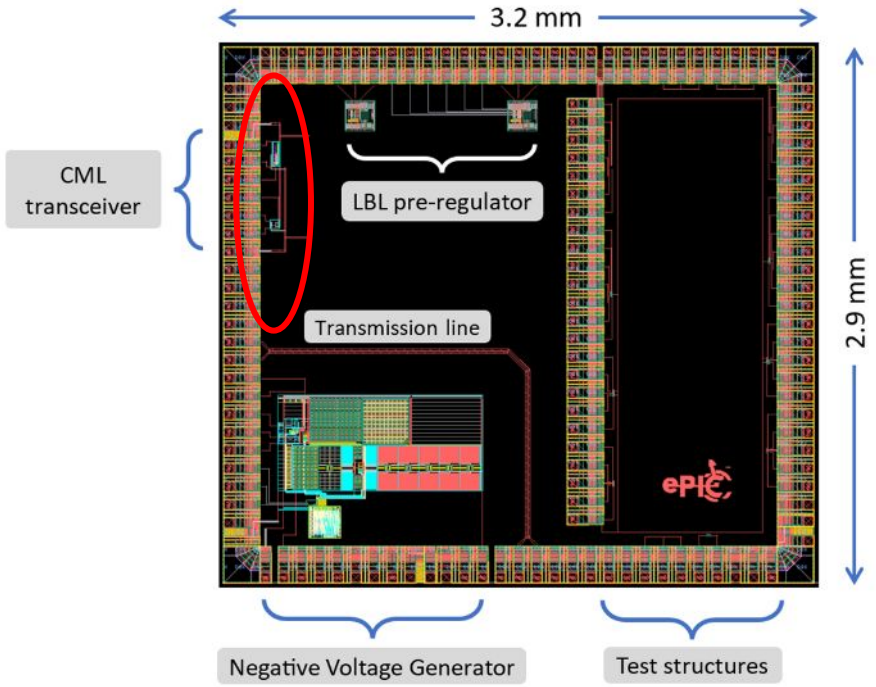
Transmission line test



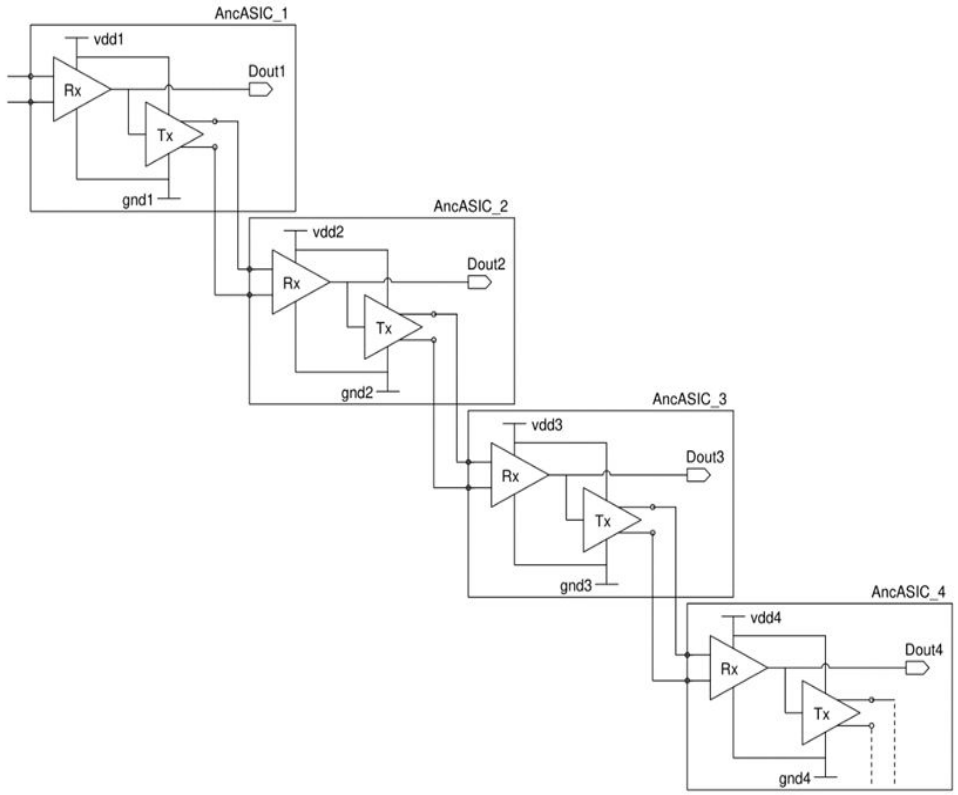


- Open area or ratio sharply decrease with increasing the data rates, similar behavior across all chips tested
- Signal quality of the on-chip transmission line path may be suboptimal/compromised @ high data rates

CML Transceiver



- Designed to enable DC-coupled slow control links between adjacent serially-powered AncASIC chips



Daisy-chain test structure

Test plan:

- Transmission loss, time delay, and eye diagram for **single chip tests** and **daisy-chain tests with DC or AC-coupling** with Tx and Rx under different common voltage.

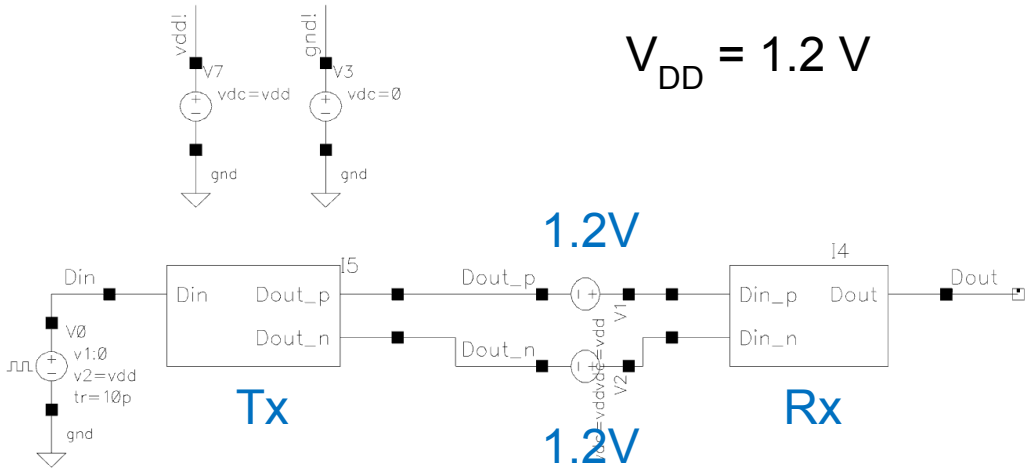
Instrument:

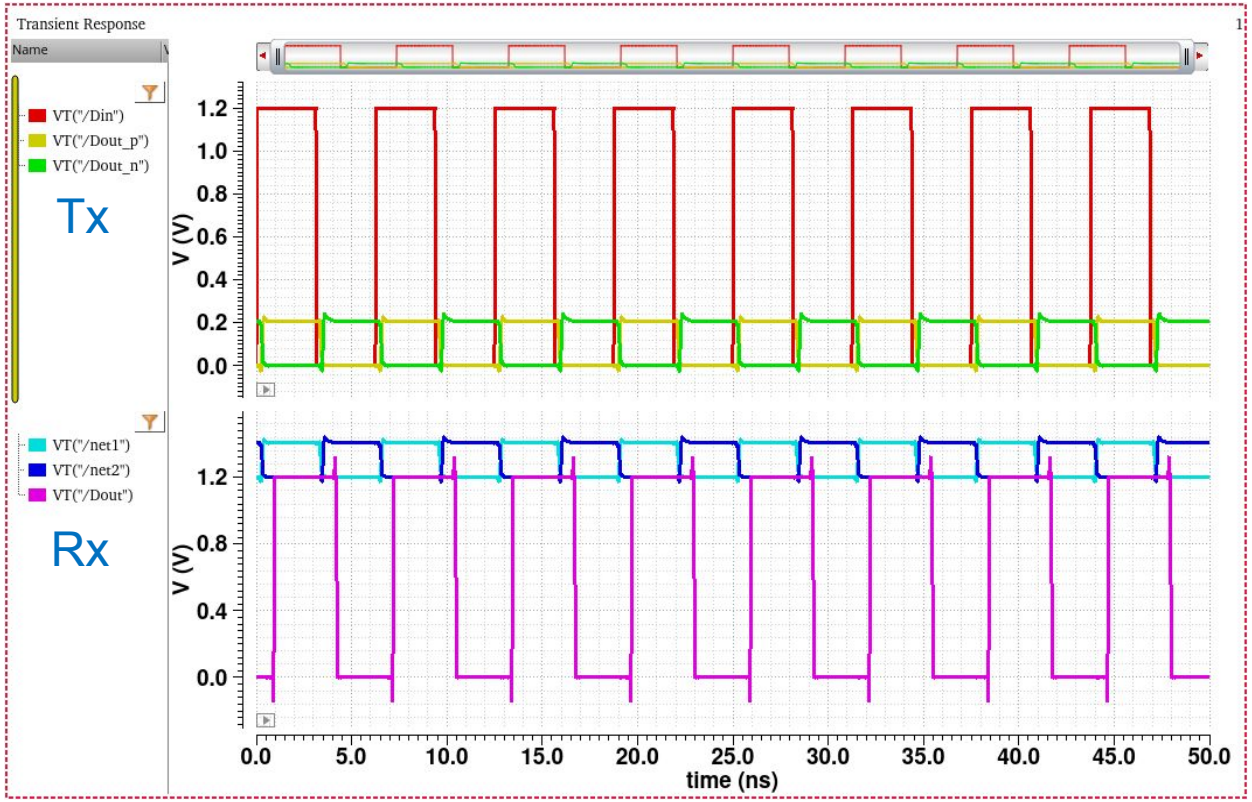
- Power supplies to set different common voltage
- Oscilloscope
- FPGA

CML Transceiver

- Simulation of a DC-coupled link using a simple repeated 0/1 pattern

slide from Soumyajit





- **Transmitter: V_{pp} of $D_{out\_p/n}$ ~ 0.2 V** at V_{DD} = 1.2 V with D_{in} = 0 - 1.2 V from simulation
- **Receiver: V_{pp} of D_{out} ~ 1.2 V** at V_{DD} = 1.2 V with V_{pp} of $D_{in\_p/n}$ = 0.2 V from simulation

CML Transmitter Test

- Transmitter:

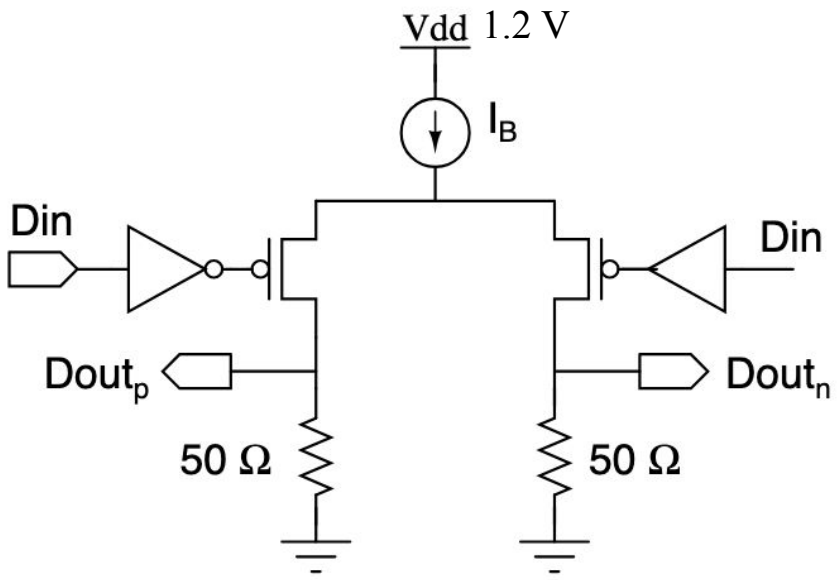
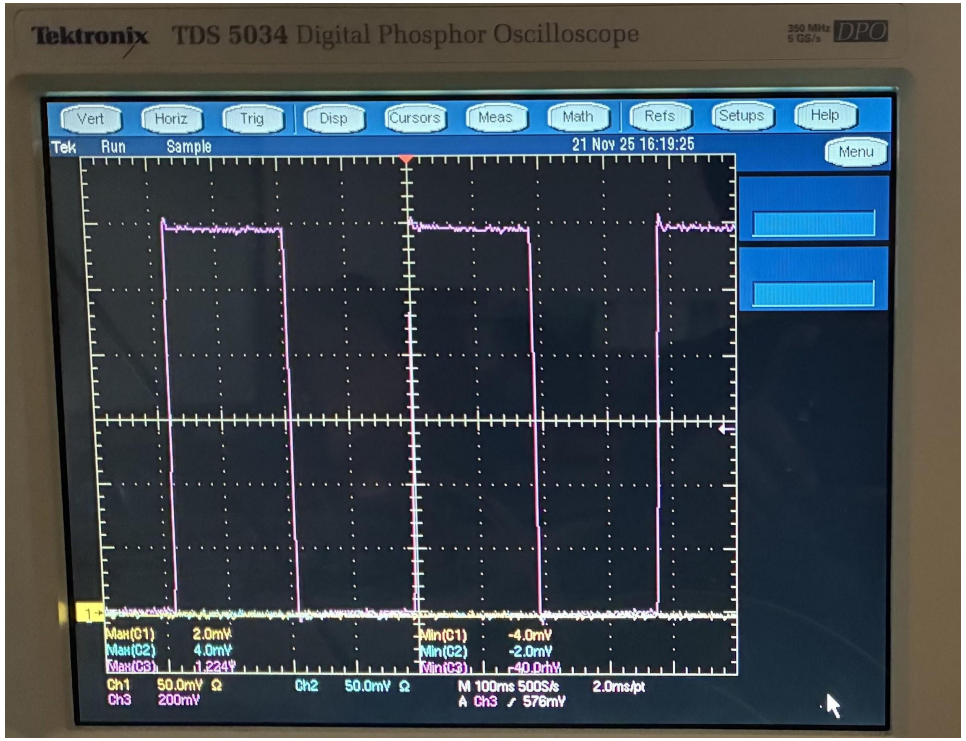


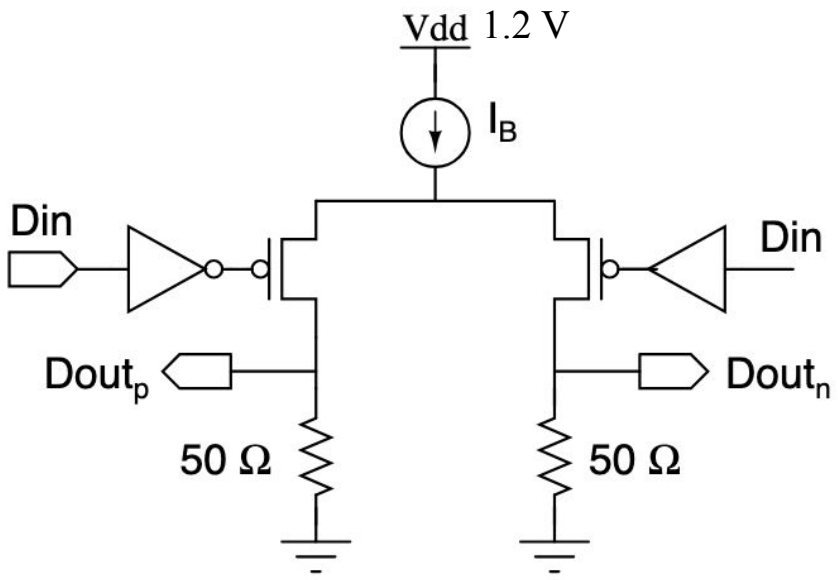
Figure 13: CML transmitter.

- Single-end input from signal generator setting: high-Z, 1MHz square, rail-to-rail 0-1.2V



CML Transmitter Test

- Transmitter:



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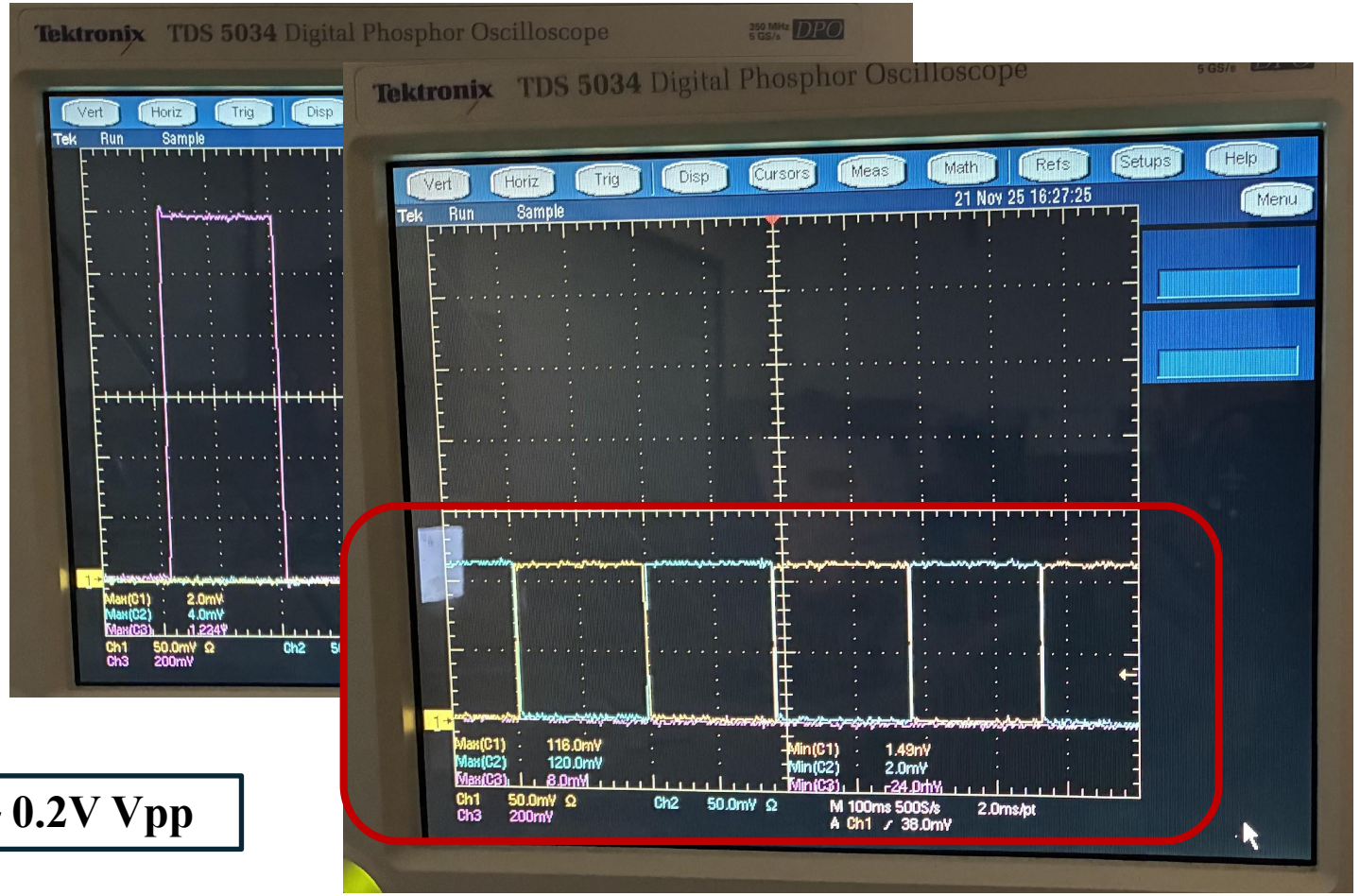
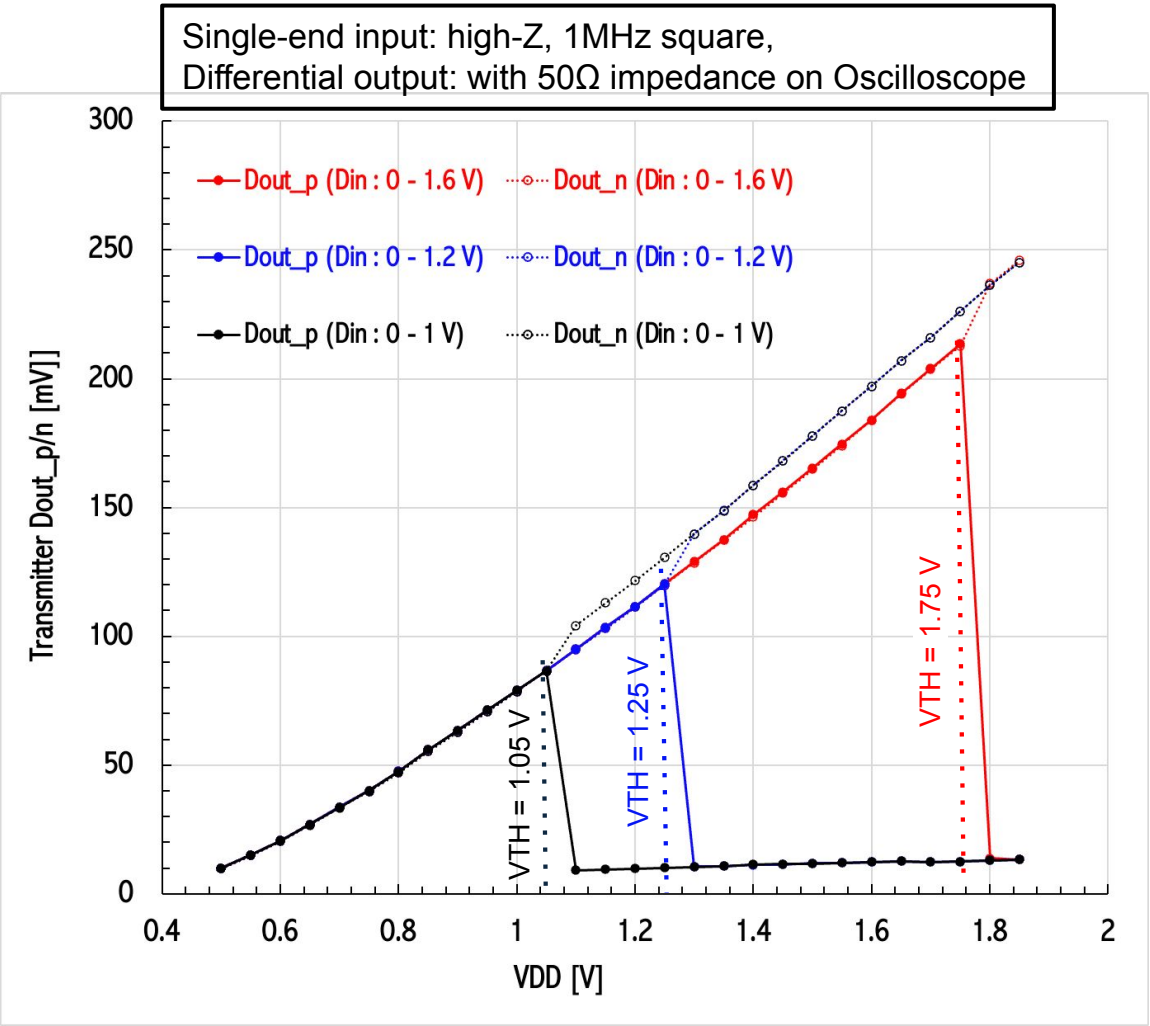


Expected differential output from simulation ~ 0.2V Vpp

- Differential output measured on oscilloscope setting:
  50 Ohms, common mode ~ 0.06V, **amplitude 0.12V Vpp**

CML Transmitter Test

❑ Transmitter:



- We have looked at the transmitter output for different D_{in} (single ended input) amplitudes while increasing V_{DD}
- Differential output $D_{out\_p/n}$ swing amplitude of the transmitter increase with V_{DD} until V_{DD} reaches proximity to the amplitude of D_{in} ($V_{TH,}$ shown as vertical line for each D_{in}).
- At $V_{DD} > V_{TH}$, D_{out_p} drops to zero and D_{out_n} appears as DC (no oscillation) and increase with V_{DD}
- For V_{DD} = 1.7 V and D_{in} = 0 - 1.6 V, **V_{pp} of $D_{out\_p/n}$ ~ 0.2 V**
- For V_{DD} = 1.2 V and D_{in} = 0 - 1.2 V, **V_{pp} of $D_{out\_p/n}$ ~ 0.12 V**
- Expected **V_{pp} ~ 0.2 V** at V_{DD} = 1.2 V with D_{in} = 0 - 1.2 V for the differential output $D_{out\_p/n}$ **from simulation**

CML Receiver Test

- Receiver:

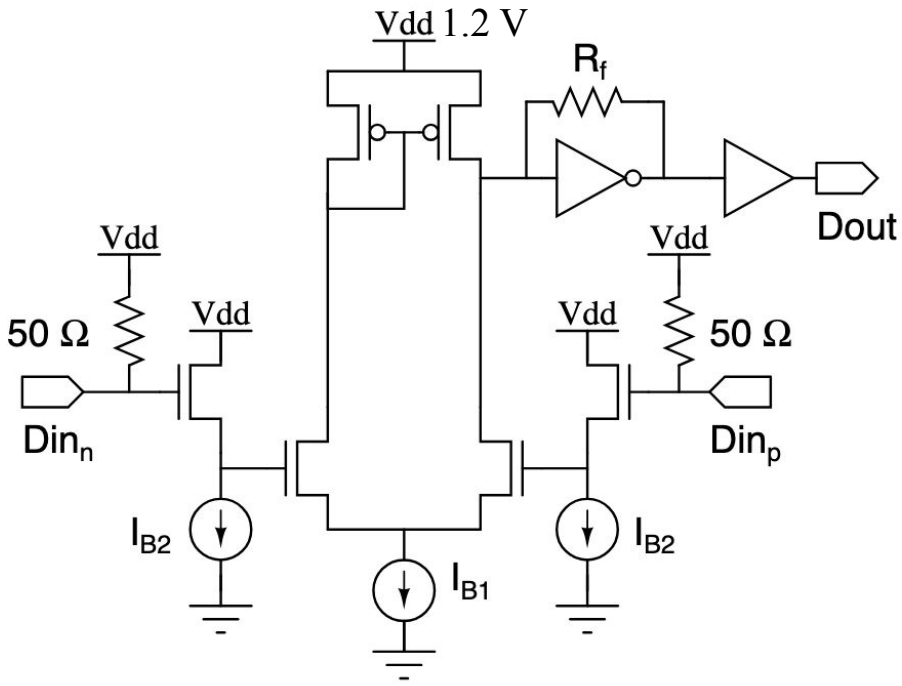


Figure 14: CML receiver.

- Differential input from signal generator setting:
  50 Ohms, 1MHz square, common mode 1.1V, amplitude 0.2V Vpp

CML Receiver Test

- Receiver:

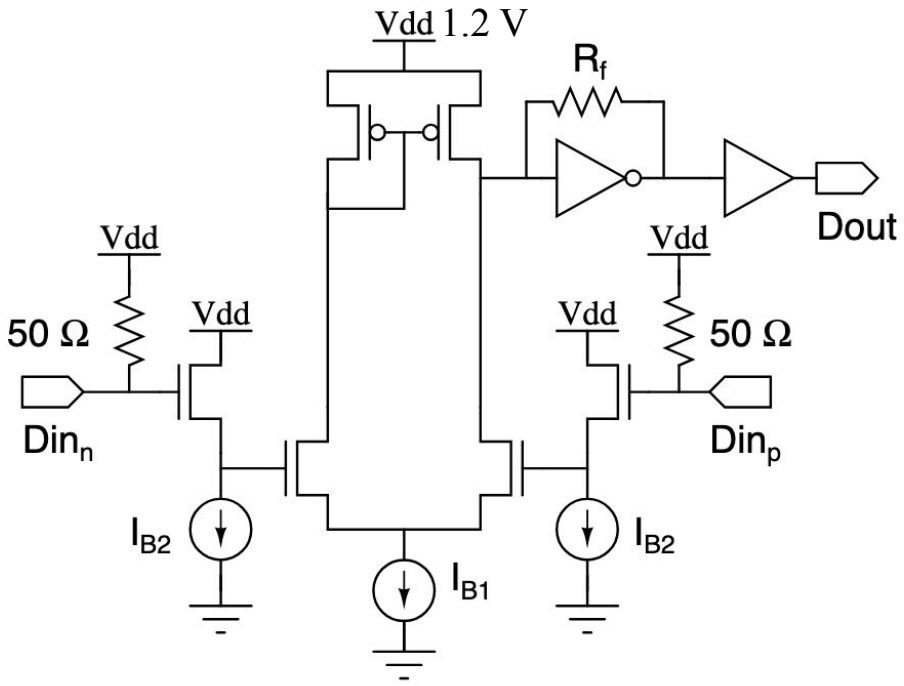
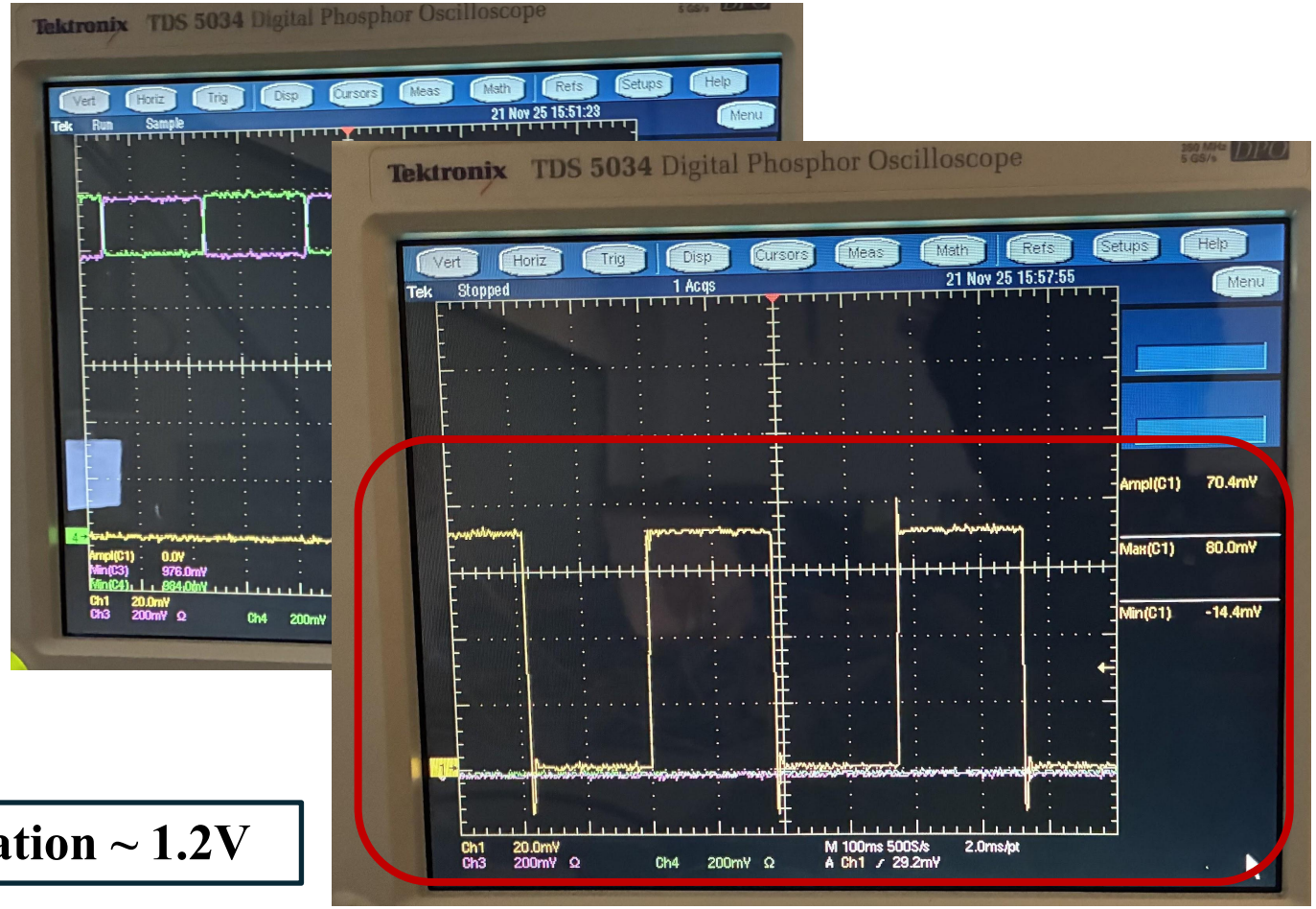


Figure 14: CML receiver.

Expected single-ended output from simulation ~ 1.2V

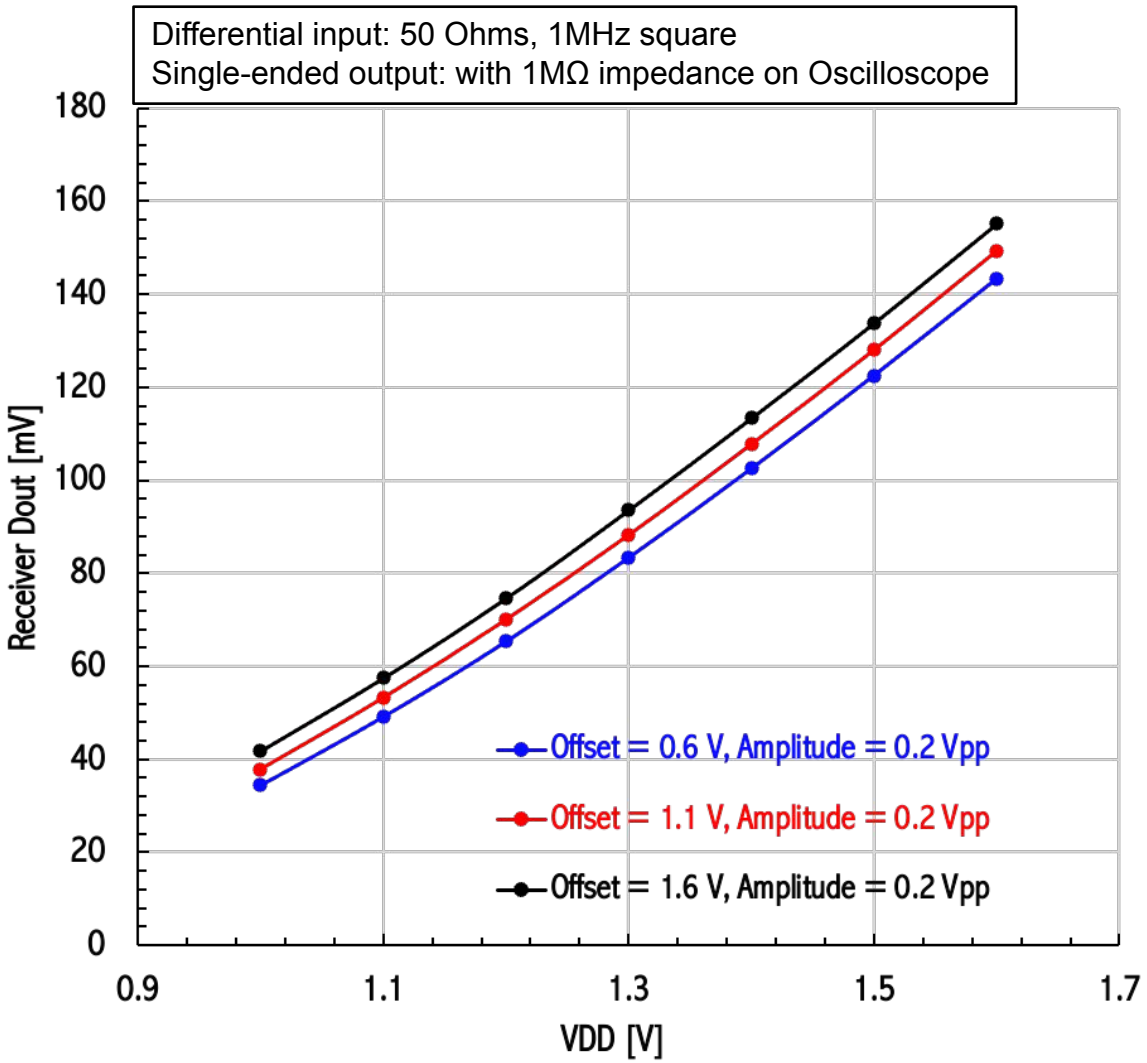
- Differential input from signal generator setting:
  50 Ohms, 1MHz square, common mode 1.1V, amplitude 0.2V Vpp



- Single-end output measured on oscilloscope setting:
  1M Ohms, **0-0.07V rail-to-rail**

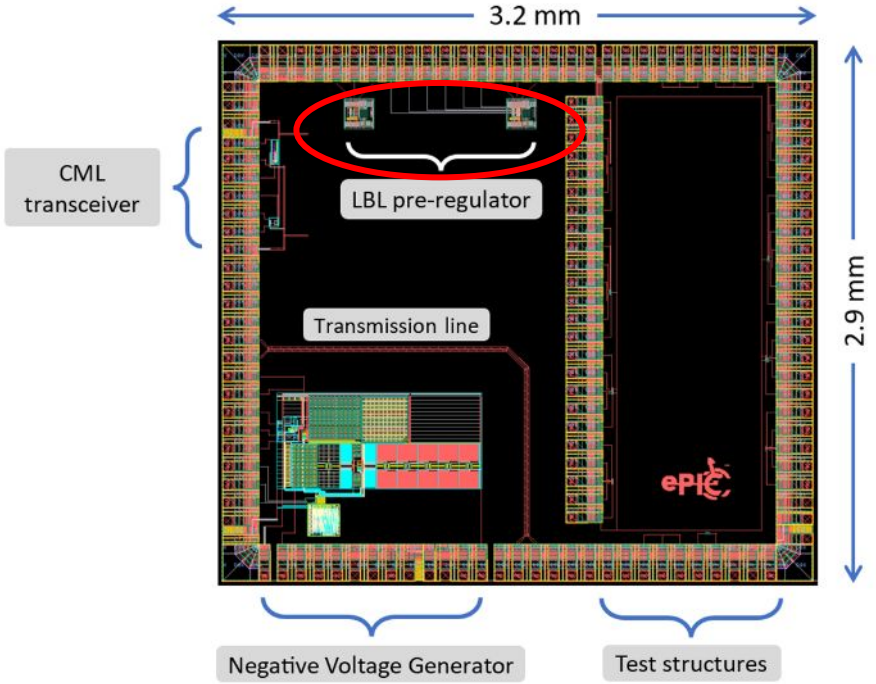
CML Receiver Test

❑ Receiver:



- We have also looked at the receiver output D_{out} for $D_{in\_p/n}$ at different common mode (offset) while increasing V_{DD}
- Single-ended output D_{out} increases with V_{DD}
- An increment of ~ 10 mV in D_{out} is observed when changing the offset (common mode voltage) of $D_{in\_p/n}$ from 0.6 to 1.6 V at fixed V_{DD}
- For V_{DD} = 1.6 V, **V_{pp} of D_{out} ~ 145 - 155 mV**
- For V_{DD} = 1.2 V, **V_{pp} of D_{out} ~ 65 - 75 mV**
- Expected **V_{pp} of D_{out} ~ 1.2 V** at V_{DD} = 1.2 V with V_{pp} of $D_{in\_p/n}$ = 0.2 V **from simulation**

SLDO Pre-Regulator



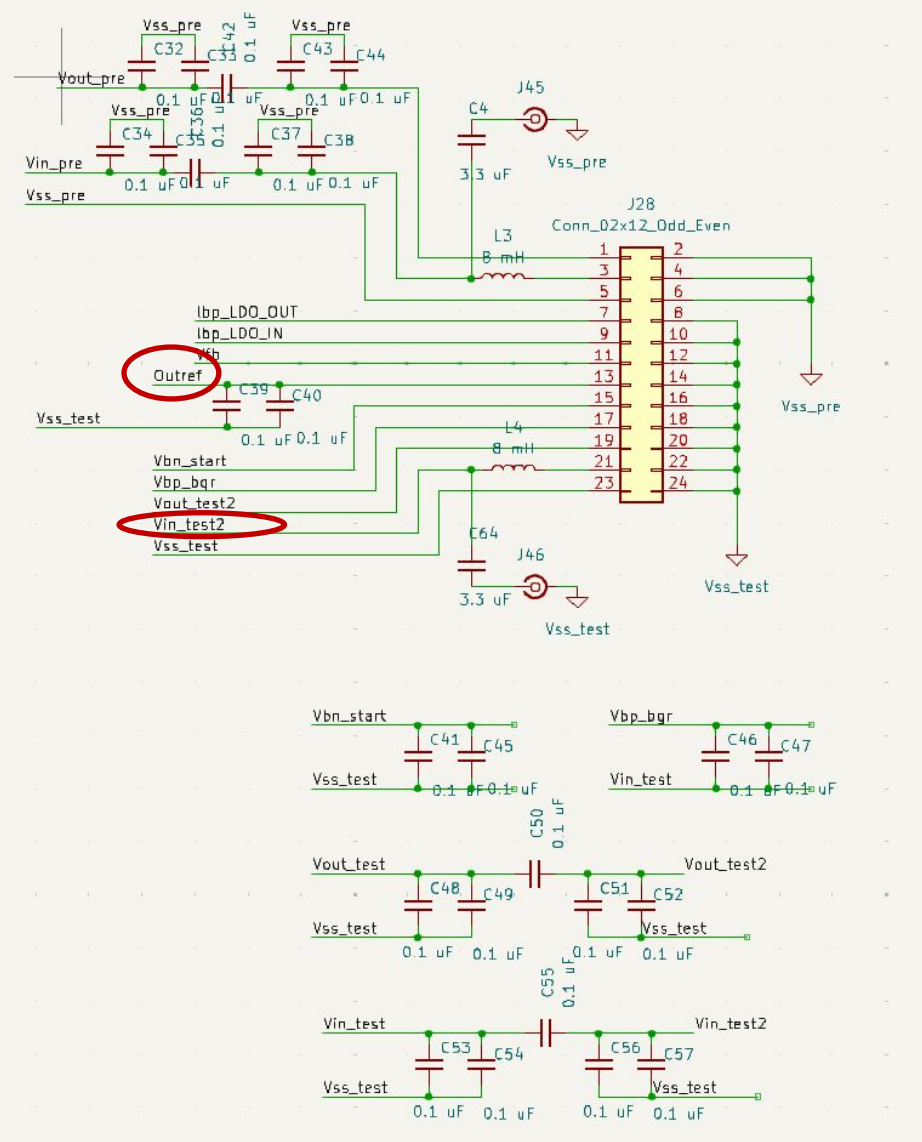
Test Plan:

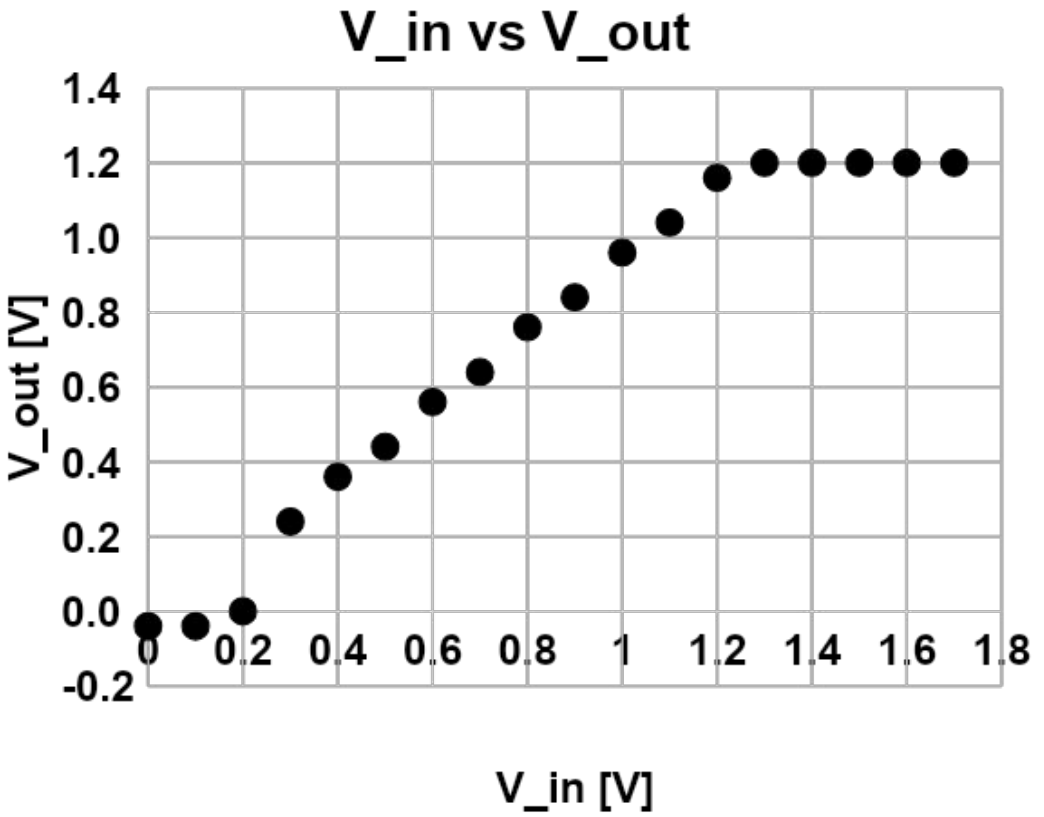
- **Start-up:** Plot the Vin and Vout signal response while ramping the Vin at specified rates. Determine the voltage at Vin and Vout where the Vout response stabilizes (flat). Vin: ramp 0 to 1.7V; Ramp rates 0 to 1.7V: 10u , 100u, 1m, 10m, 100m, 1s
- **Output Ripple/Noise:** Measure the RMS noise on Vout with Vin at 1.7V using an instrument math function, or with a true-RMS noise meter. Plot Vout at 10 mV full scale at time scales 10 ms, 1ms, …, 1 us per division.
- **PSRR and line regulation:** With Vin at 1.7V plot the Vin and Vout signal response while asserting a 10 mV step on Vin. Measure the DC value of both signals before and after the step. If equipment is available, sweep Vin from 10 Hz to 10 MHz at a DC offset of 1.7V at an AC amplitude of 10 mV and plot the Vout response.
- **Transient Response (overshoot and settling time):** ESR - 3.5k; With Vin at 1.7V plot the Vout signal response while switching a +/- 100uA load onto Vout. Measure the DC value of both signals before and after the step.
- **Load Capacitance:** Repeat the start-up ramping test at the 1pF, 10pF, 100pf, 1nF.
- **Temperature:** Repeat the start-up ramping test at -30 C, 0 C, 60 C, 90 C

Instrument:

- Power supply
- Oscilloscope
- Signal generator to power VDD with ripple
- Environmental chamber for temperature test

SLDO Pre-Regulator

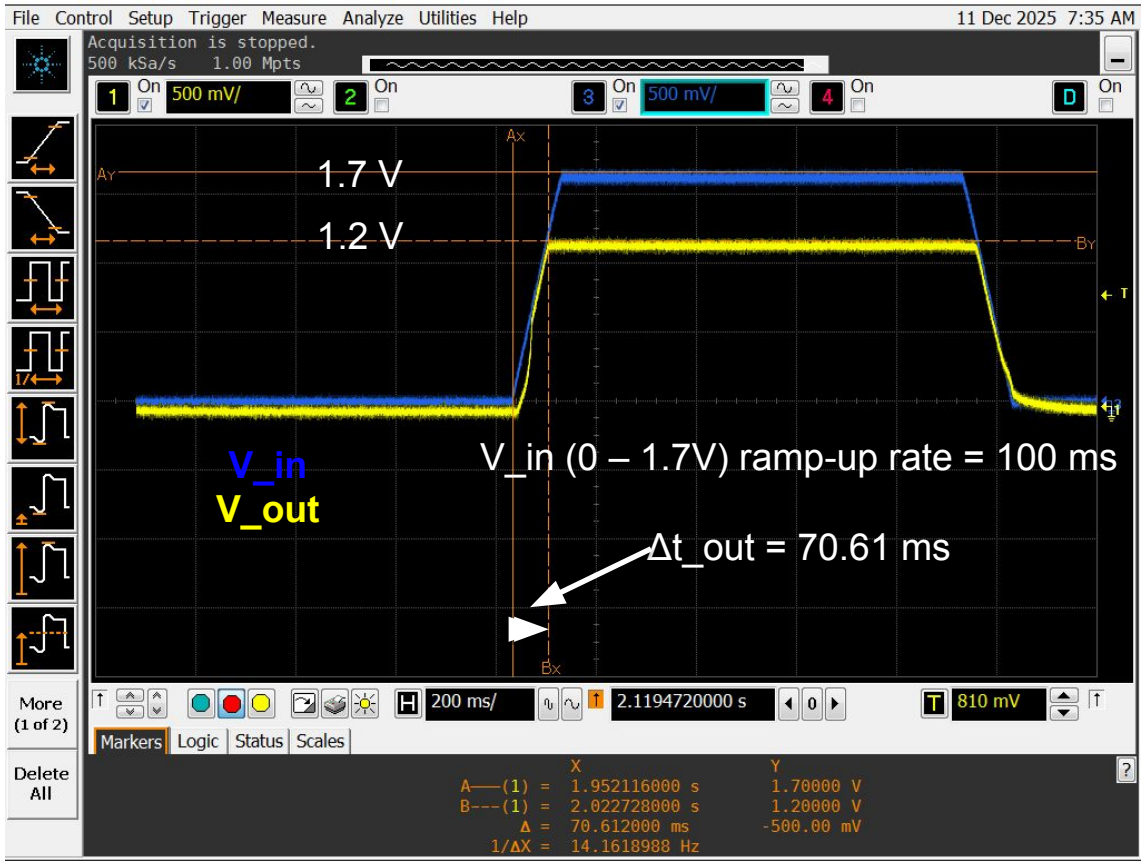




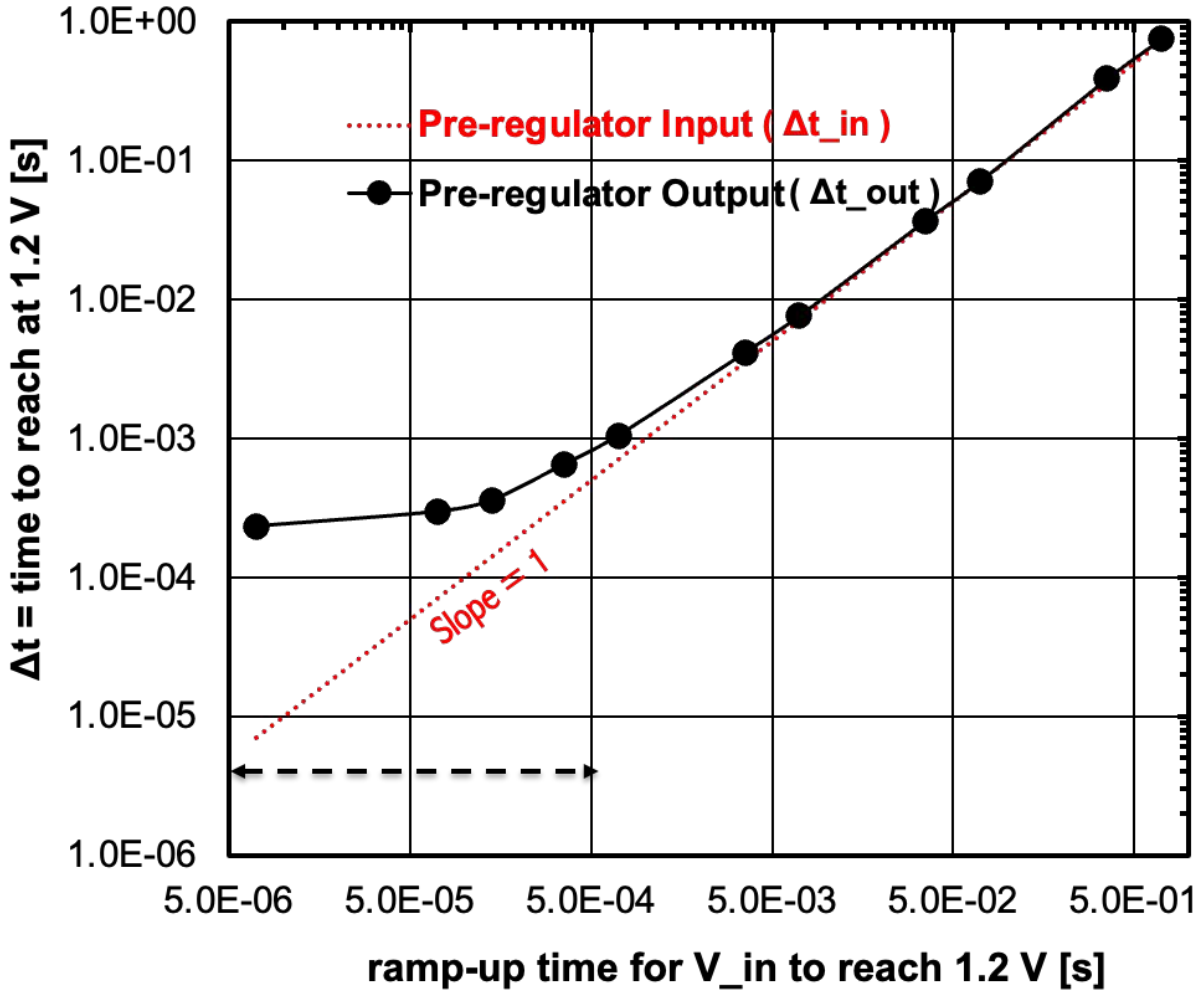
- Linear increase in V_outref with Vin_test2 below ~ 1.2 V
- **V_outref stabilize ~ 1.2V**

SLDO Pre-Regulator

- Used ‘burst’ mode of the oscilloscope to have one ramp-up, i.e., without repeating function
- Extracted Δt_out (Δt_in) for pre-regulator V_out (V_in) when both ramp-up from 0 to 1.2 V
- Repeated the measurements for different ramp-up rates for the V_in from 0 to 1.7 V



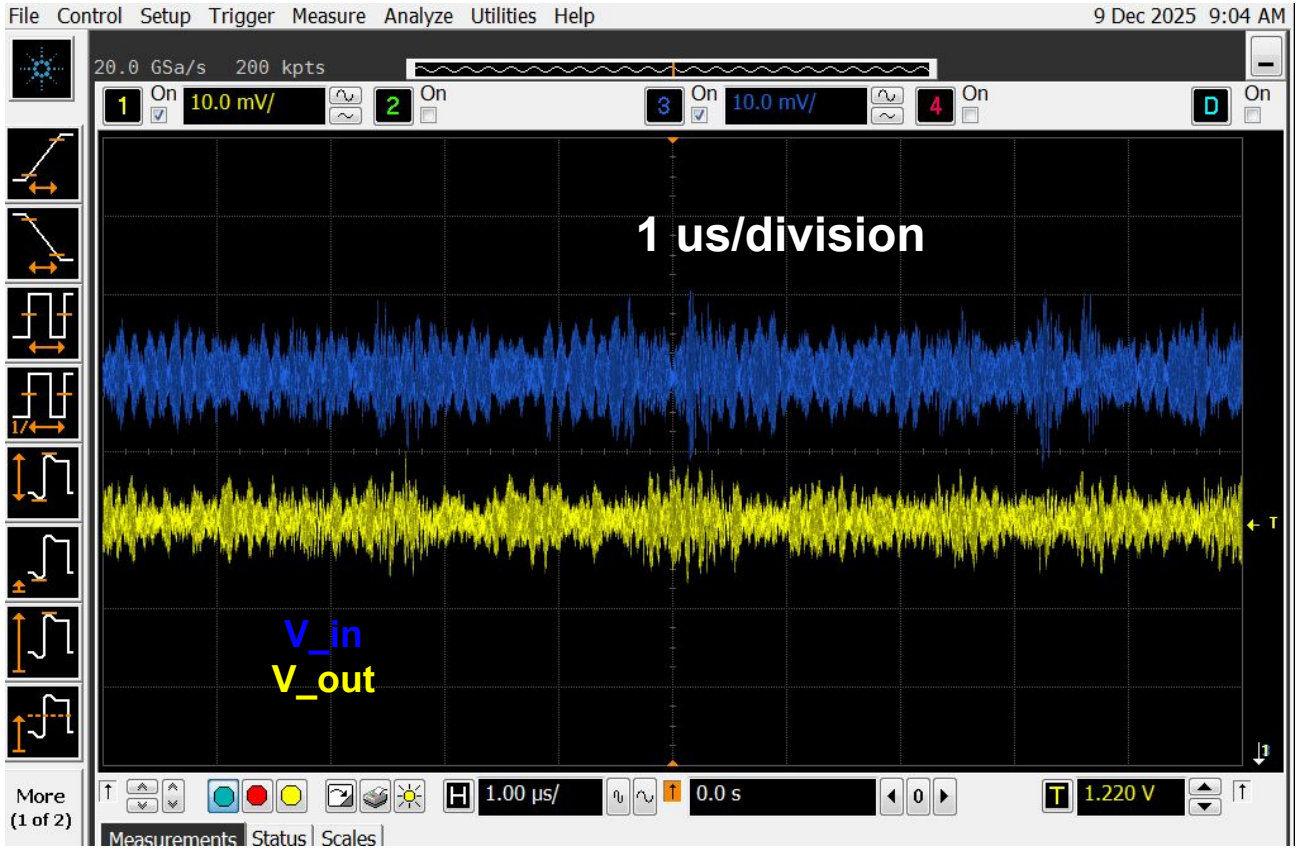
SLDO Pre-Regulator



- Repeated the measurements for different ramp-up rates for the V_in from 0 to 1.7 V
- Δt for pre-regulator output follows well the input when ramp-up time for V_in from 0 to 1.2 V > 500 us
- **Below the ramp-up time of 500 us**, the pre-regulator output ramp-up time, minimum **Δt_out ~ 300 us**
- We will investigate if this is output load dependent

SLDO Pre-Regulator

Output Ripple/Noise:



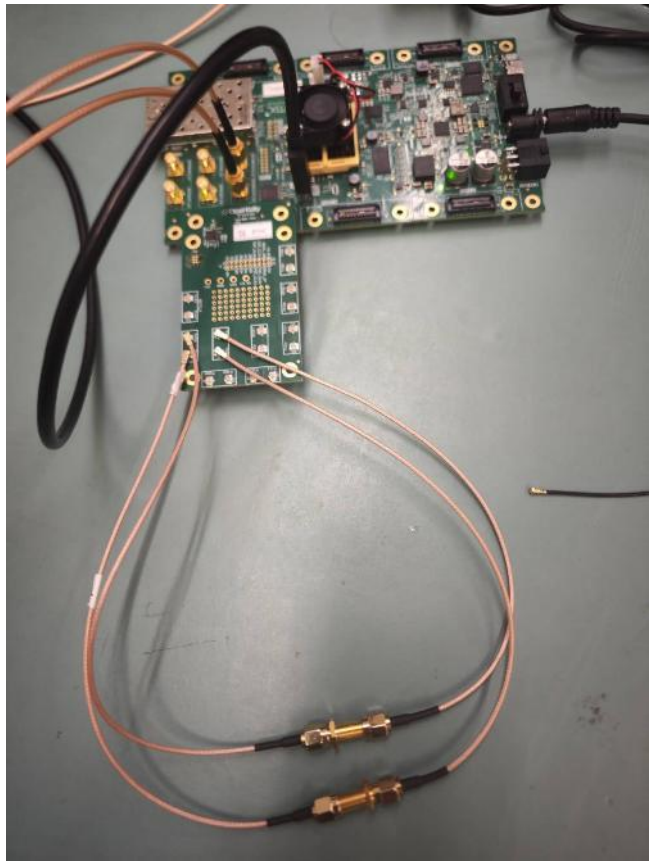
- V_in were set at 1.7 V and used 10 mV full scale in the oscilloscope
- Measured noise at different time scale, starting from **1 us/division to 100 ms/division**
- No significant changes in noise value observed between different time scales per division
- **Noise** value for **Vin (~2.6 mV)** is slightly higher than noise in **Vout (~ 2.0 mV)**

Summary and Outlook

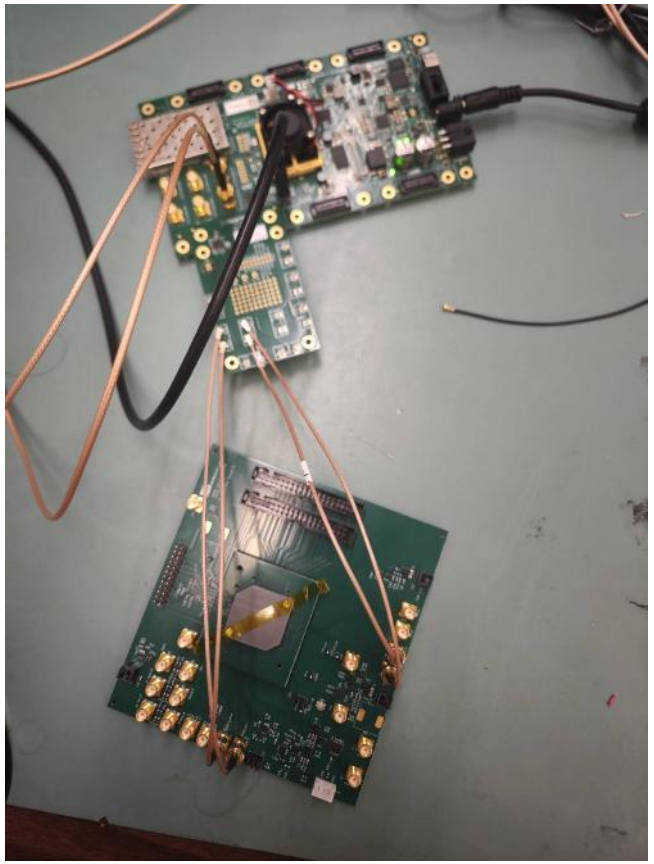
	Status	Initial Results
Transmission Line	alive	Signal quality of the transmission line path may be suboptimal @ high data rates
CML Transceiver	alive but output amplitudes much lower than expected	Differential output for transmitter ~ 0.12Vpp (from simulation ~ 0.2 Vpp, 2X higher than observed) Single-ended output for receiver ~ 0-0.07V rail-to-rail (~ 1.2 V from simulation, 20X times higher than observed)
SLDO Pre-regulator	alive and results consistent with expectation so far	V_out stabilize at ~ 1.2 V with noise ~ 2 mV, follows the input ramp up well > 500 us
I2C Controller	alive	in discussion with BNL designers
NVBG	alive	need I2C to work

Extra Slides

Transmission line test

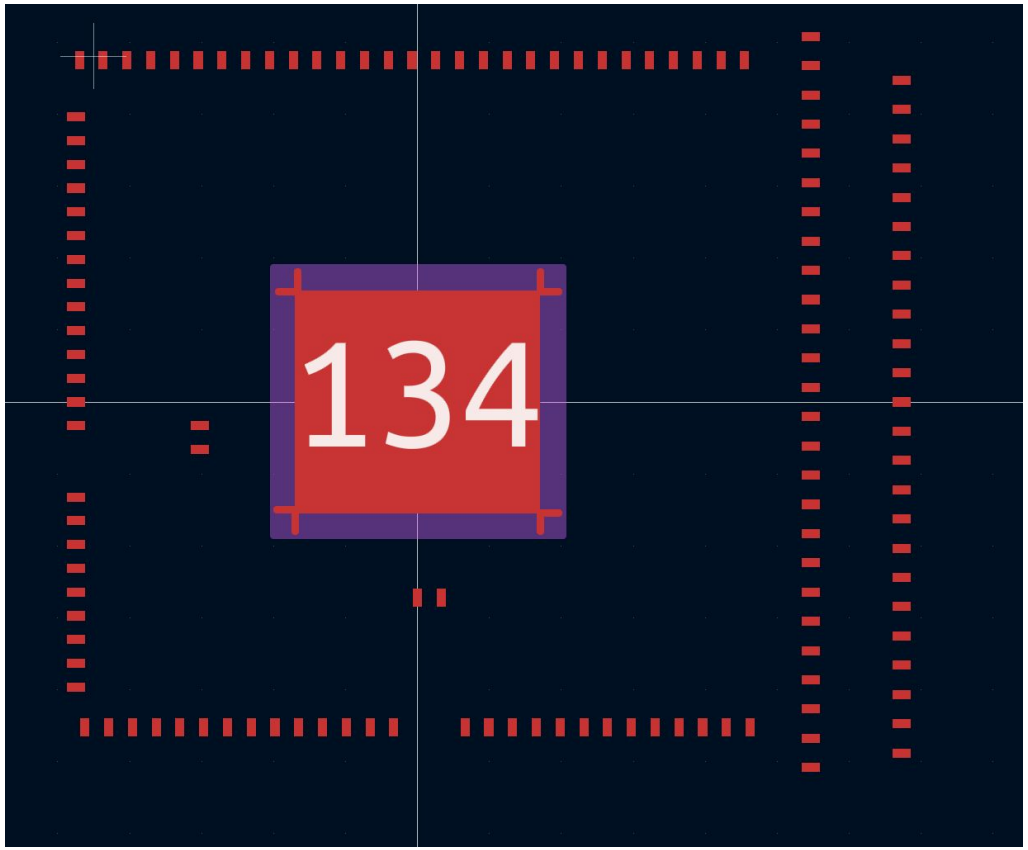


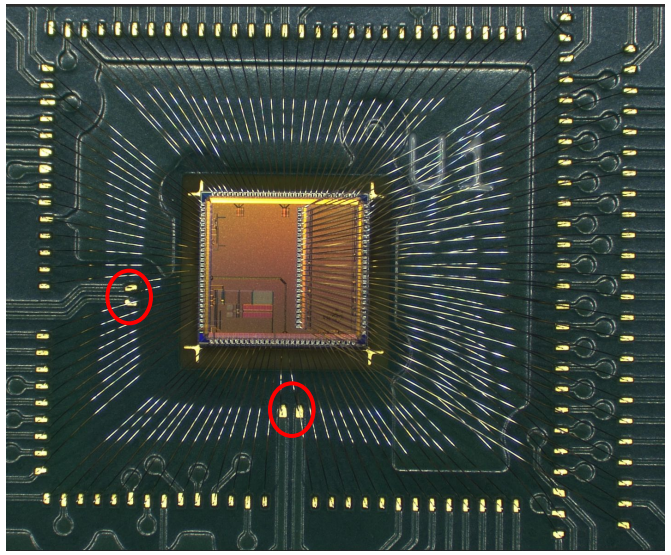
Directly connected



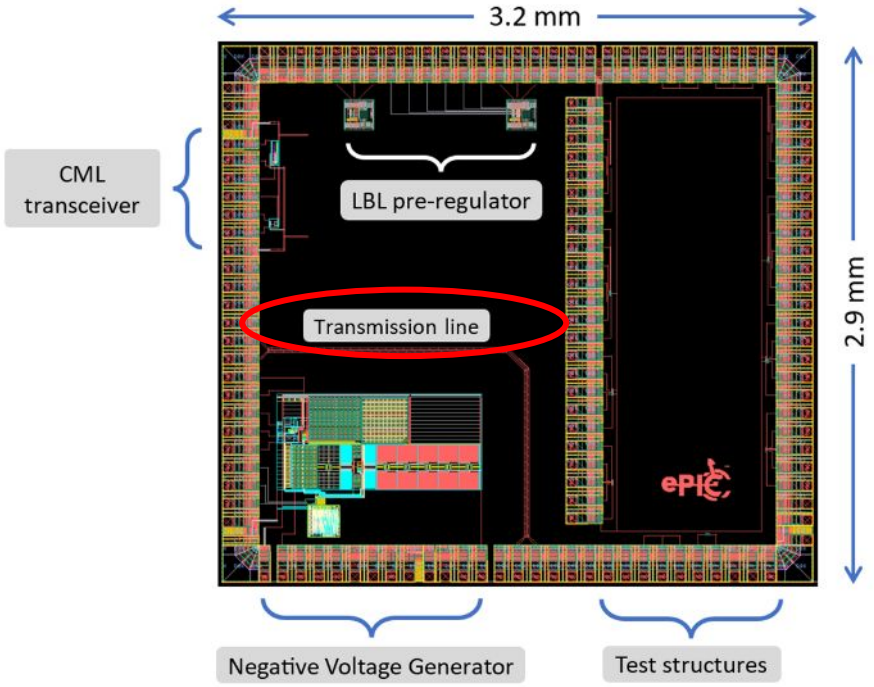
The signal travels along the traces on the MPW1.

Transmission line test





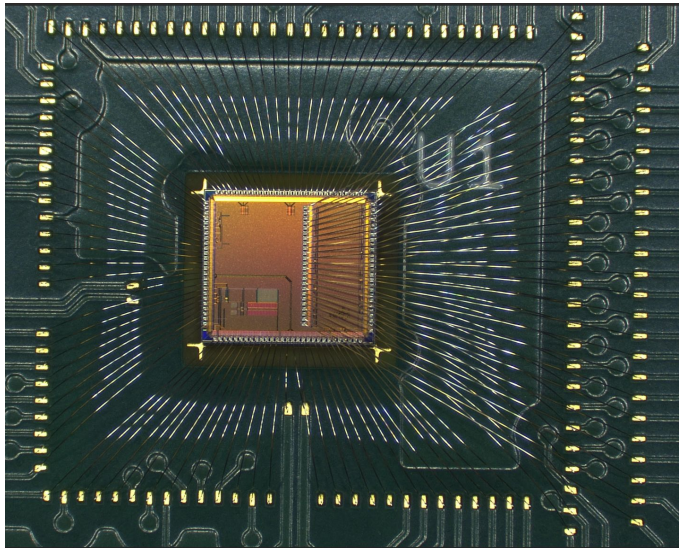
- Requested to direct wire bond between the pair of pads
- Repeat the Eye scan for this configuration and compared with Ref and MPW1 results



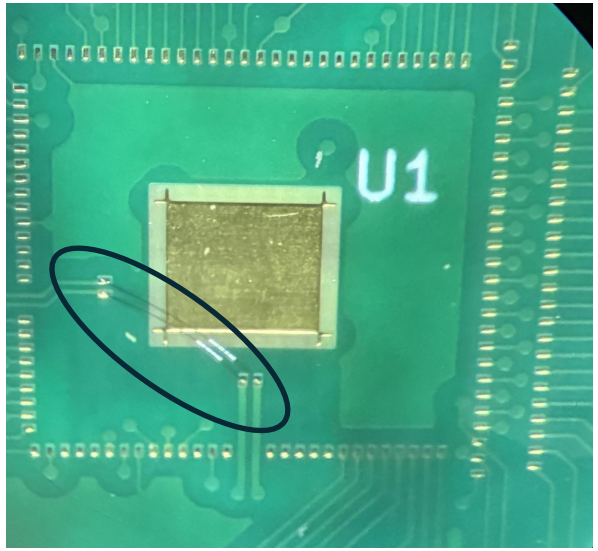
"Trace" (actual "transmission line"): differential trace of transmission line

"Ref": a pair of differential trace close to trace of transmission line

D1/D2/D3 [w/ chip]

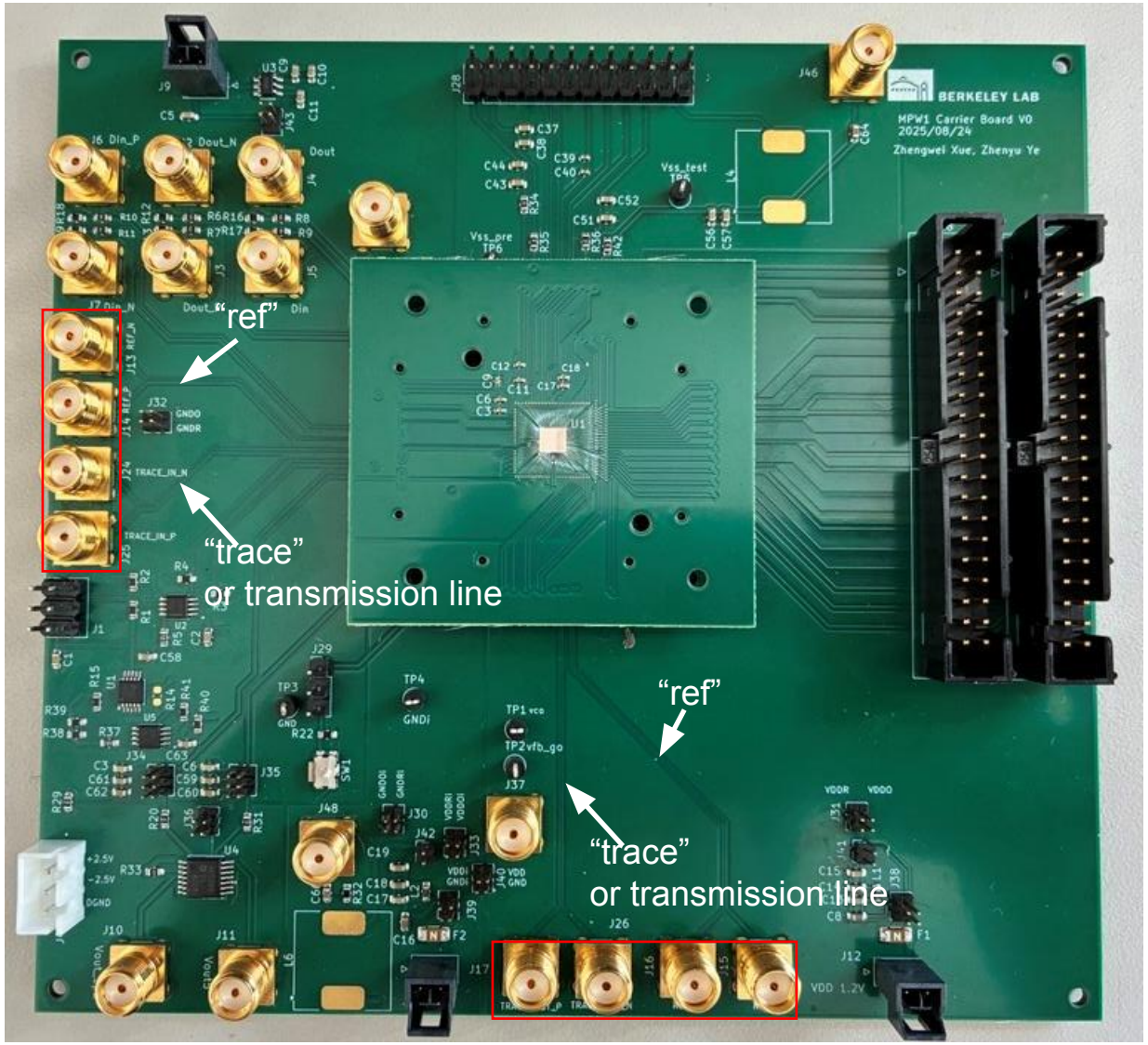


D4/D5 [w/o chip]



MWP1 Carrier Board

Input for “trace” and “ref”



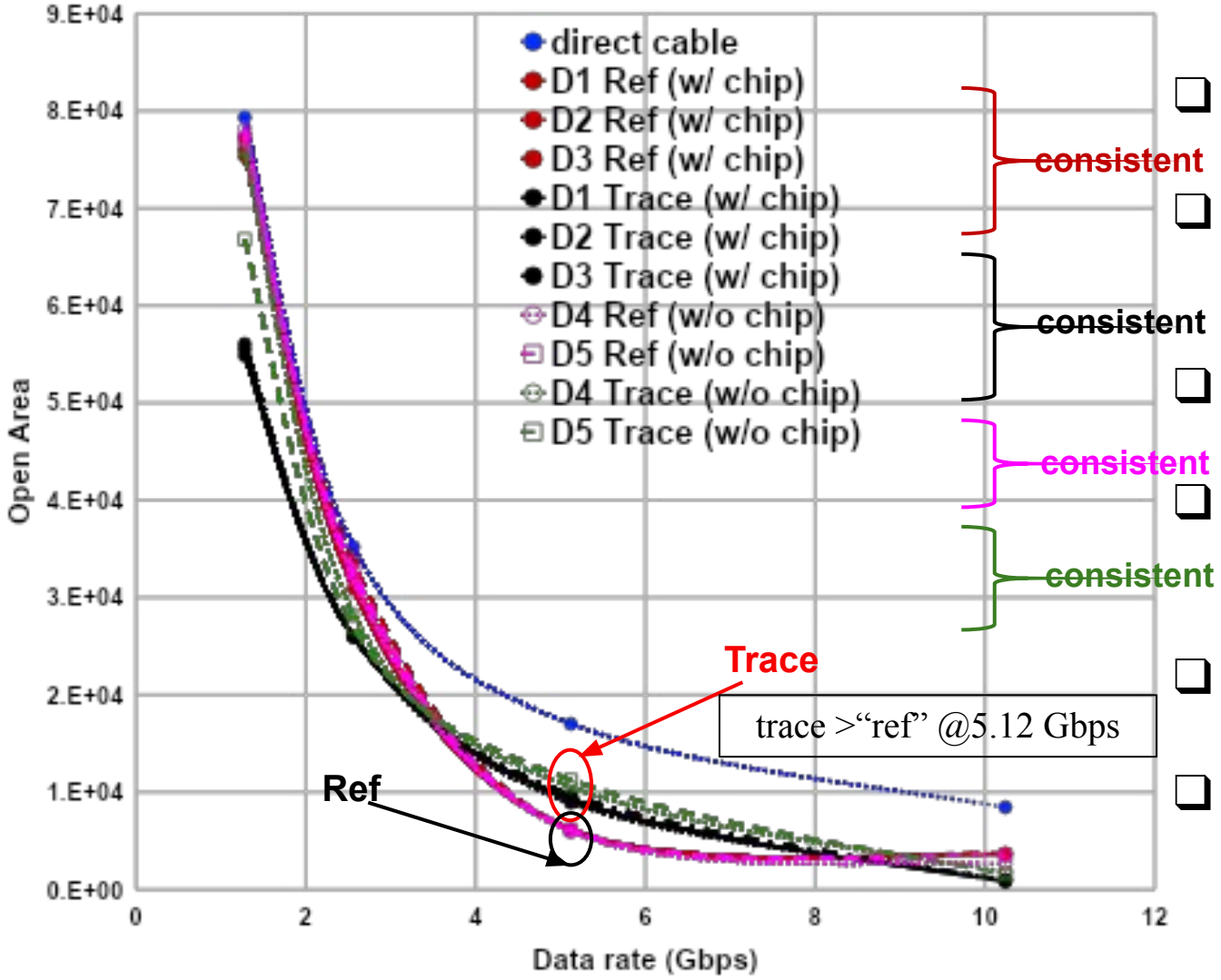
Output for “trace” and “ref”

“Trace” (actual “transmission line”): differential trace of transmission line

"Ref”: a pair of differential trace close to trace of transmission line

Both “Trace” and “Ref” run over the mother board and via daughter board

Transmission line test

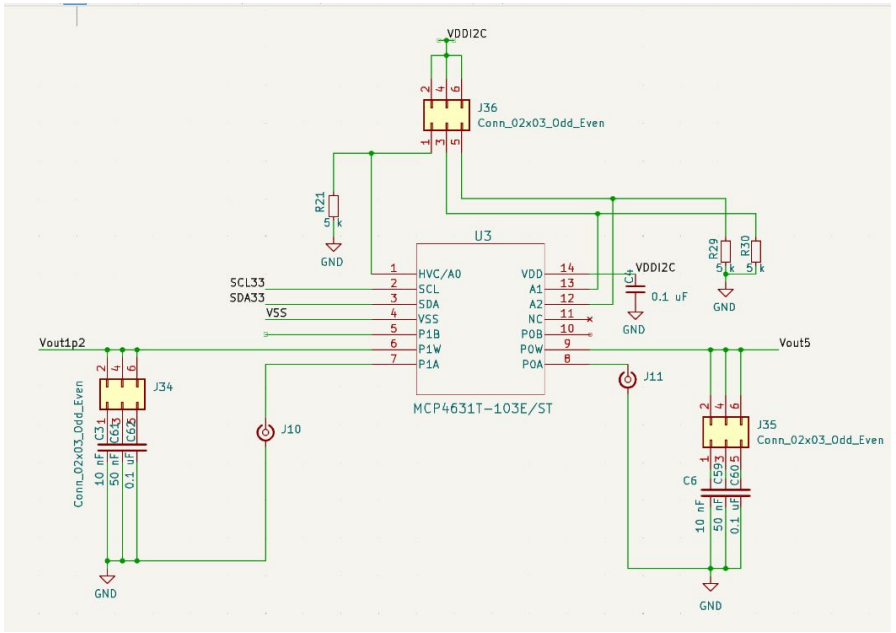


- Open area decrease with increasing data rates
- Open area for "ref" > "transmission line" (exception @5.12 Gbps)
- Results consistent across all MPW1 tested
- Two daughter boards tested w/o MPW1 mounted, direct wire bond across the transmission line trace
- "ref" consistent between w/ and w/o chip
- Slightly higher open area for w/o chip compared to w/ chip across the transmission line

Negative Voltage Generator

Test Plan:

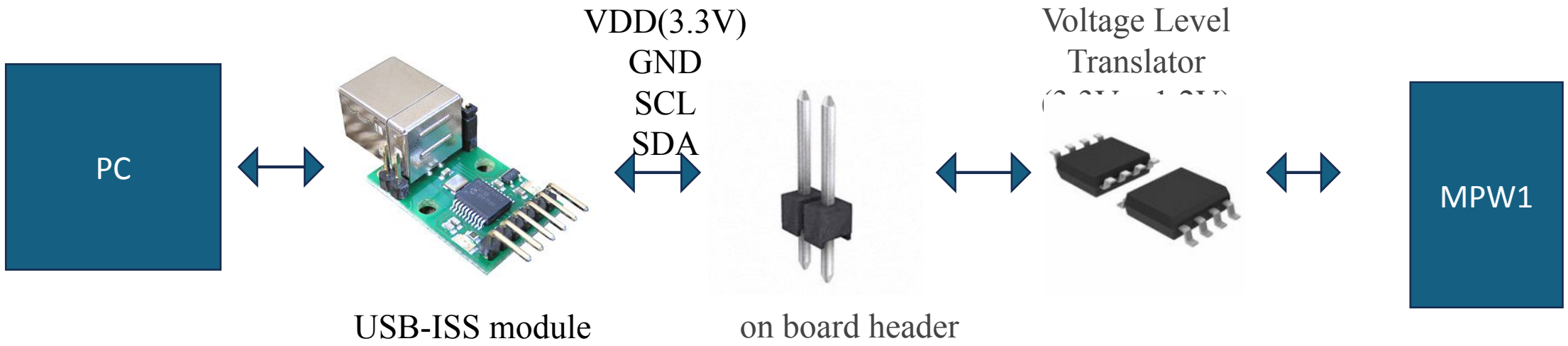
- **Output range**
  Change Verf, verify:
  $V_{OUT} = -(20/3)V_{REF}$.
- **Line regulation**
  Change VDD (1-1.4V), get the curve between VDD&Vout;
- **Transient response**
  Catch the waveform of Vout & Vdd. estimate the rise time, settling time, and peak overshoot as a function of VREF. Repeat for different values of the load current, I_load.
- **Loop bandwidth**
  Repeat test 3 in different f_sc. Verify loop stability.
- **Power supply rejection ratio (PSRR):**
  Inject sinusoidal ripple on the power VDD, measure the ripple on Vout
- **Output noise and ripple:**
  Use oscilloscope record Vout in different Vref & I_load, Analyze the output histogram, peak, rms and frequency spectrum.
- **Temperature:**
  Repeat the above tests from 25℃ to 85℃

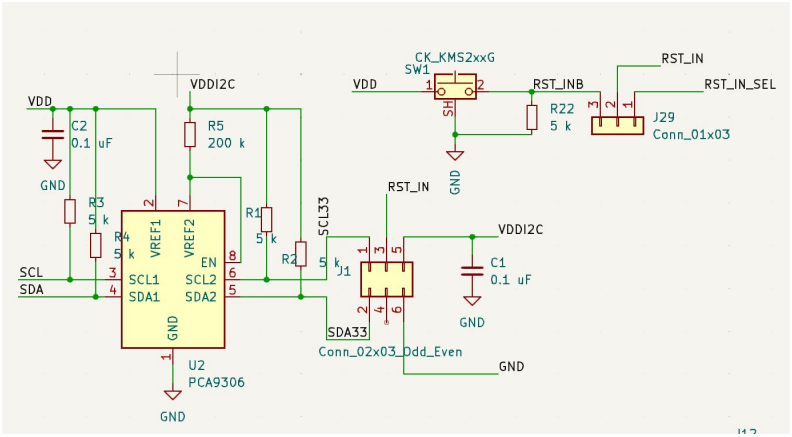


Instrument:

- Power supply for VDD
- Power supply for Vref
- Oscilloscope
- Clock generator for CLK_SC
- Signal generator for power VDD with ripple
- Environmental chamber for temperature test

I2C Controller





I2C register	AncASIC parameter
Register[0] <2:0>	EN <2:0>
Register[1] <7:0>	EN_{CP} <15:8>
Register[2] <7:0>	EN_{CP} <7:0>
Register[3] <7:0>	I_{integ} <15:8>
Register[4] <7:0>	I_{integ} <7:0>
Register[5] <7:0>	I_{vco} <15:8>
Register[6] <7:0>	I_{vco} <7:0>
Register[7] <7:0>	I_{off} <15:8>
Register[8] <7:0>	I_{off} <7:0>

Parameter	Description
Iinteg	bias current for the SC integrator
Ivco	bias current for the VCO
Ioff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (Vc) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

Register map and Description

Test Structures

- **Standard V_T NMOS transistors:**

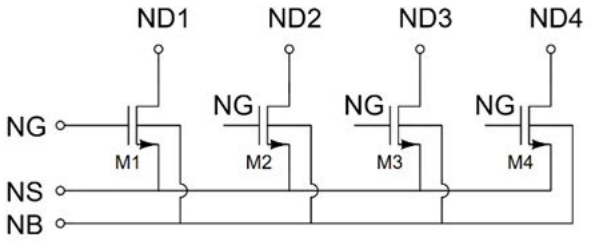


Figure 7: Standard V_T NMOS devices.

- **Standard V_T PMOS transistors:**

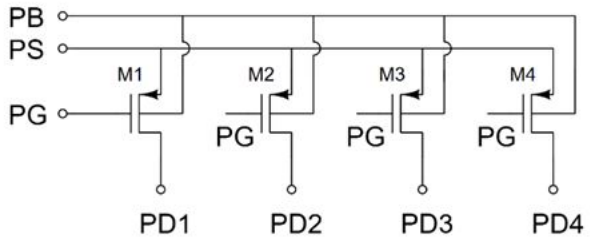


Figure 8: Standard V_T PMOS devices.

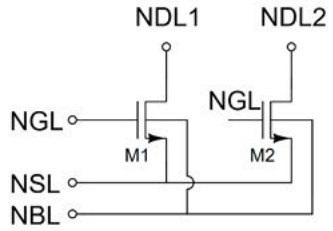


Figure 9: Standard V_T NMOS (large).

- **Standard V_T PMOS transistors:**
  - Large transistors for leakage measurements.
  - Two devices with different Deep Trench Isolatio

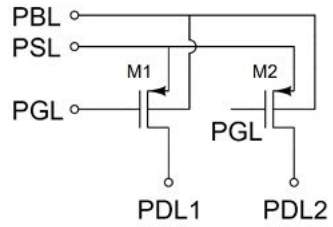


Figure 10: Standard V_T PMOS (large).

- **Additional devices:**

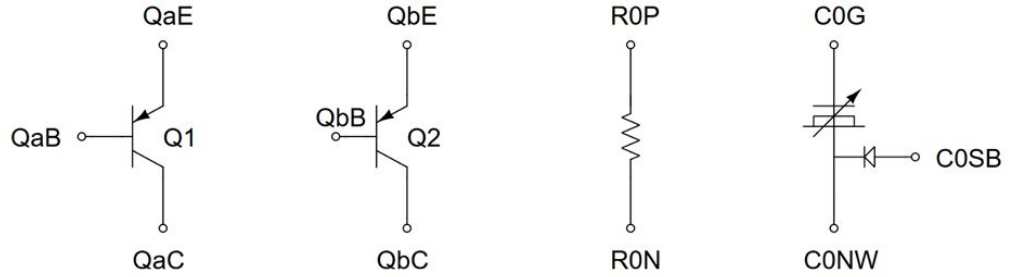


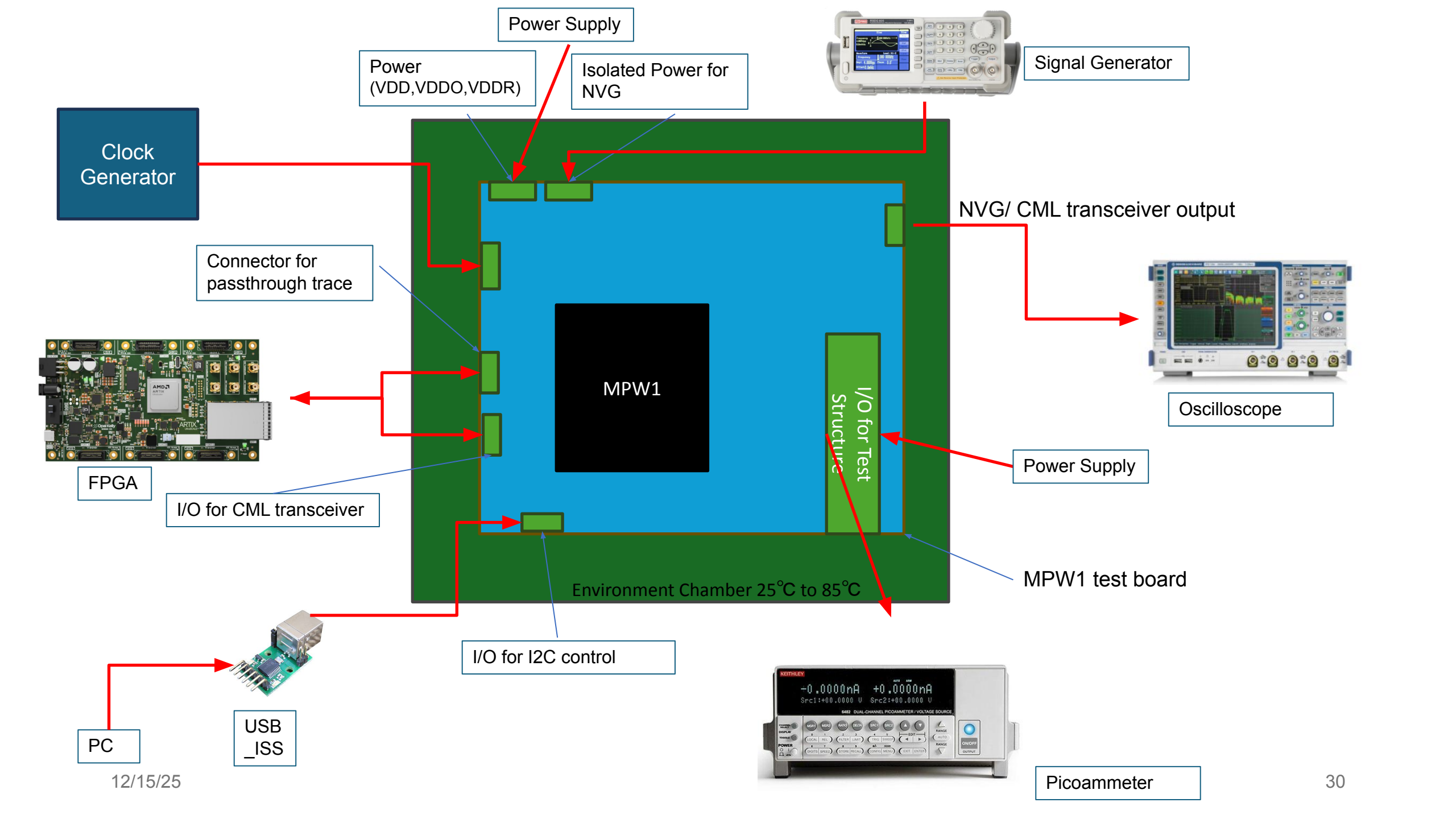
Figure 11: Additional test devices: BJTs, polysilicon resistor, and MOS capacitor.

Test Plan:

- Power consumption
- Threshold Voltage shift
- Leakage current

Instrument:

- Power Supply
- Picoammeter
- Gamma/X-ray/protons


Power Supply
Power
(VDD,VDDO,VDDR)
Isolated Power for
NVG
Signal Generator
Clock
Generator
NVG/ CML transceiver output
Connector for
passthrough trace
MPW1
I/O for Test
Structure
Oscilloscope
FPGA
I/O for CML transceiver
Power Supply
MPW1 test board
Environment Chamber 25°C to 85°C
I/O for I2C control
PC
USB
_ISS
Picoammeter