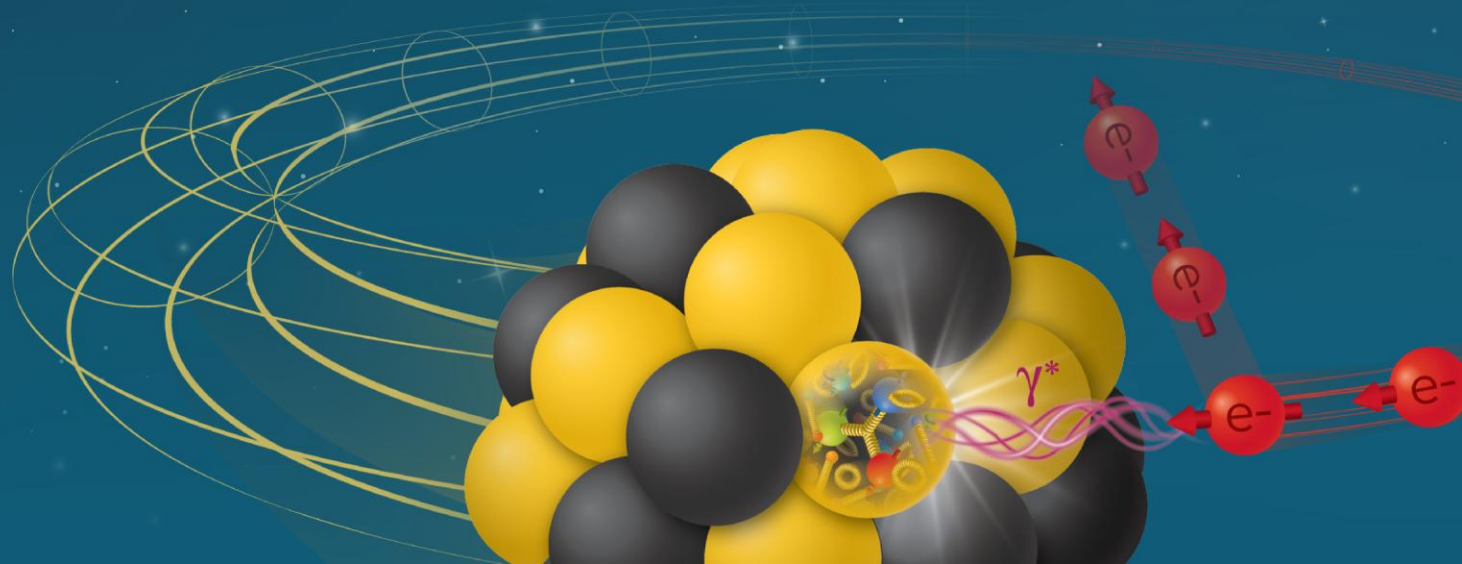
Brookhaven National Laboratory

Jefferson Lab

U.S. DEPARTMENT of ENERGY | Office of Science

Discussion Points

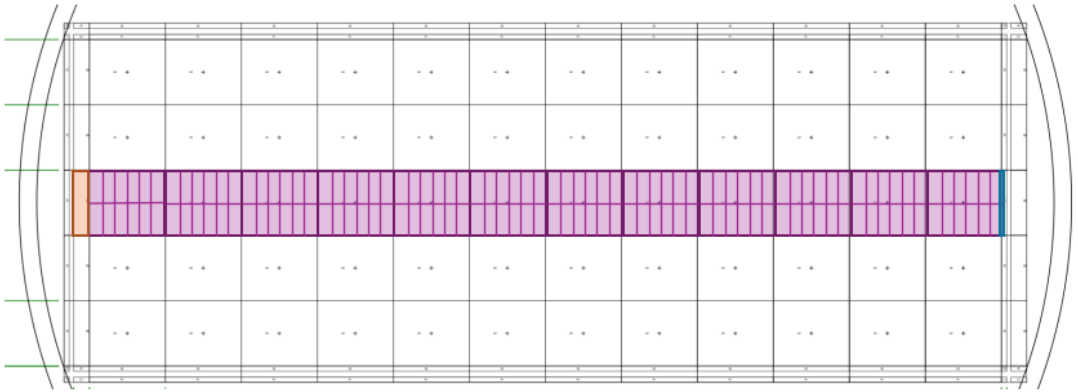


Electron-Ion Collider

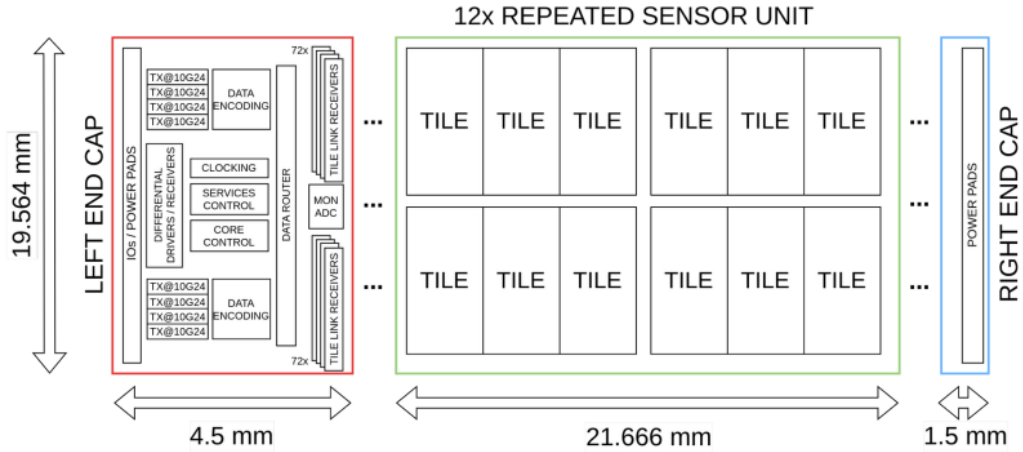
Discussion Points – EIC-LAS

- Status of DOE-CERN Agreement?

MOSAIX



- Simulation
  - Hit Rates – impact on power, data rate, number of links
  - Yield – How many tiles can be turned off?



Discussion Points - AncASIC

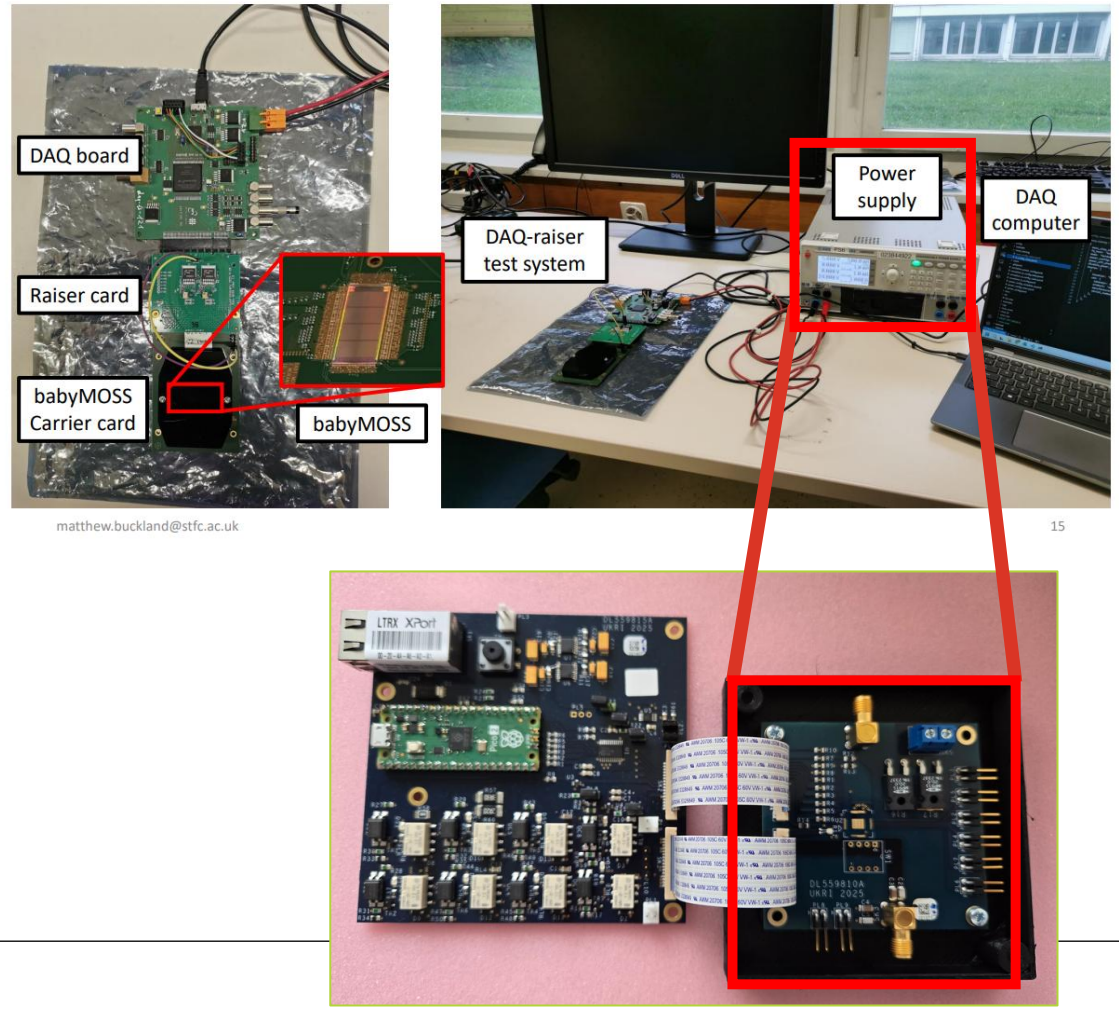
https://indico.bnl.gov/event/24723/contributions/96279/attachments/57524/98763/20240923-babyMOSSTraining_results.pdf

- AncASIC Layout:
  - Further comments welcome!
- Practical integration of the serial powering chain:
  - Need to plan a startup sequence
  - Need to think about impact of non-idealities on operating region and power efficiency
  - Not clear to me who I should talk to about this?
- Further serial powering tests:
  - Validation of MPW2_SLDO
  - SP chains
  - Tests with babyMOSS? babyMOSAIX? Real MOSAIX? Who? Where?
  - Making a basic prototype? Who? Where?

Daresbury Laboratory

ALICE

babyMOSS test system



Discussion Points - AncASIC

Questions to Resolve
- answers expected from System design

Question	Status
Propagation delay per AncBrain hop?	TBD
Max number of AncBrains in chain?	TBD
Total delay to compensate?	TBD

Action Required
- Assessment of propagation delays through system is needed

From and To AncBrain

lpGBT Options

Understanding of protocol modes (ePortTx.pptx)

- E-links output MSB first
- Shadow disabled:

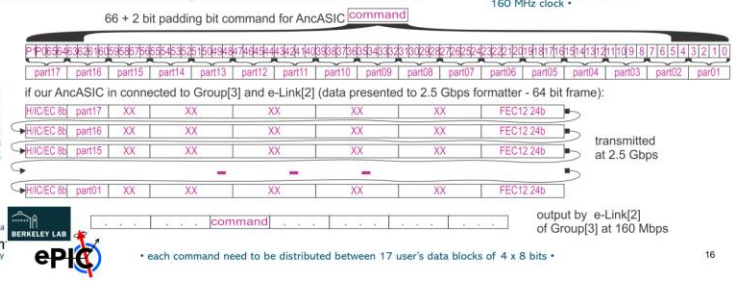
DataRate[1:0]	DataIn[7:0]	DataOut			
		e-Link[3]	E-Link[2]	E-Link[1]	E-Link[0]
2'b10 (x4) 160Mbps	{chn2[3:0],chn0[3:0]}	-	DataIn[7:4]	-	DataIn[3:0]

- Shadow enabled:

2'b10 (x4) 160Mbps	{chn2[3:0],chn0[3:0]}	DataIn[7:4]	DataIn[7:4]	DataIn[3:0]	DataIn[3:0]

- Knowing that AncBrain uses 66-bit long data format, we need to send:

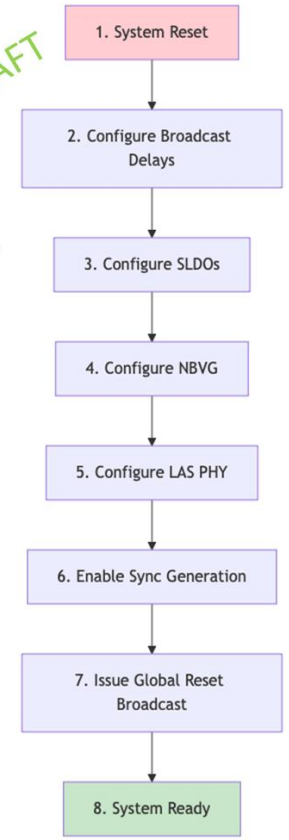
• data out on falling edge of 160 MHz clock •



Start-up procedure

DRAFT

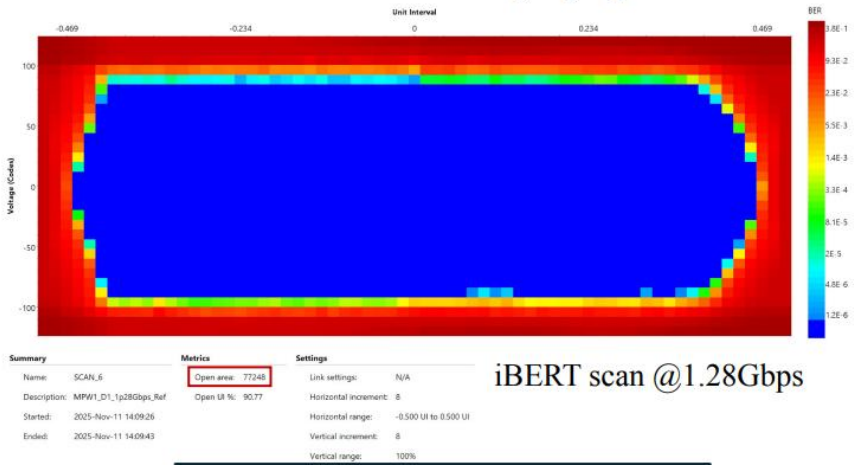
1. **System Reset**
   - Assert rst_n low, wait for stable clock, release rst_n
   - All registers return to defaults
2. **Configure Broadcast Delays (for chain synchronization)**
   - Write ADDR_BCAST_DELAY (0x22) with computed delay value
   - Delay = (chain_position * propagation_delay) / 6.25ns
3. **Configure SLDO**
   - Write SLDO_MODE0..4 (0x0F, 0x1A-1D) = 0x02 (Normal mode)
   - Write SLDO_CTRL0..4 (0x10-14) with DAC values
4. **Configure NBVG**
   - Write NBVG_REG0 (0x40) enable bits
   - Write NBVG current/voltage registers (0x41-4D)
5. **Configure LAS PHY Timing (if non-default needed)**
   - Write PHY timing registers (0x50-54)
   - Write PHASE_ALIGN (0x2A) if needed
6. **Enable Sync Pulse Generator**
   - Write SYNC_PERIOD (0x25)
   - Write SYNC_WIDTH (0x26)
   - Write SYNC_CTRL (0x27) bit[0] = 1
7. **Issue Global Reset Broadcast**
   - Send command with ADDR=0x0000
8. **System Ready for Normal Operation**



Discussion Points - AncASIC

Agree minimum BER for data rate tests

- Differential transmission line for testing high-speed data transmissio



iBERT scan @1.28Gbps

Effect of Hit Rate Updates

Latest Updates and Considerations

➢Updated hit-rate estimates (~10x) and their impact on:

- Assessment of strategies to reduce the tile clock frequency below 160 MHz
- Evaluation of the feasibility of operating with a single output driver