Software: Testing, Commissioning, and Operation

Oxford SVT working meeting

16 Dec. 2025

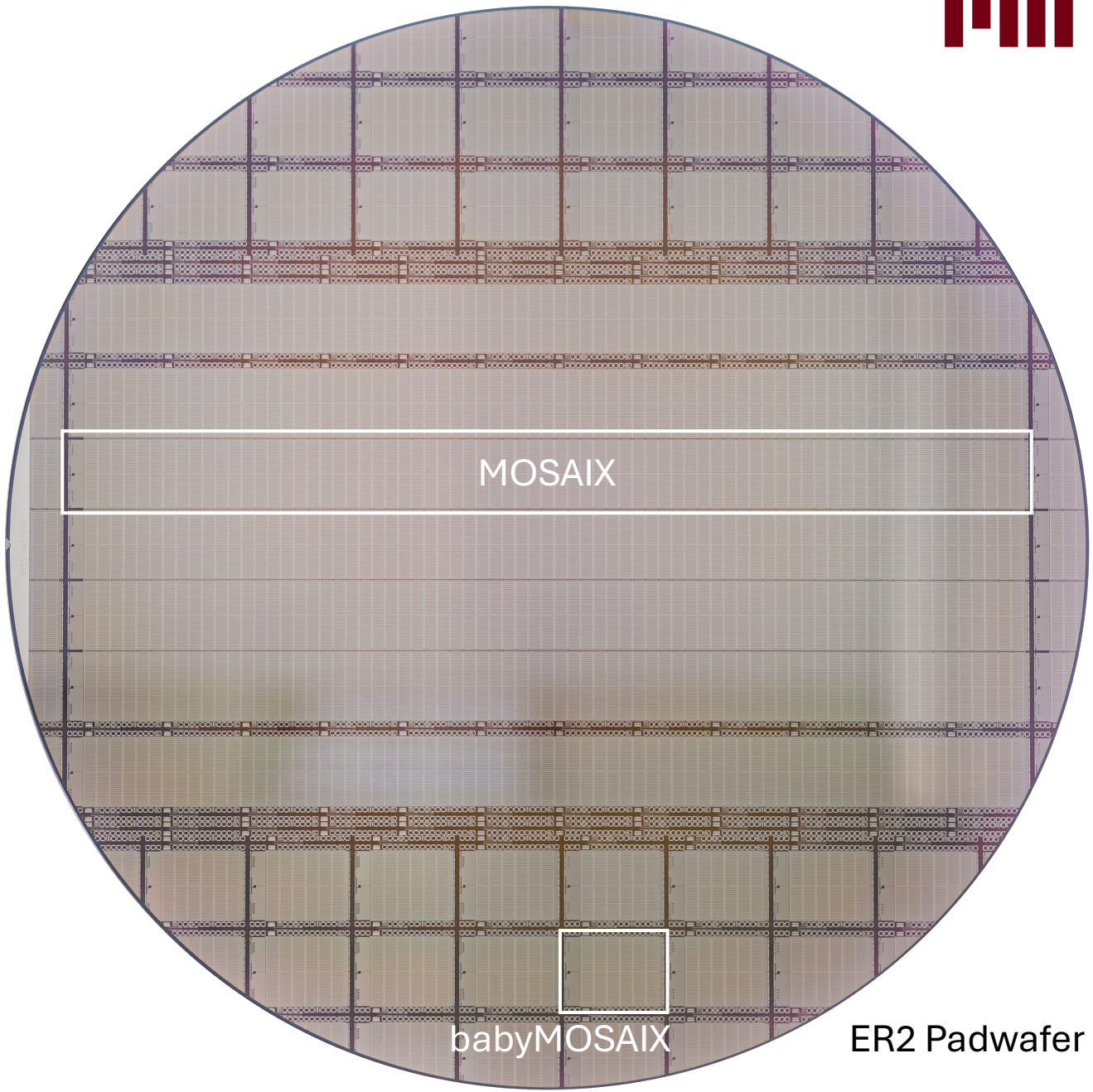
Gregor Eberwein (MIT) on behalf of SVT WP2

Outline

- MOSAIX recap
- Testing infrastructure, qualification and status
- SVT SW framework

MOSAIX chip status

- MOSAIX wafers (ER2) arriving in February
  - Pad wafers: arrived December
- ER3 submission preparation in progress -> feedback to designers by mid 2026



ER2 Padwafer

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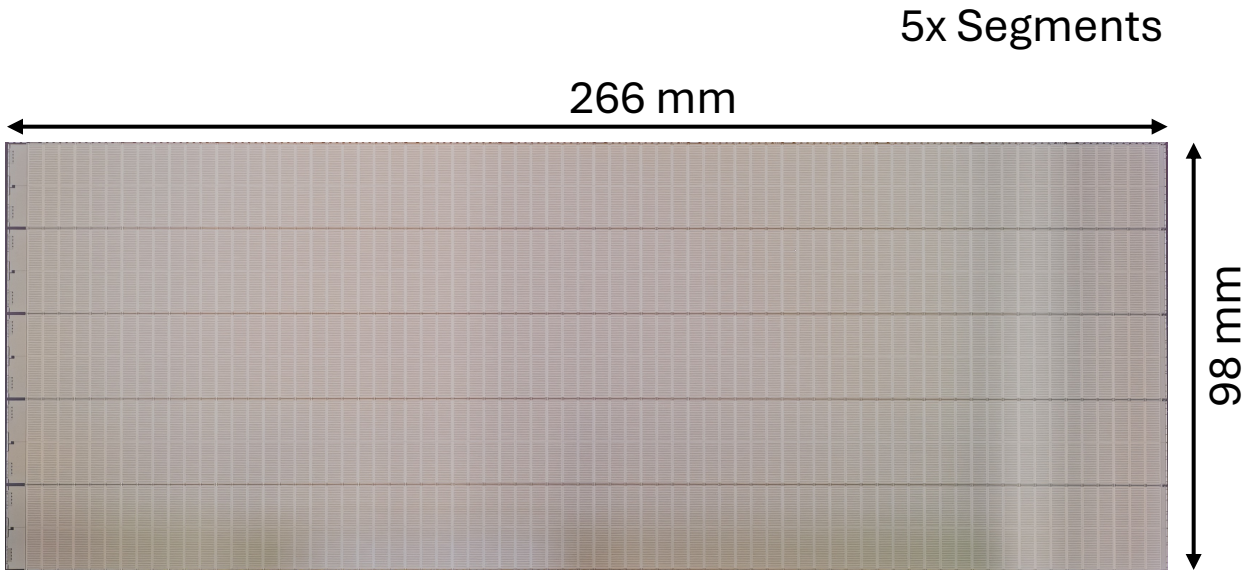

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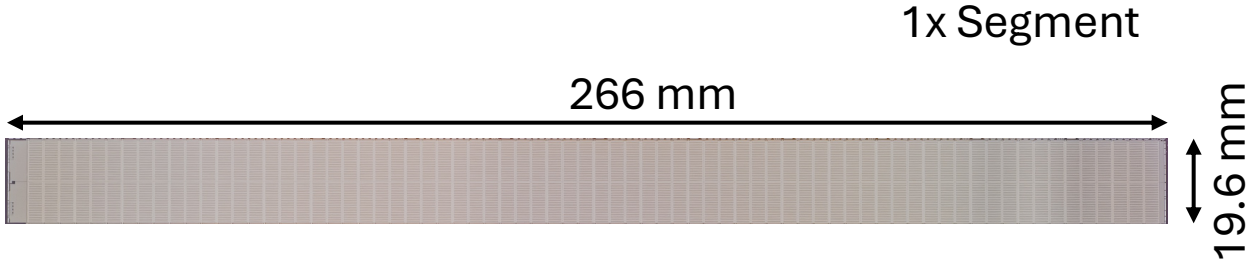
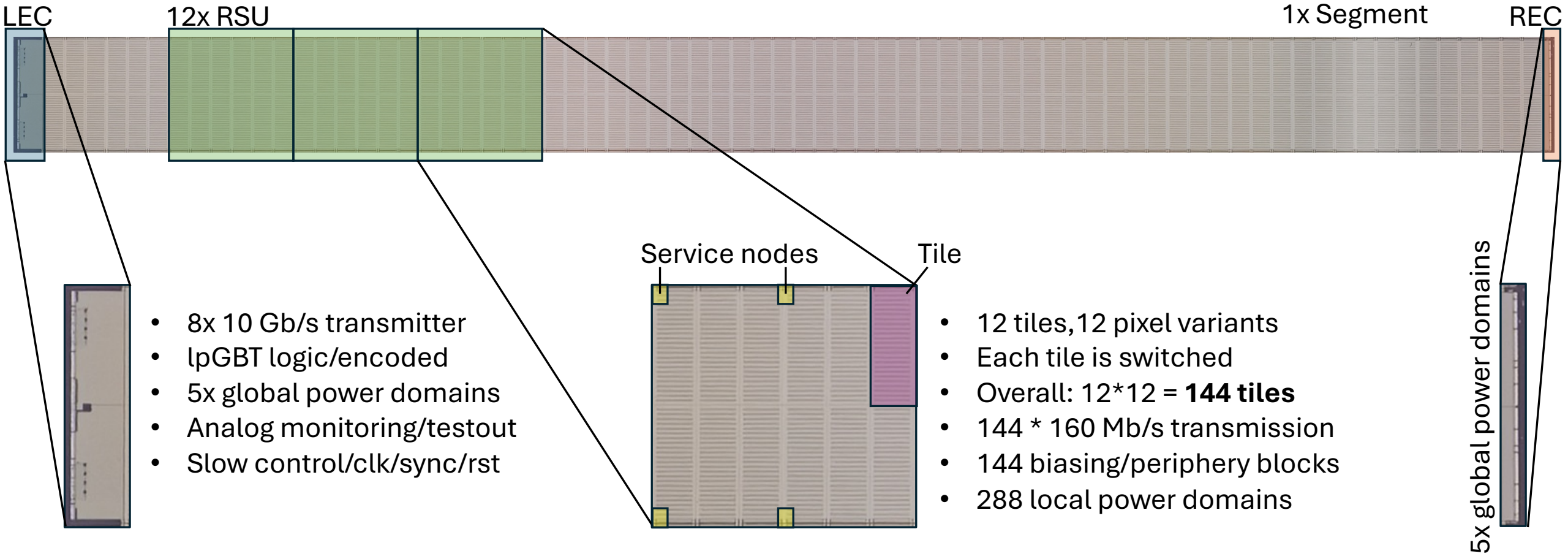


..one monolithic sensor

MOSAIX anatomy



- 8x 10 Gb/s transmitter
- lpGBT logic/encoded
- 5x global power domains
- Analog monitoring/testout
- Slow control/clk/sync/rst

- 12 tiles,12 pixel variants
- Each tile is switched
- Overall: 12*12 = **144 tiles**
- 144 * 160 Mb/s transmission
- 144 biasing/periphery blocks
- 288 local power domains

One tile ~ one pixel sensor

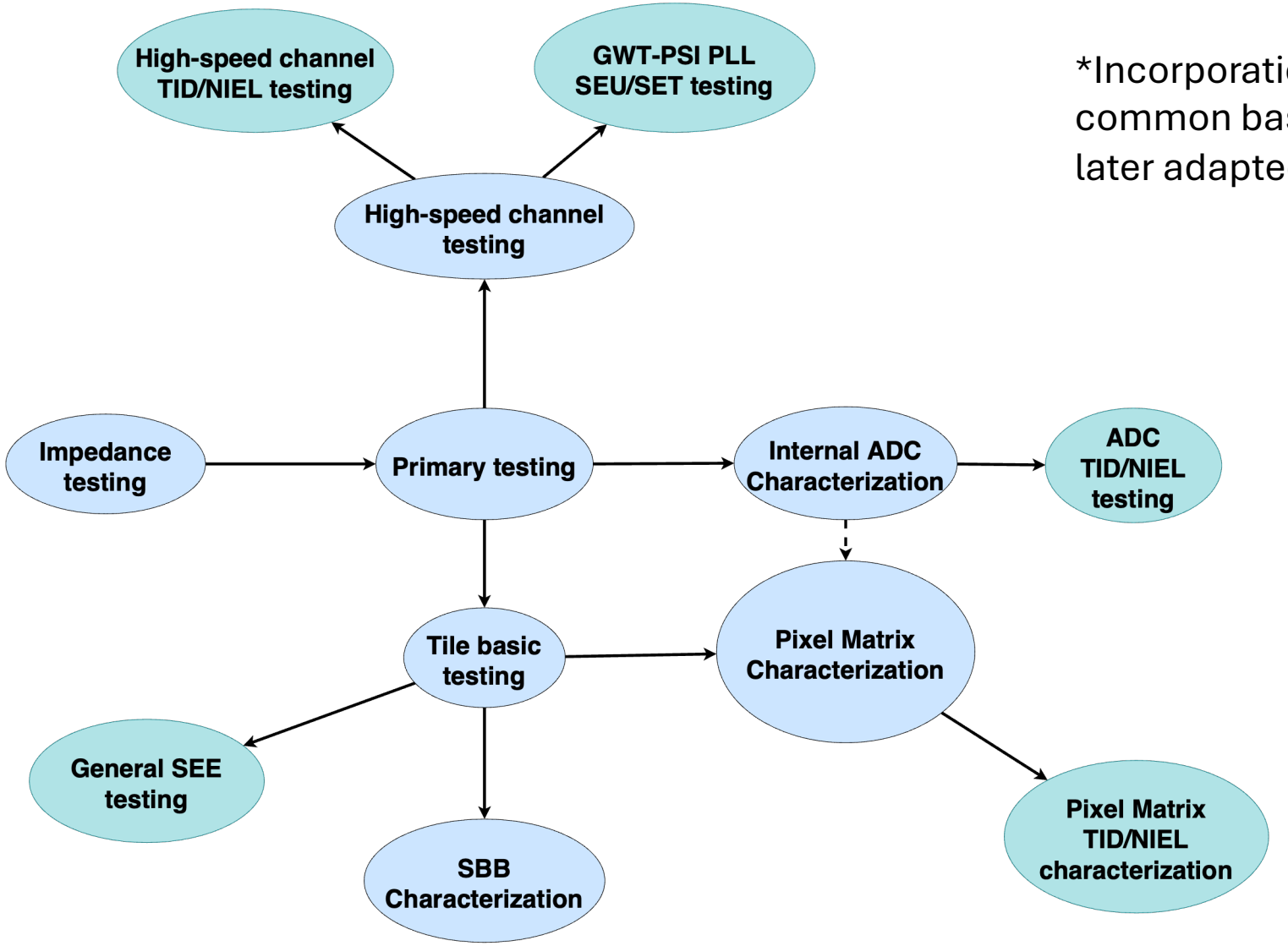
MOSAIX qualification goals

- Verify functionality of all features
- Yield of blocks
- Identify the pixel variant
- 10 Gb/s transmission on-wafer
- Radiation effects
- *ambition for day one readiness*

Test stage	Dependencies	Description
Primary testing	Impedance testing	Testing of services and global supplies, slow control access and critical features, e.g., service node control. Pre-requisite for all further testing.
Impedance testing	Primary testing	TBD
Tile basic testing	Primary testing	Testing tile-level functionality. SBB data transfer.
Analog circuitry and ADC testing	Primary testing	Characterization of on-chip ADC and analog monitoring network. Includes also testing of bandgap reference.
Pixel matrix characterization	Tile basic testing /ADC testing?	Characterization of pixel matrix.
High-speed channel	Primary testing	Testing high-speed channel
SBB characterization	Tile basic testing	Full characterization of the SBB. Check margins for data transfer.
General SEE testing	Tile basic testing	SEU cross-section, SEL susceptibility
Pixel matrix TID/NIEL characterization	Pixel matrix characterization	Pixel matrix perfomance after radiation
High-speed channel TID/NIEL testing	High-speed channel	LEC/serializer performance after radiation
ADC TID/NIEL testing	ADC testing	ADC performance after radiation
GWT-PSI PLL SEU/SET testing	High-speed channel	Check PLL susceptibility for SEU/SET

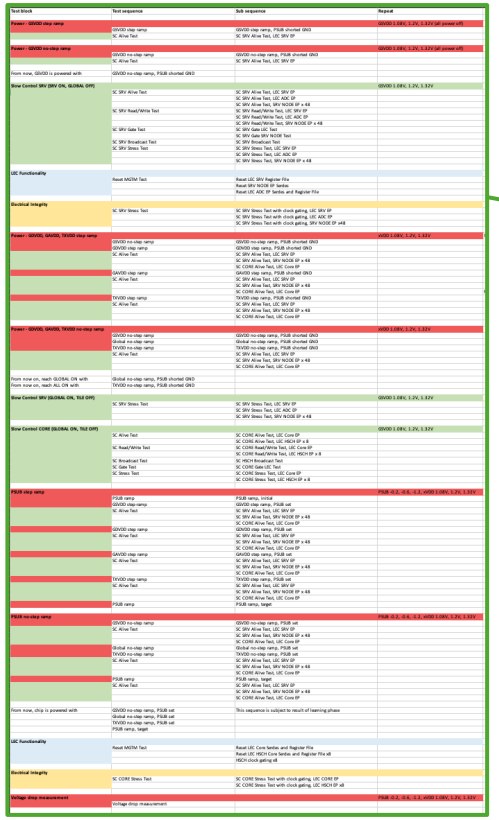
*ITS3 stage plan

Qualification and characterisation stages

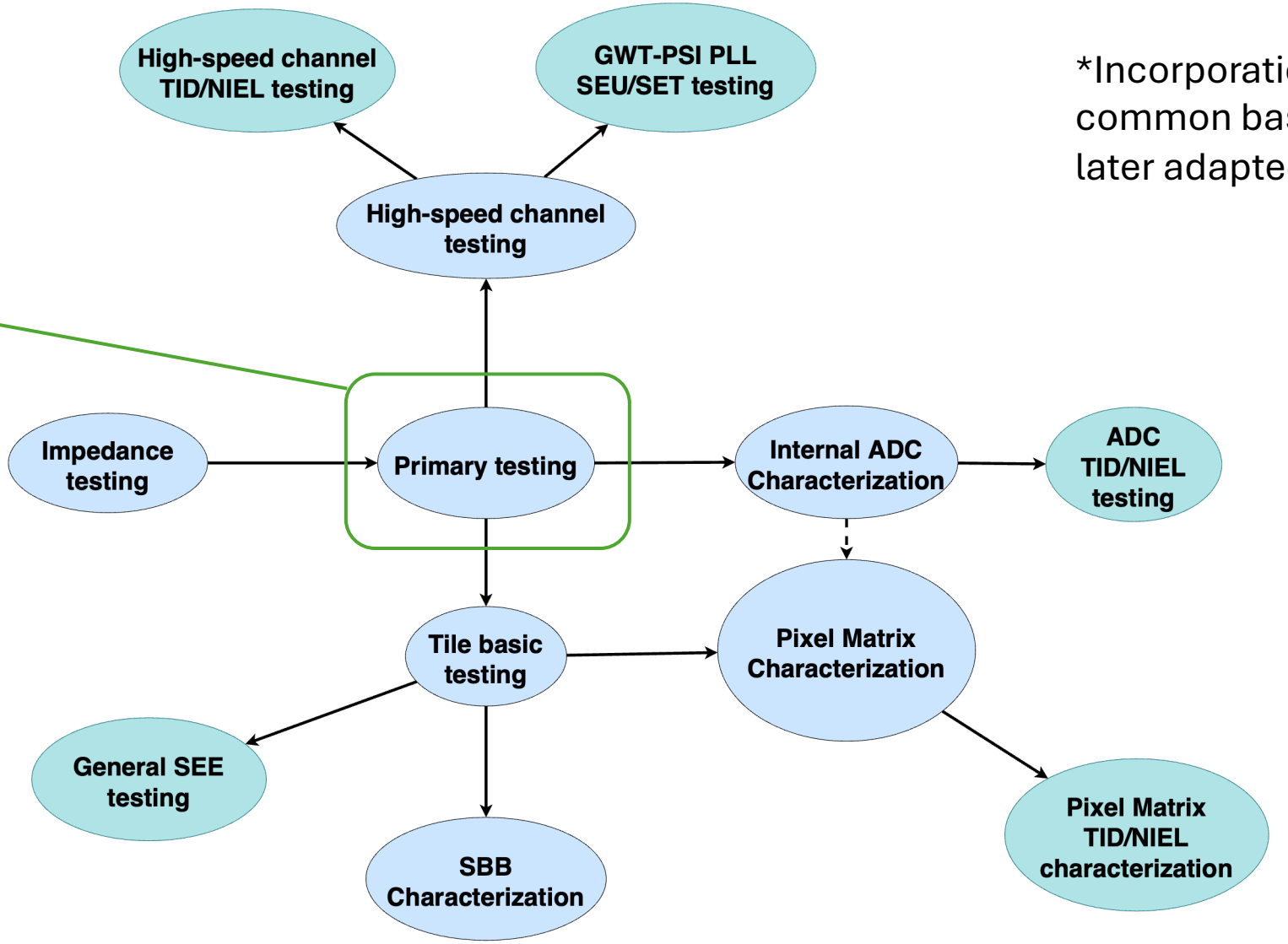


*Incorporation of ITS3 plan as common baseline in ER2, later adapted for SVT

Qualification and characterisation stages



Tests *before* powering on the individual tiles



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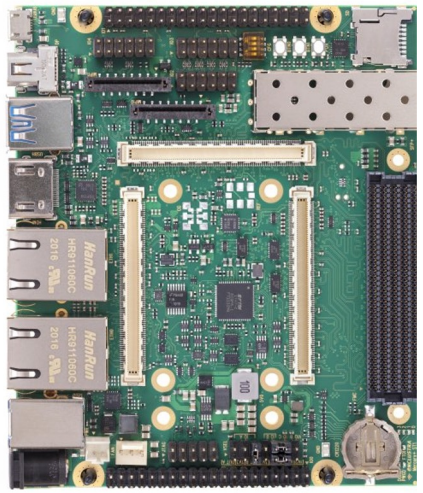
Testing Infrastructure

2x power supply

SMU & multiplexer for impedance

Altera Arria 10 & Enclustra baseboard



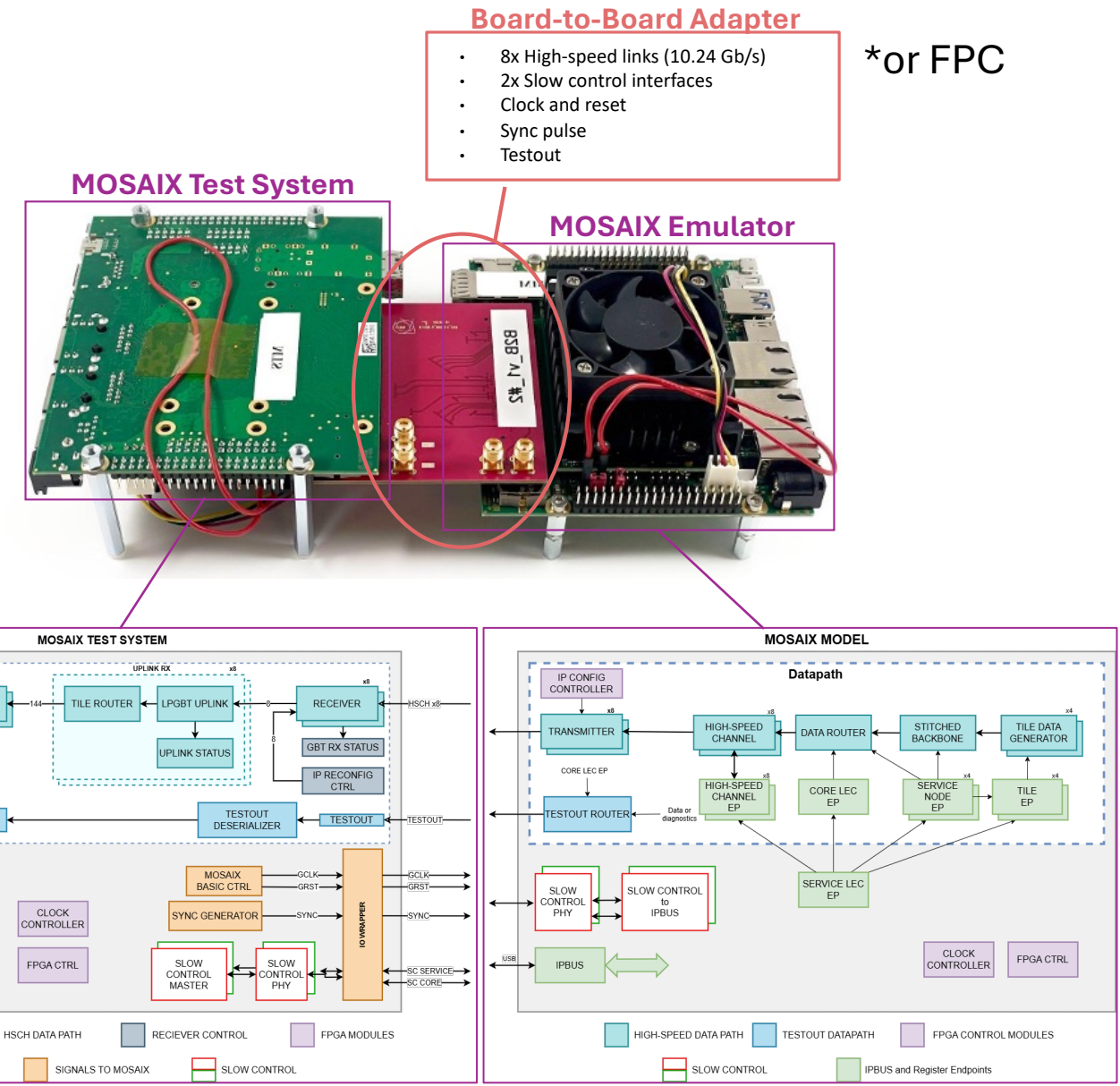
1 set/MOSAIX (Segment)
Connected via USB3 <> PC

MOSAIX targets:

- **Wafer Probing** *see Stefano's presentation*
- Carrier PCB
- Bent models/test beams

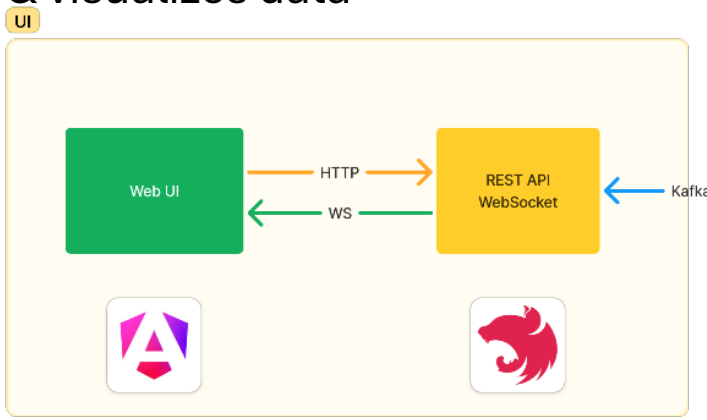
Tests and readiness

- Firmware -> done (ITS3)
  - Includes emulator allows to test framework
- Hardware agnostic API -> ongoing (ownership of small part)
- List of tests & status thereof
  - Readiness report this week
  - It will be possible to run set of tests when chips are available



SVT SW framework

Web based UI
Produces commands
& visualizes data



Kafka Msg

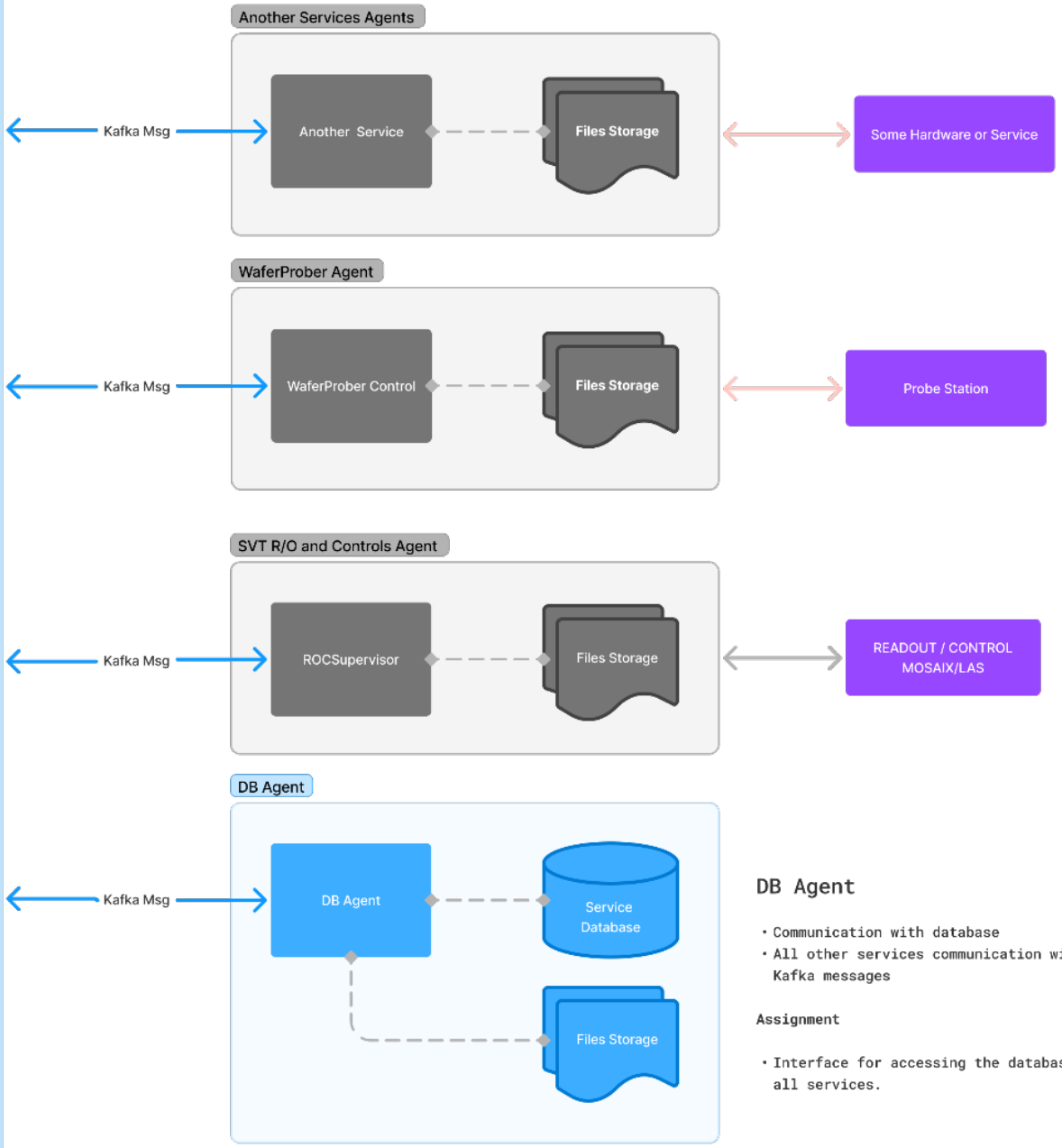
SVTSupervisor

Kafka Msg

Distributed Kafka backbone

Kafka

Distributed Agents



UI

- Web based service, consist of 2 parts:
  - Front-end
    - running in the browser
  - Back-end
    - ensure communication between other services, provides HTTP, WS, Kafka interfaces for communication
- Assignment
  - UI for start/stop operations
  - UI for data overview/analysis

DB Agent

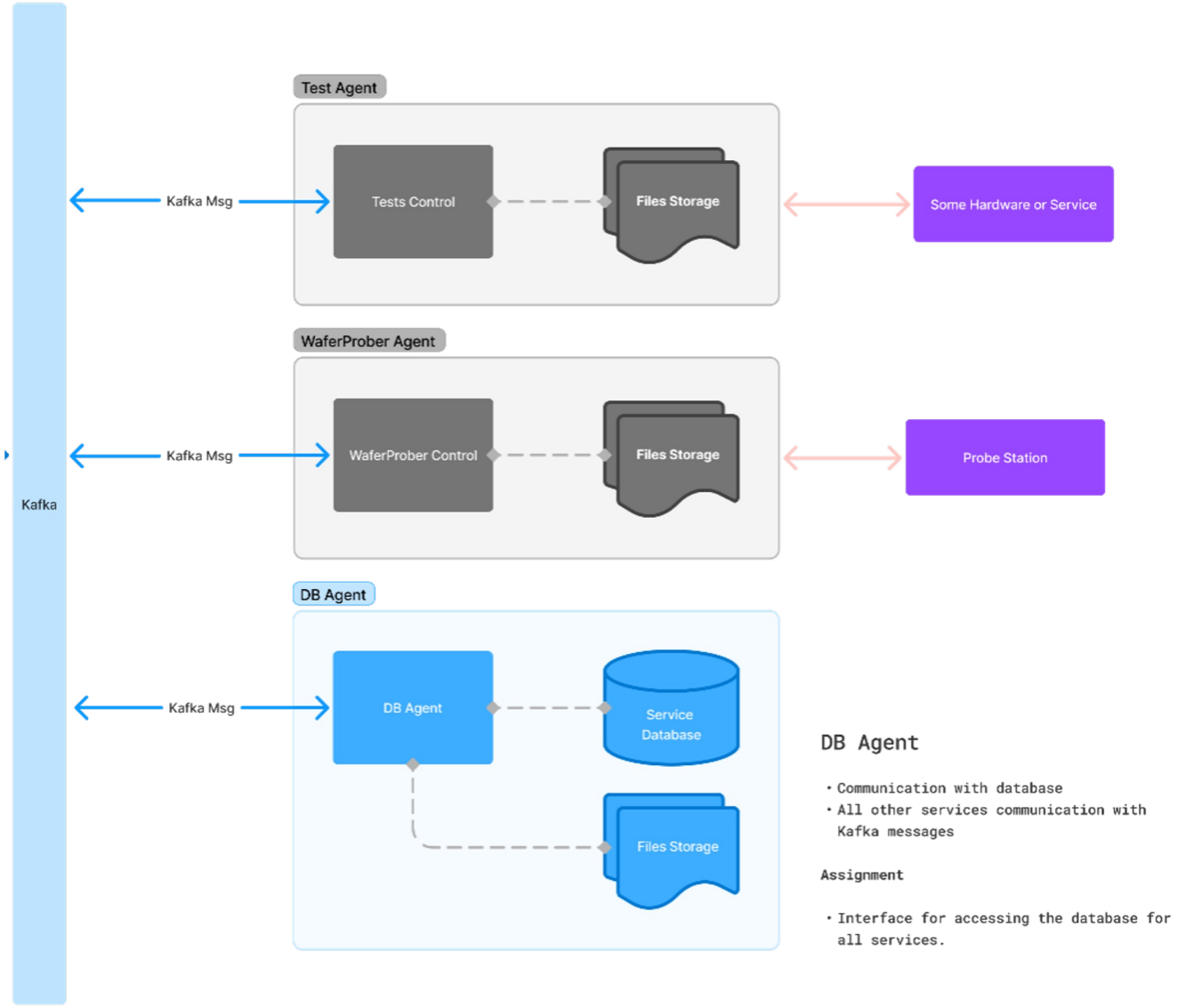
- Communication with database
- All other services communication with Kafka messages

Assignment

- Interface for accessing the database for all services.

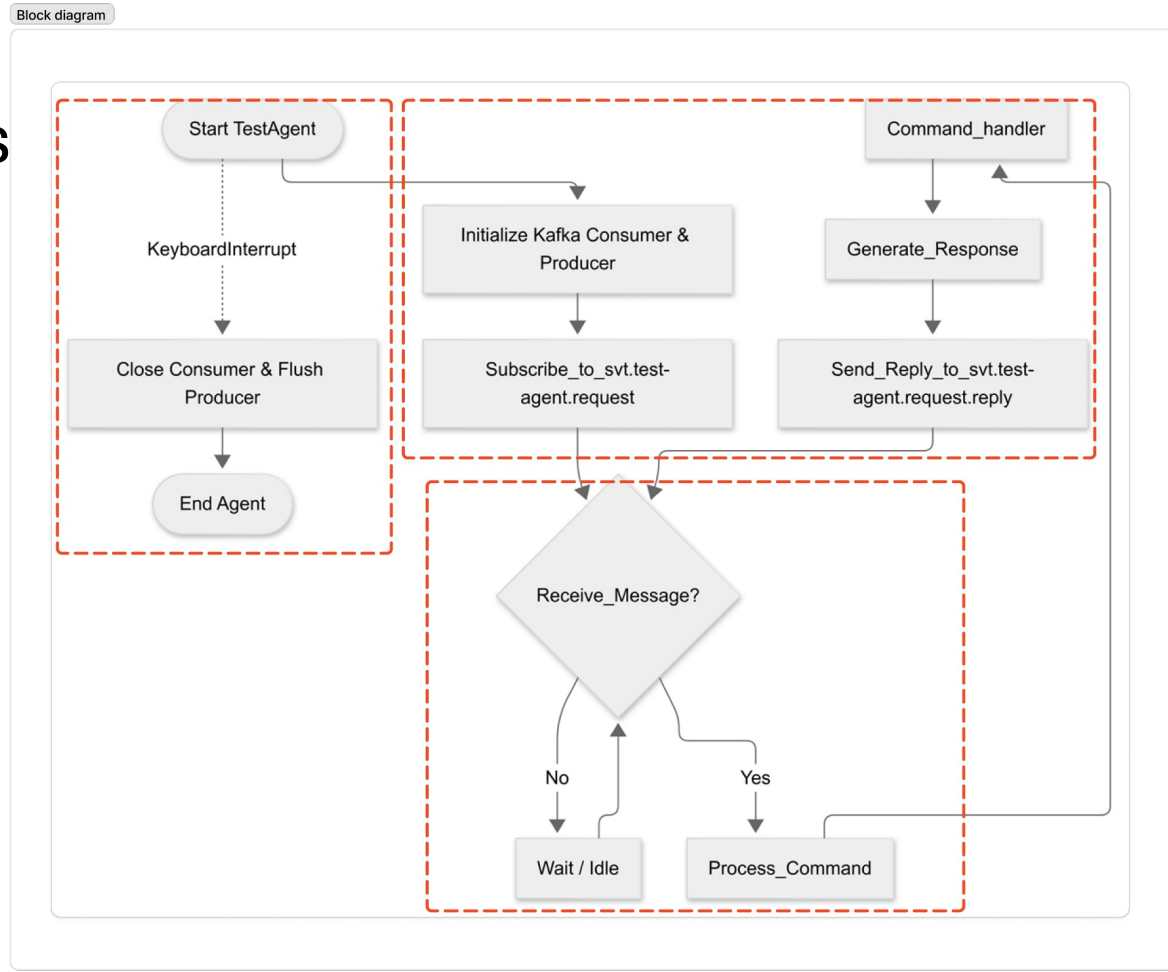
Agents under development

- Test Agent
  - Runs the chip tests
- Wafer Probe Agent
  - Controller to operate the wafer prober
- Database Agent
  - Communication with DB (CERN DB on demand service)



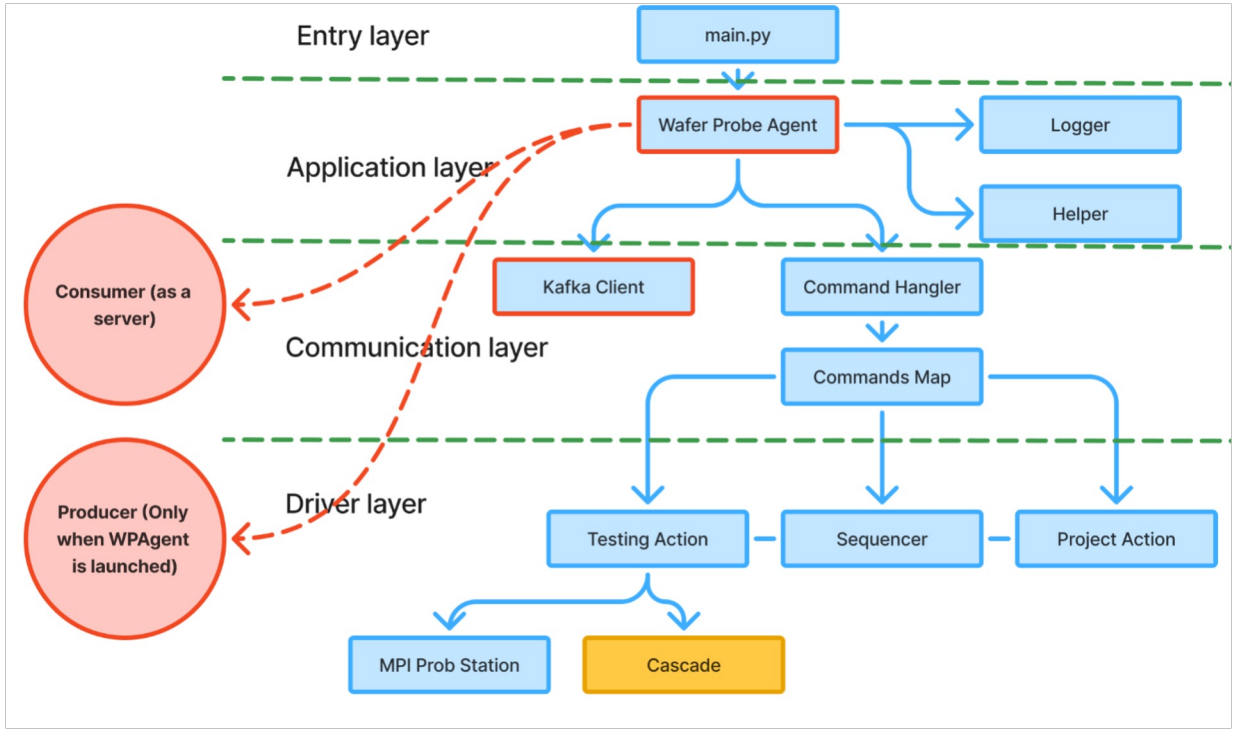
Test Agent

- Individual agents for separate SVT ASICs
- For MOSAIX:
  - Full integration of ITS3 ER2 qualification and characterisation tests in SVT SW framework
  - Derive qualification strategy for ER3
  - Use emulator setup (running) to create dummy tests
- Status: ongoing
  - New: test sequencer, direct DB Agent access, direct feedback to UI



Wafer Probe Agent

- Central controller to operate wafer probe stations autonomously
- Interface with the remaining testing framework
  - I.e. move to chip, perform test (sequence)
- Status: ongoing
  - New: set of interace commands for MPI wafer prober, retrieving DB info, command sequences(json), wafer maps -> *see Stefano's presentation*

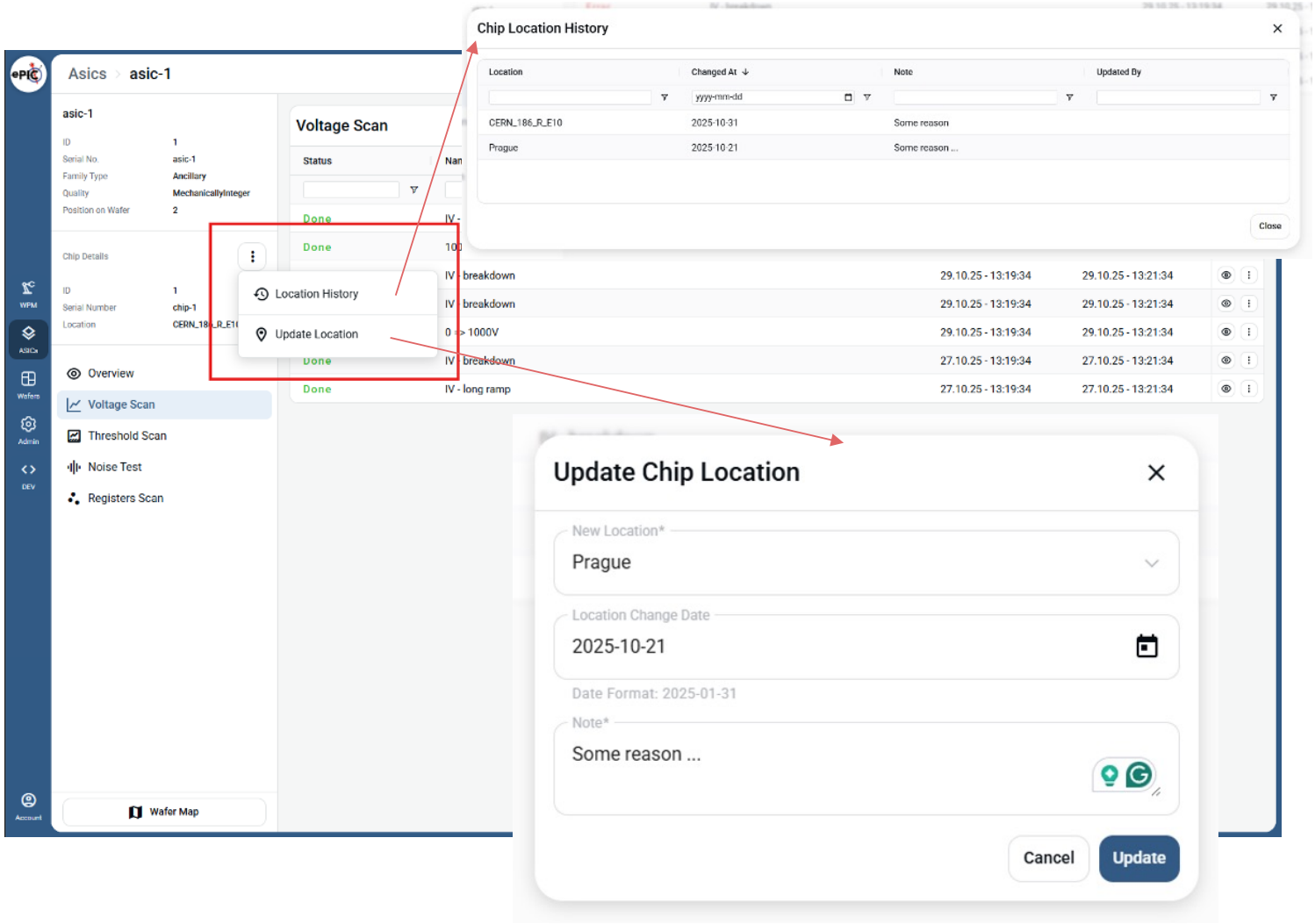


DB Agent

- DB Agent is the main communication layer with the Database
  - Kafka consumer/producer for pull and push request/reply messages
- DB structure: work in progress
  - New: history tracking
- Database on temporary dev instance

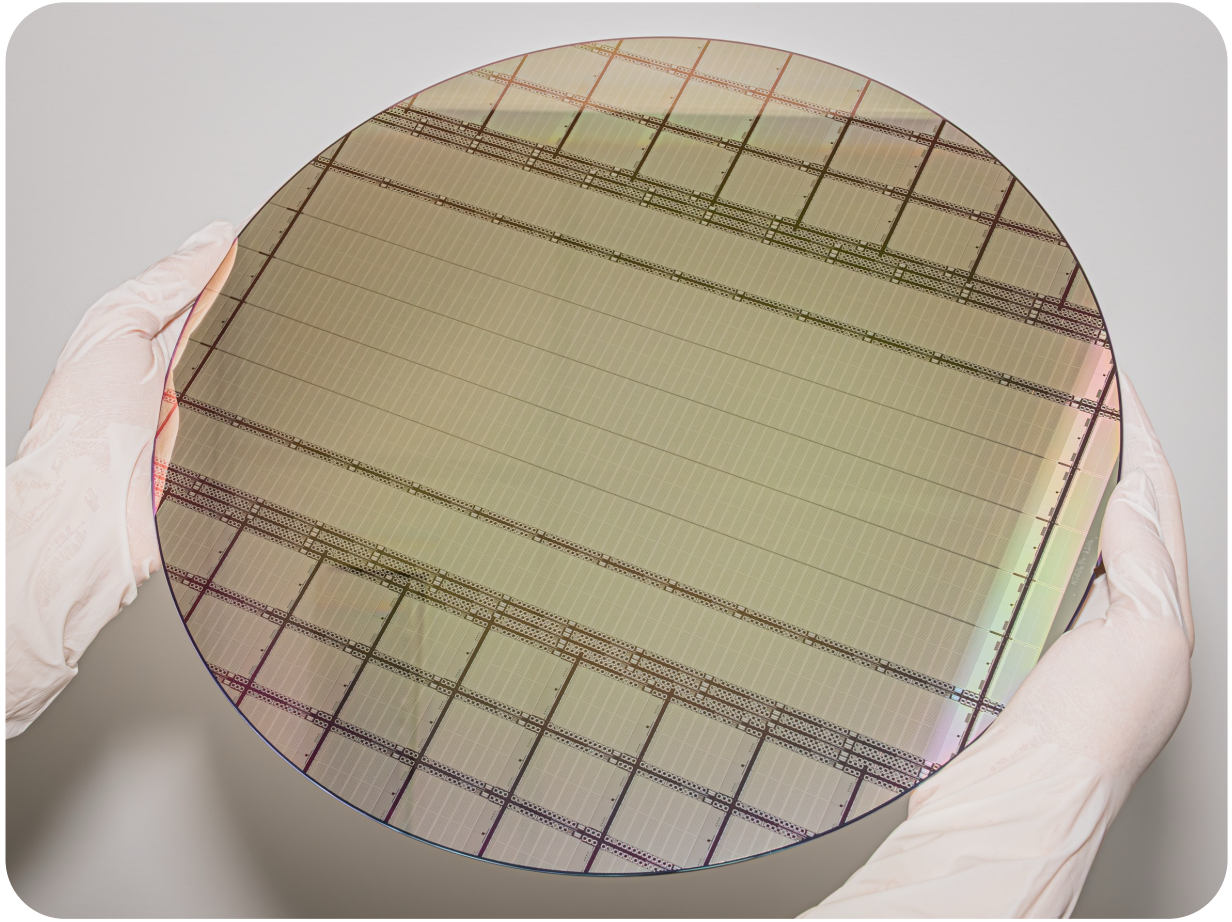
User interface (UI)

- Global interface between operator, DB, and all Agents
- Status: ongoing
  - New: chip tracking, creation of new ASICs individually or in bulk



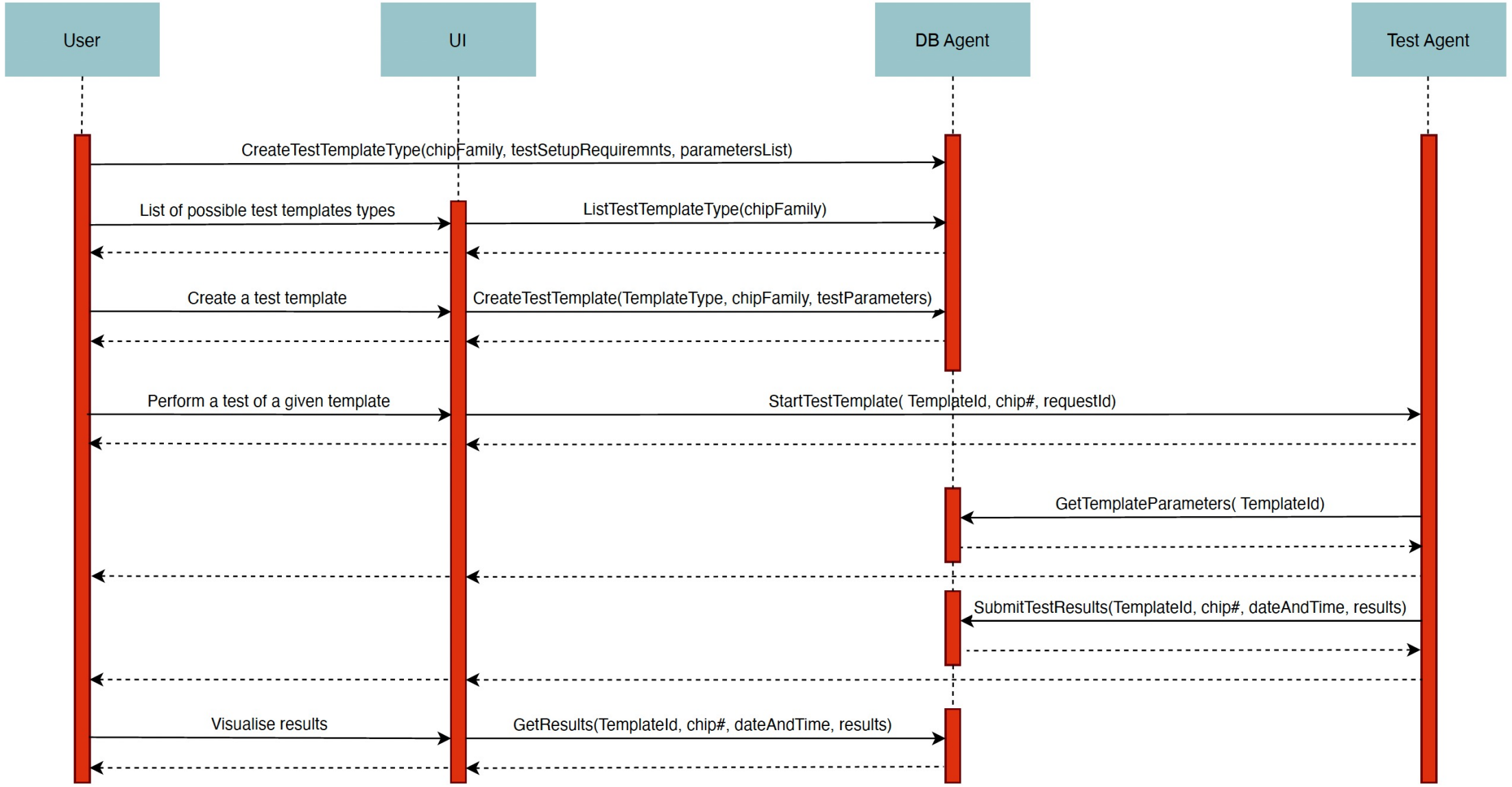
Conclusions

- MOSAIX wafers arrive early 2026
- Foundational infrastructure ready and tested, using emulator for pre-testing
- MOSAIX test sequence development in progress
- SVT SW framework is steadily growing, Agents need still work. Next: use emulator to run realistic test cases
  - Input and contributions very welcome
  - Agnostic and flexible in regard to adding Agents and functionality for testing sites and production
  - Goal of plug-and-play with tested hardware

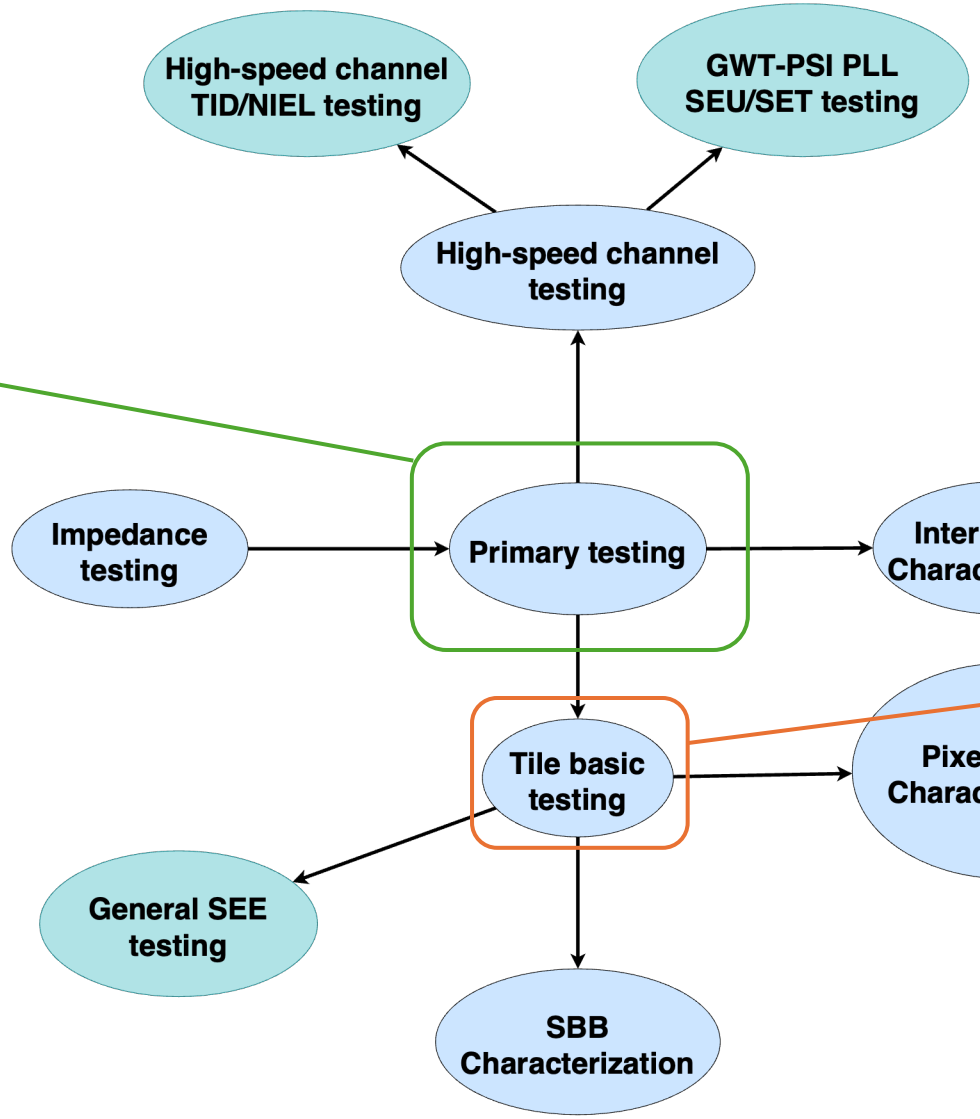


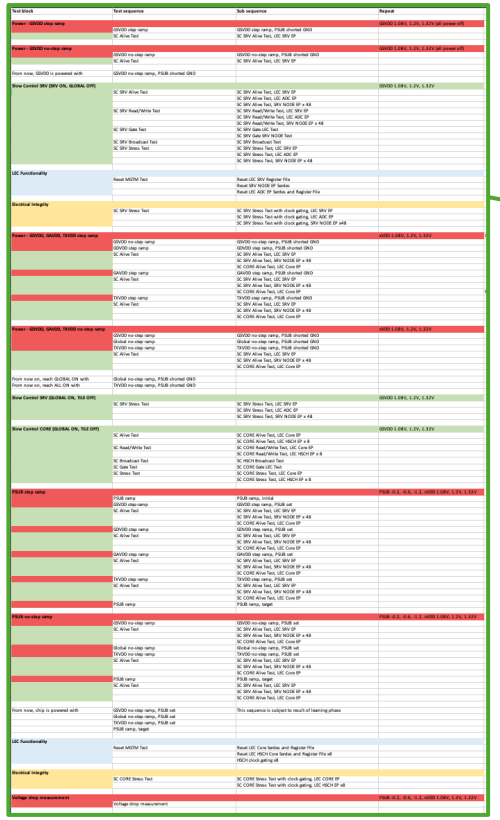
BACKUP

Example communication



Qualification and characterisation stages





Tests *before* powering on the individual tiles

*Incorporation of ITS3
-> Tests assumed in WP2, baseline later adapted for SVT

Baseline common plan for ER2, then

Qualification of MOSAIX

The Challenge(s)

144x independent pixel sensors

Distributed configuration

144x power switches,
288x local power domains

Timing synchronization

On-chip data distribution

Independent control and monitoring

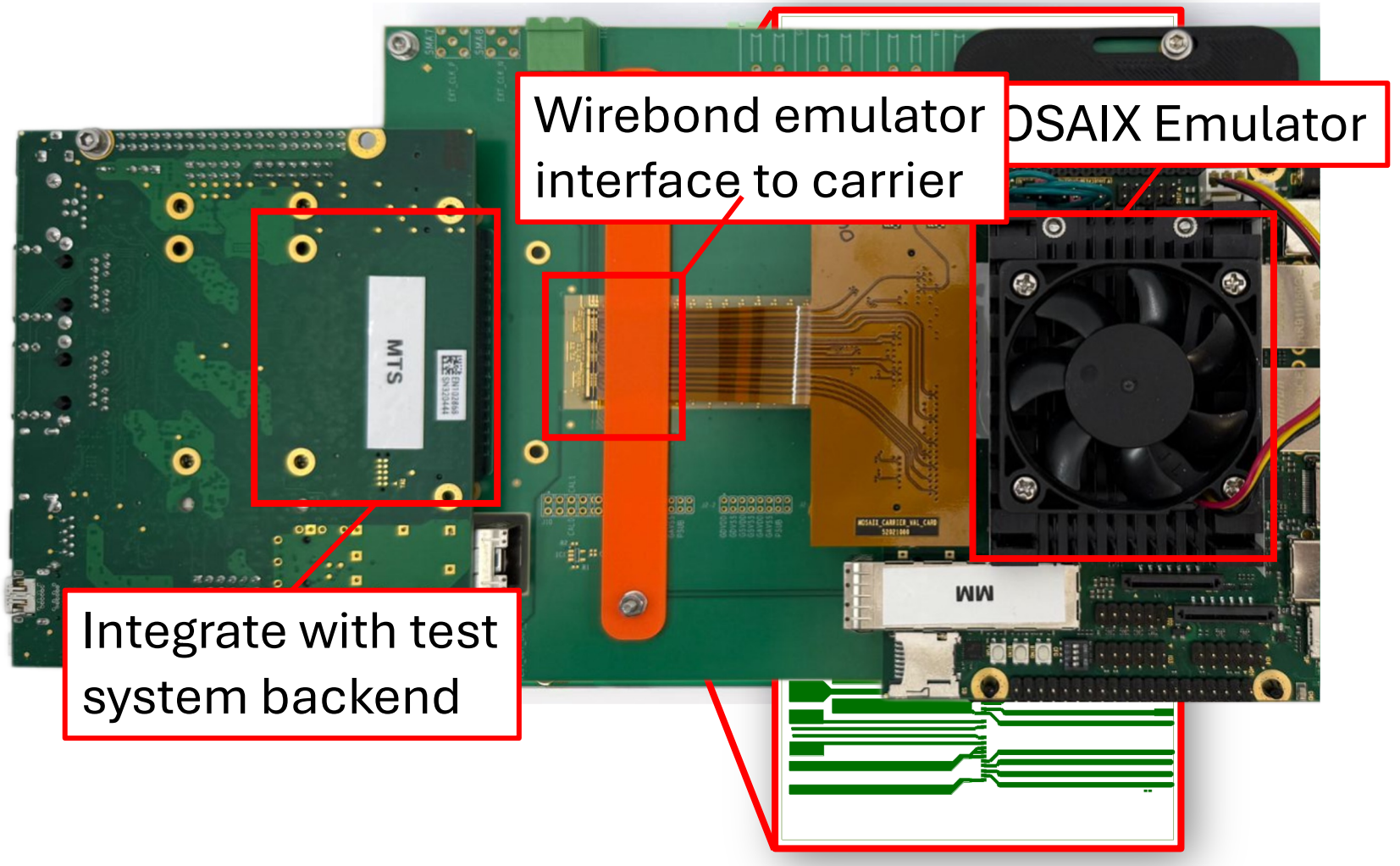
8x High-speed links

On-chip power distribution

ALL AT ONCE

Qualification Infrastructure

Pre-Silicon Verification



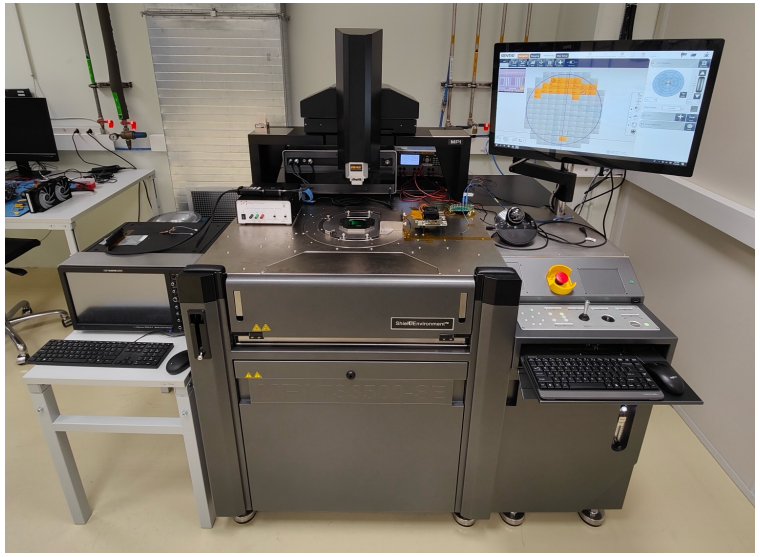
Wafer probing @ CERN DSF

Status

- Two probe setups
- Both probers are fitted for:
  - impedance measurements
  - power ramping
  - functional testing
- All equipment acquired and at CERN
- Contact and automation testing with pad wafers: ONGOING

CERN prober – Standard cantilever needle probing

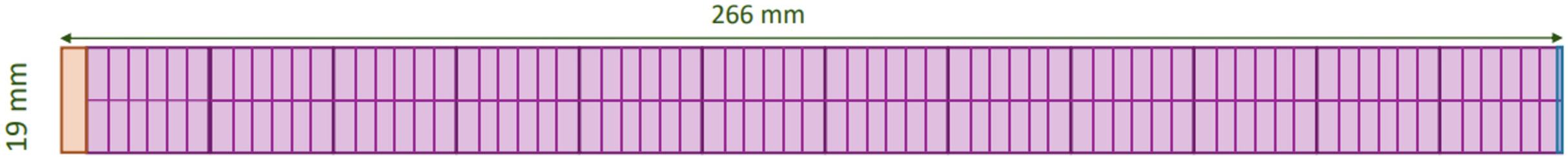
- Probe card: 1x DELIVERED, 2x ARRIVING SOON
- Functional tests with emulator: ONGOING



MIT prober – High-speed vertical needle probing (R&D)

- Studies on high-speed probing: DONE
- Probe card: ORDERED, expected delivery EOY (single-segment) and January 2026 (multi-segment)

MOSAIX Core Specs



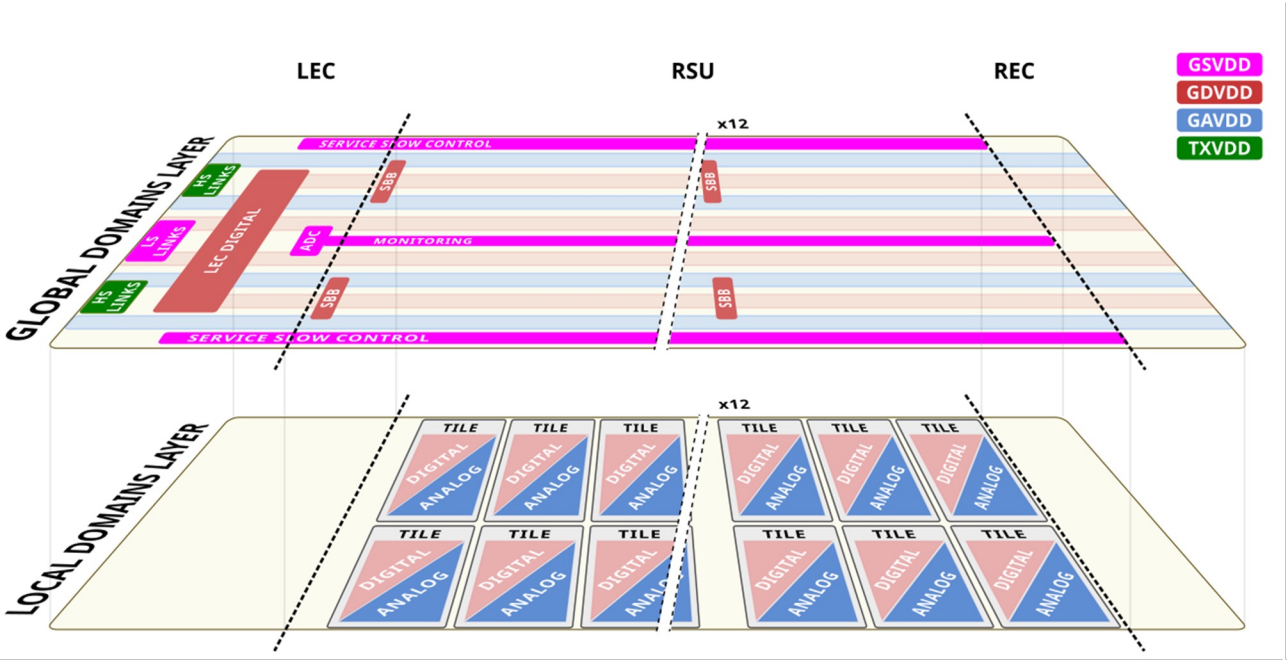
- 93% sensitive area
- 0.7% modularity
- 144 tiles
- 4.4 MHz/cm^2 particle rate

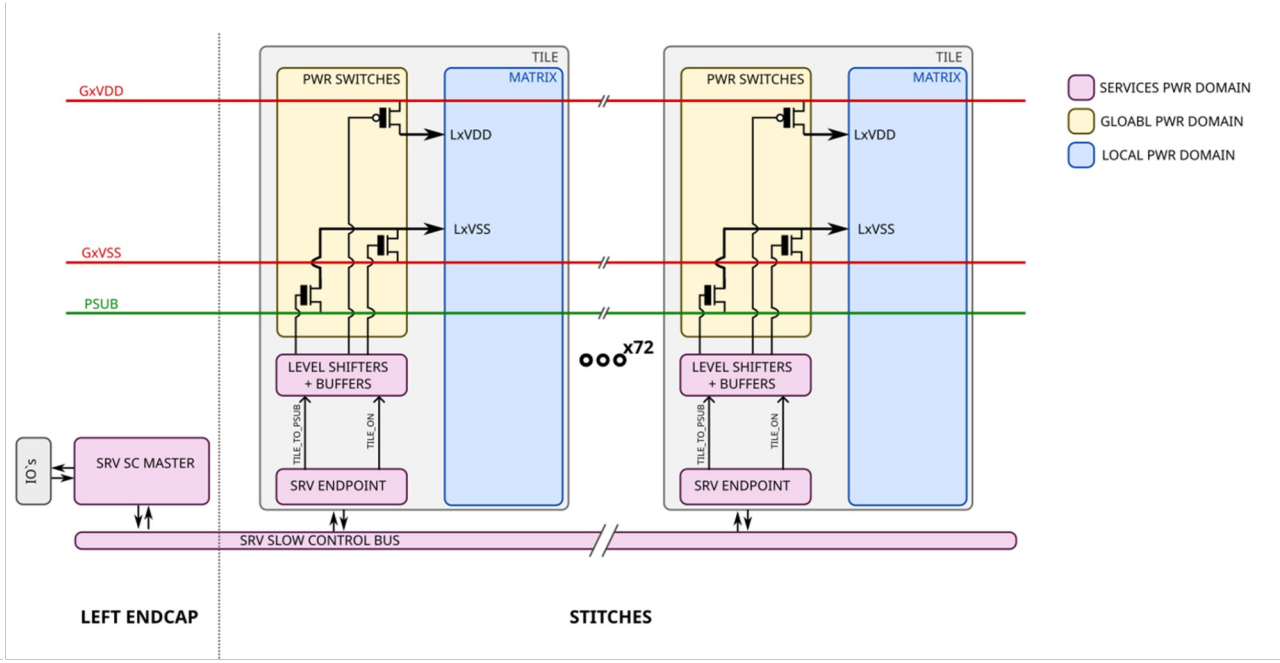
- 30.72 Gb/s off-chip data transmission
- minimum 2 µs integration time
- < 40 mW/cm^2

- 1013 NIEL (1 MeV neq cm^{-2})
- 10 kGray TID
- Triple modular redundancy

- 20.8 x 22.8 µm^2 pixel size
- 444 x 156 pixels per tile
- Detection efficiency > 99%
- Fake-hit rate: < 0.1 pixel^{-1}s^{-1}

MOSAIX


LEC
RSU
REC
GSVDD
GDVDD
GAVDD
TXVDD
GLOBAL DOMAINS LAYER
SERVICE SLOW CONTROL
HS LINKS
LS LINKS
LEC DIGITAL
ADC
MONITORING
SBB
x12
LOCAL DOMAINS LAYER
TILE
DIGITAL
ANALOG


GxVDD
GxVSS
PSUB
PWR SWITCHES
TILE
MATRIX
LxVDD
LxVSS
LEVEL SHIFTERS
+ BUFFERS
TILE_TO_PSUB
TILE_ON
SRV ENDPOINT
x72
IO's
SRV SC MASTER
SRV SLOW CONTROL BUS
LEFT ENDCAP
STITCHES
SERVICES PWR DOMAIN
GLOABL PWR DOMAIN
LOCAL PWR DOMAIN

Detector R&D

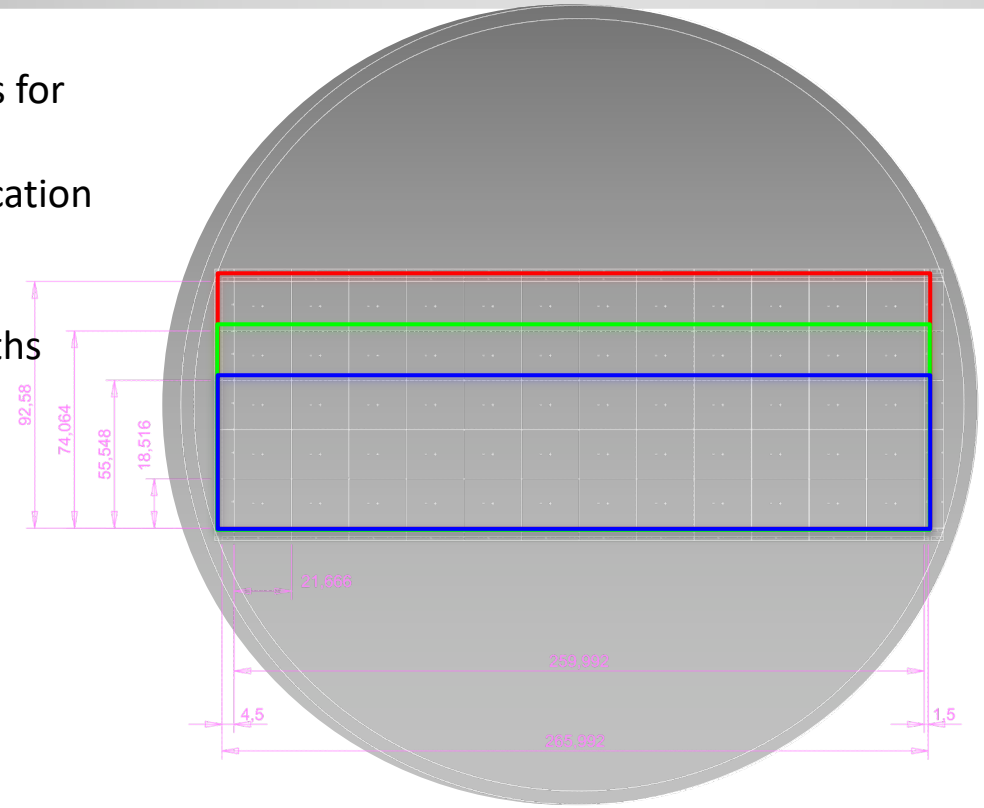
Production: ER2 & ER3

Now

Q3 2026

Engineering Run 2

- Different pixel variants for operational margins
- Design in-depth verification ongoing
- 33 wafers: 4 months
- 25 pad wafers: 3 months
- 1 month for dicing



PX1	PX2	PX3	PX4	PX5	PX6
PX7	PX8	PX9	PX10	PX11	PX12

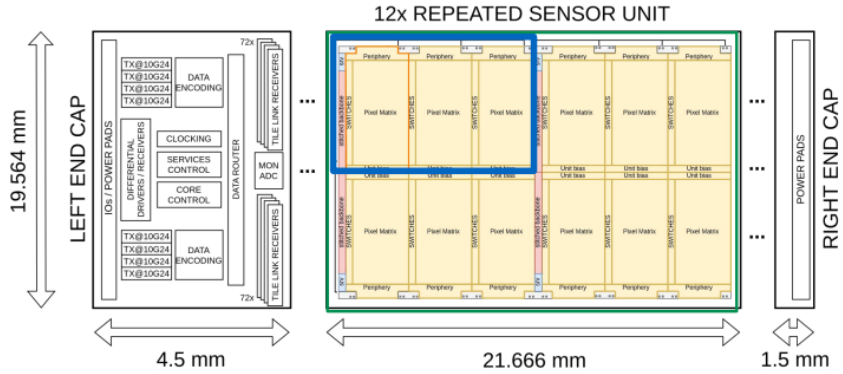
Engineering Run 3

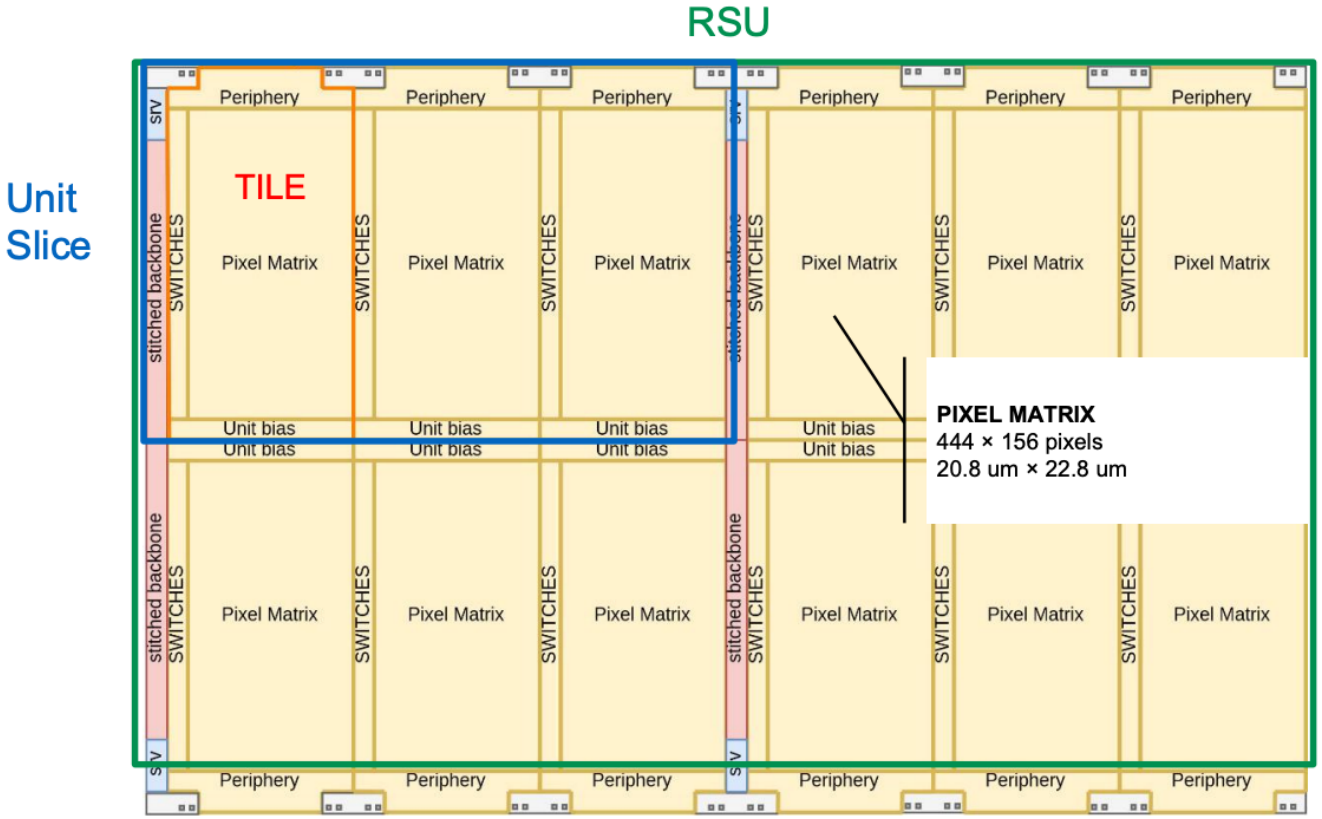
- Final pixel variant
- Functionally identical to ER2
- ER2 implementation procedure and scripts identical for ER3-For ER3 much shorter design and verification
- As little as 6 wafers needed

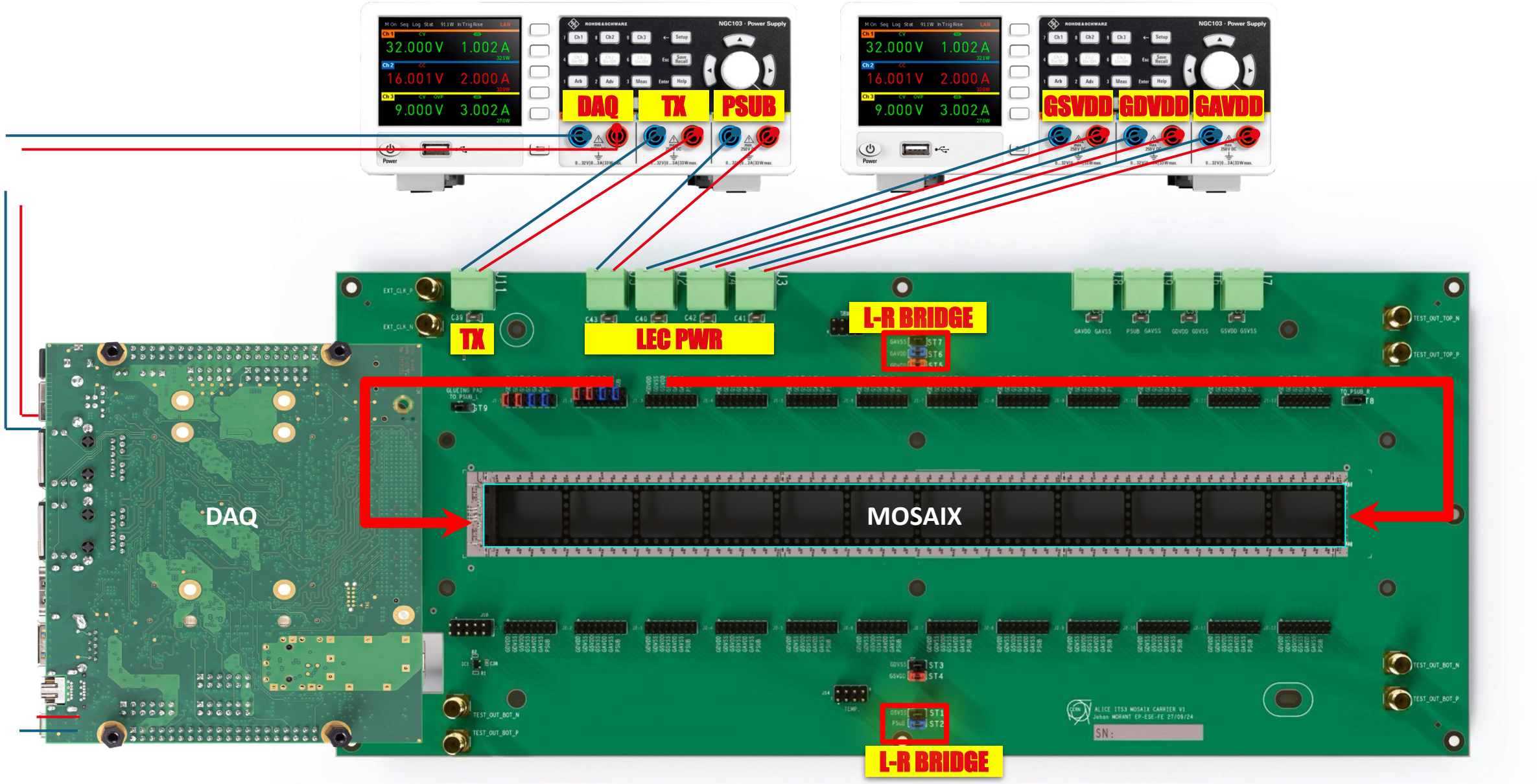
?	?	?	?	?	?
?	?	?	?	?	?

Simplified overview

- 12 RSUs
- 4 unit slices per RSU
- 1 service node per unit slice
- 12 tiles per RSU (6 top & 6 bottom)
- 4 readout regions per tile
  - Combined into 1 tile readout link






DAQ
TX
PSUB
GSVDD
GDVDD
GAVDD
TX
LEC PWR
L-R BRIDGE
DAQ
MOSAIX
L-R BRIDGE