SVT Quality Control

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SVT Working Meeting
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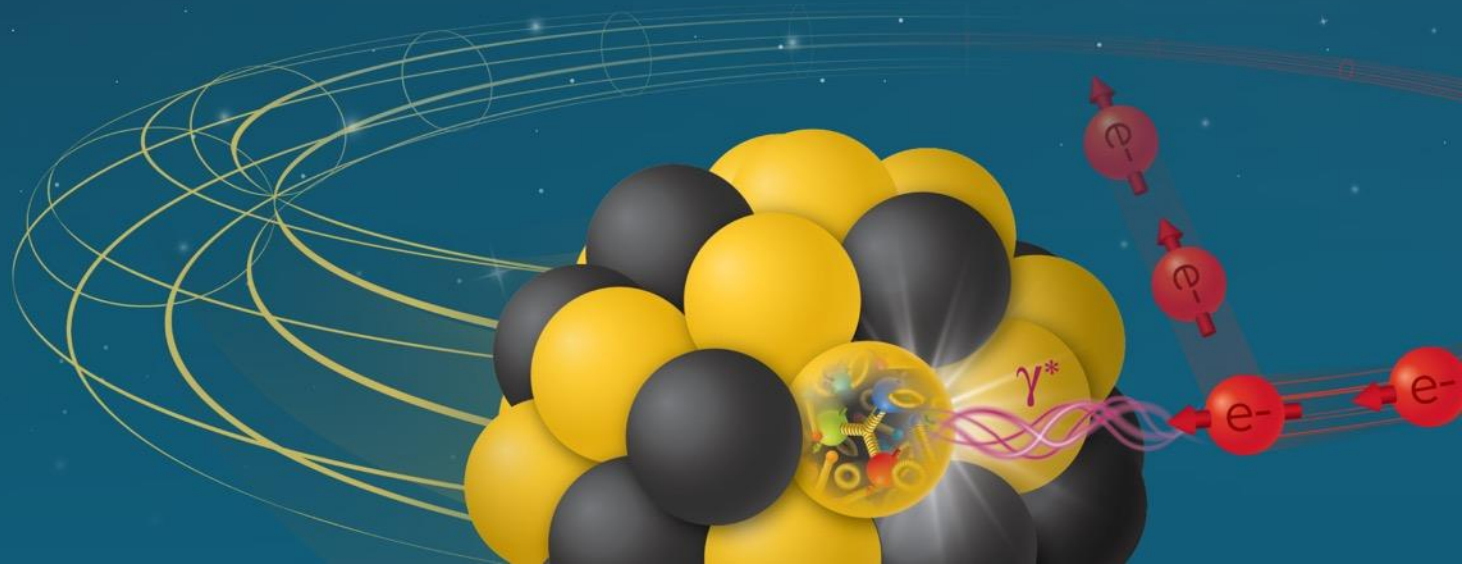
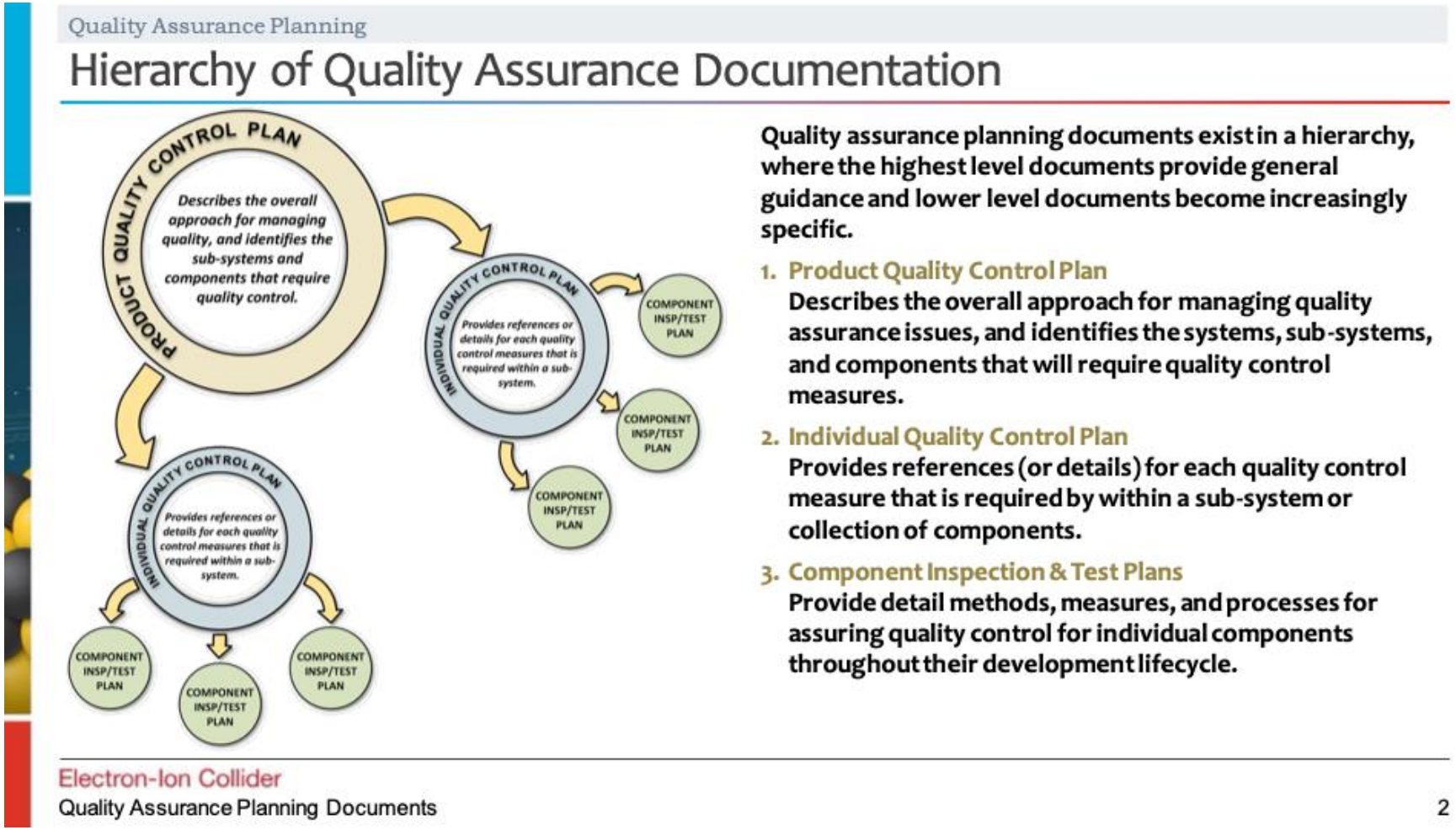
Electron-Ion Collider



Hierarchy of Quality Assurance Documentation

https://eic.jlab.org/Detector/#QUASet



Hierarchy of Quality Assurance Documentation

- Product Quality Control Plan (PQCP)
  - Overarching document for the whole detector, maintained by the project (Walt Akers)
- Individual Quality Control Plan (IQCP)
  - One document per single Level-3 or Level-4 (project) WBS sub-system
  - SVT - WBS 6.10.03.01 IQCP - Vallary + Laura
- Component Inspection & Test Plans (ITP)
  - One document per SVT component that needs QC
  - To be prepared by the SVT

Component Inspection & Test Plans (ITP)

- This is where we define our QC procedures
- The inspection and test plans go over the **specifications/requirements**, the process to measure those, the **setups** with pictures/photos, what **EH&S** considerations are applicable for the inspections, and how we **document/keep records**
- They are written from the "scientist view"
- ITP documents are a case of “less is more”, keep it brief and to the point, no need for many details

SVT components that undergo QC

- Initial list provided by the SVT for the Product Quality Control Plan (PQCP)
- More components to be added if needed as we work through QC procedures

The following components are subject to quality control

- Sensors: wafer probing of sensors (wafer-scale and EIC-LAS) prior to thinning and dicing,
- Ancillary ASICs: wafer probing prior to thinning (if any) and dicing,
- Flexible Printed Circuits (FPCs): electrical tests for the inner barrel, outer barrel, and disks.
- Assembled inner-barrel (half-)layers and shells (at a minimum electrical functionality) at assembly sites.
- Outer barrel modules (assemblies each consisting of two EIC-LAS, two ancillary ASICs, a bridge FPC).
- Outer barrel staves (electrical functionality, possibly mechanical and thermal) at assembly sites.
- Disk modules (assemblies each consisting of an EIC-LAS, an ancillary ASIC, and a bridge FPC),
- Half-disks (electrical functionality, possibly mechanical and thermal) at assembly sites.
- Readout boards - interface boards, control boards, power boards, (fiber) aggregator boards - following assembly and prior to shipping to BNL.
- Support cylinder and cones following production at production sites,
- Reception tests of IB, OB staves, half disks at BNL prior to installation (electrical).
- Global integration tests.

SVT QC procedures and ITP

- Sensors QC – Anhelina, Ivan, Lukas
  - ITP document prepared by Anhelina, Ivan, Lukas
  - Wafer probing procedures for MOSAIX and EIC-LAS as defined by MOSAIX designers
  - Review by Joao, Jo, Laura, Vallary
  - ITP document presented at WPCo and SVT meetings
  - ITP document released to project

- Outer barrel and disk modules QC
  - Module QC procedures drafted by Marcello, Matthew, James, Jian
  - Review by Iain, Nikki, Laura, Vallary; found inconsistencies between proposed tests and AncASIC/EIC-LAS design
  - Re-worked document ready for second pass of review
  - Presentation today
  - Aim to converge and release ITP to project by SVT PDR2 (week of January 26)

SVT QC procedures and ITP

- Readout boards QC
  - James started to draft QC procedures
  - Presentation today
  - Next steps
    - Implement today's feedback and prepare first ITP document for review

- Proposed QC to be defined next
  - FPC (once module is done)
  - Support cylinder and cones
  - Global Integration tests
  - AncASIC (after March submission)