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OB module: powering tests

WP3 Electrical interfaces

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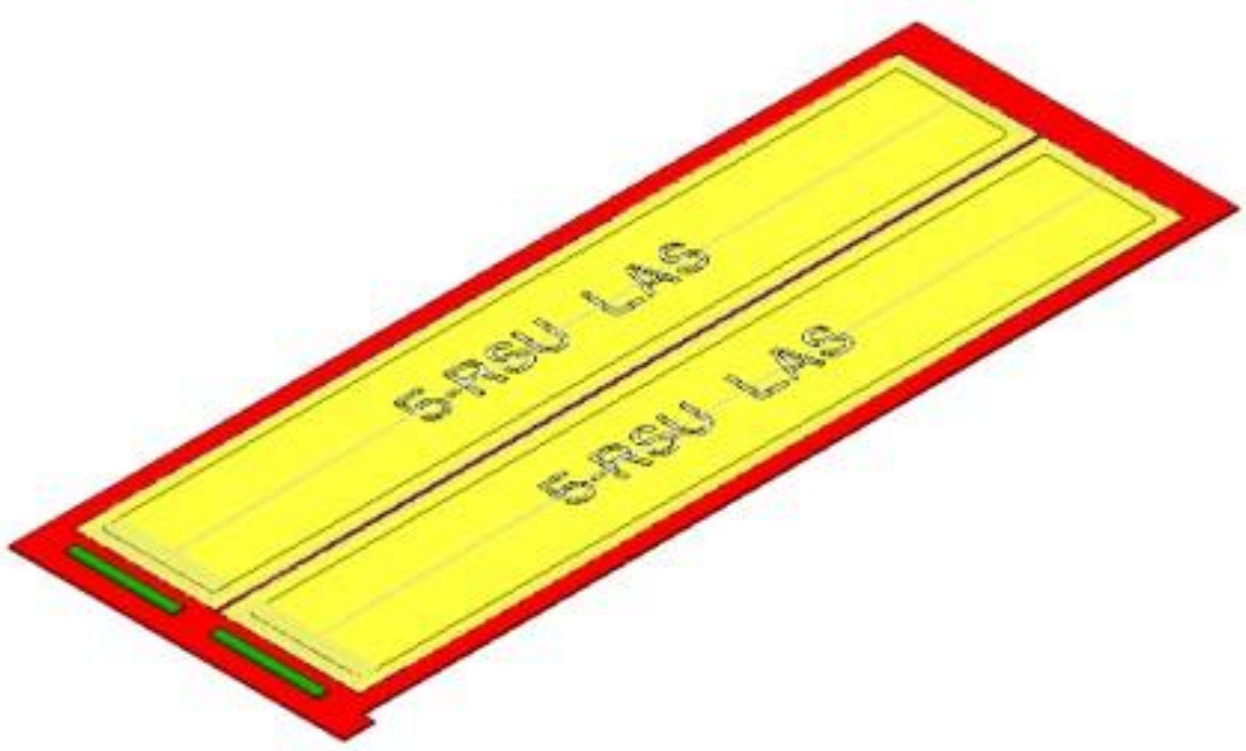
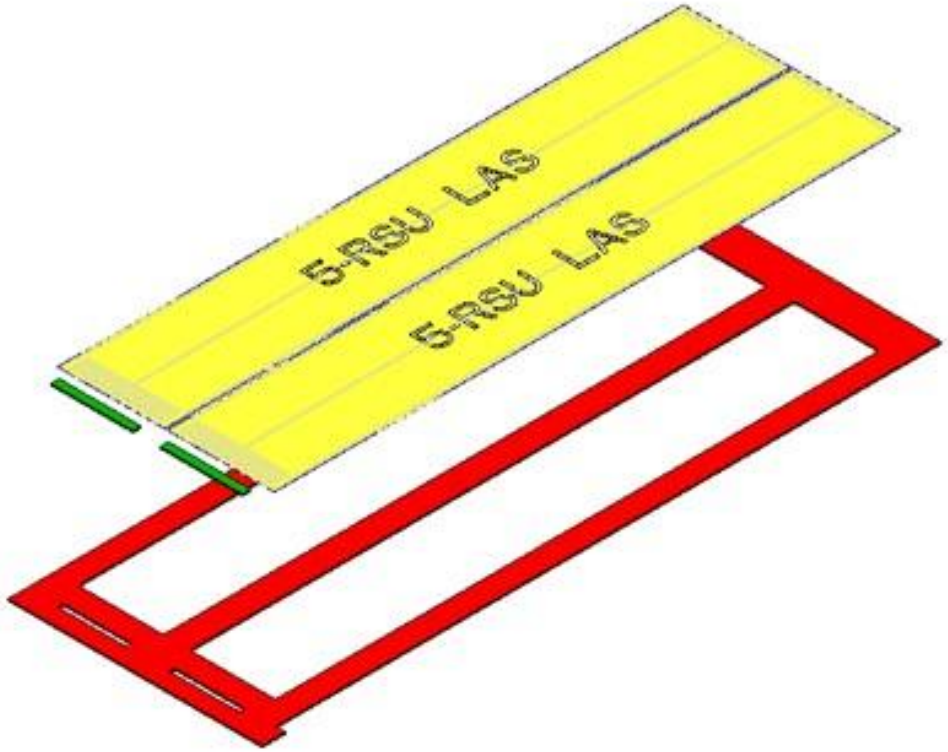
Overview of module





Goal: to capture how a powering test would look like on a module.

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Note: powering tests on a module depend on built-in features of AncAsic.

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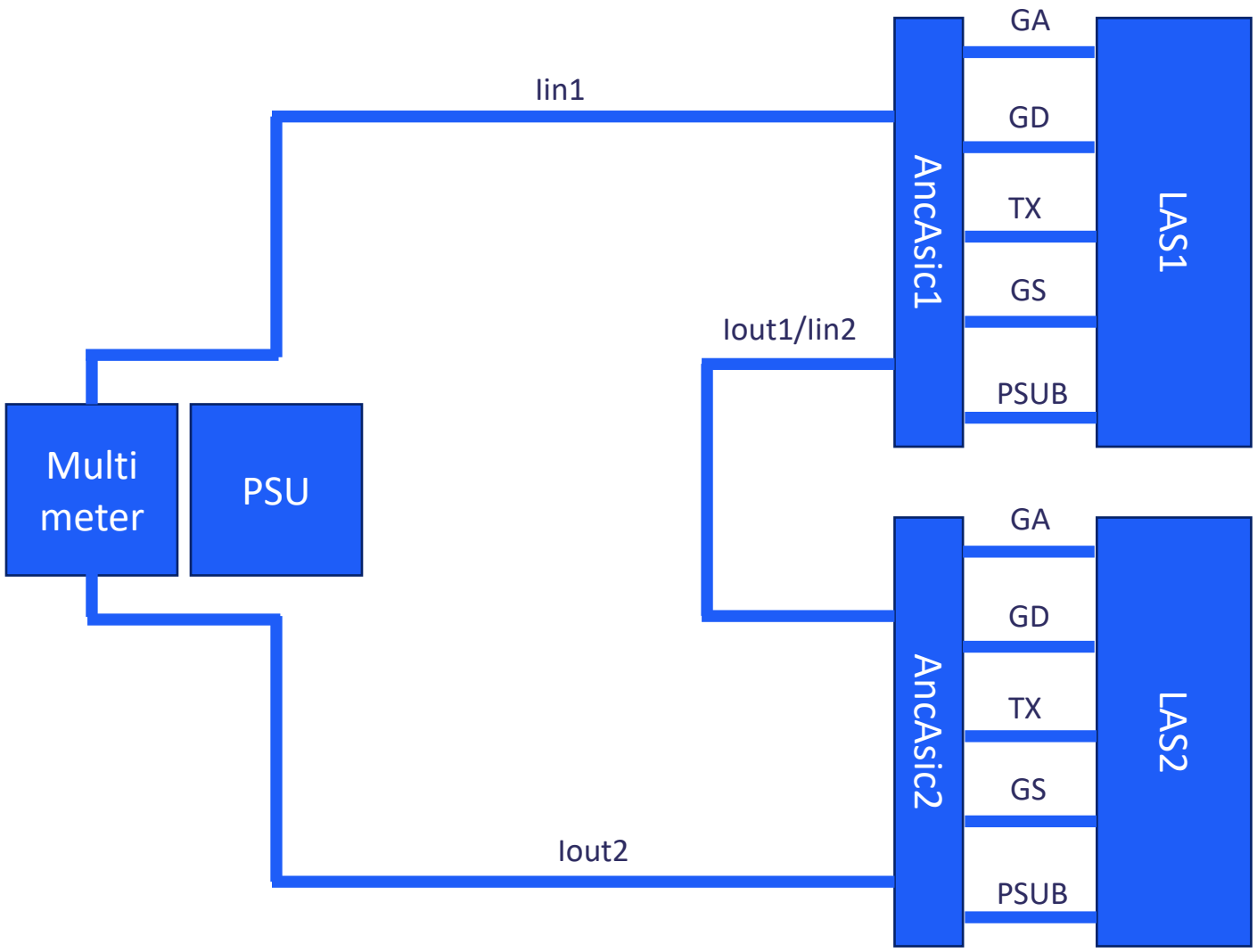
Step0 - power off

Probe lines to detect shorts or opens.



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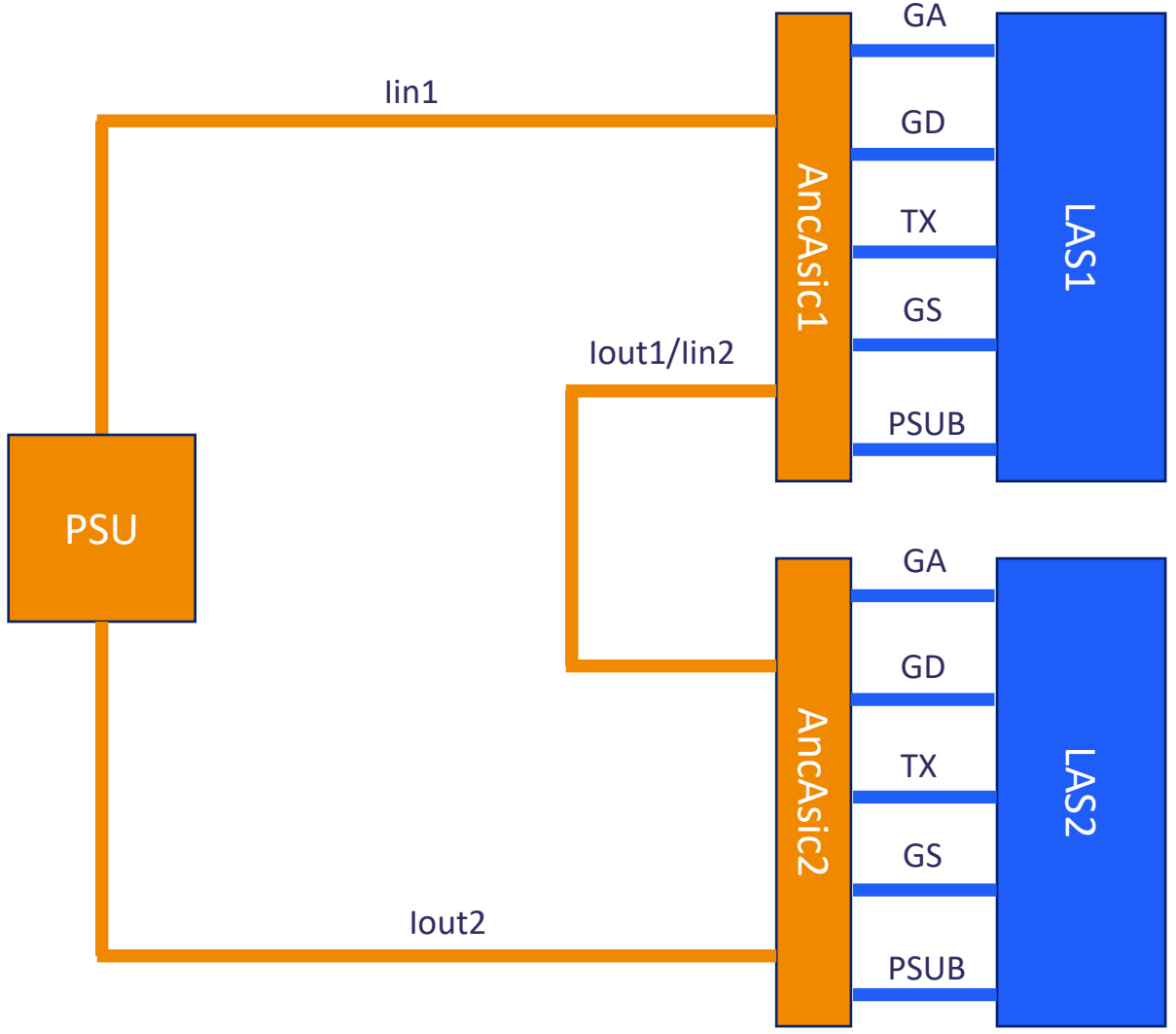
Step1 – AncAsics ON

Digital communication test:
Q:can perform configuration and read/write register operation on each AncAsic in this powering condition?
A: Yes, Arif: “to send read command from the control room”

GA, GD, TX, GS, PSUB are in high-impedance.

Measure PWR consumption on PSU and compare it to reference value.

Q: Is there a possibility to switch 1 AncAsic ON at the time?
A: No, Iain: “once a serially powered chain is constructed, I don’t think there is a way to turn off 1 AncASIC – it would mean asking the AncBrain to shut down its own supply, and then there would be no way to tell it to turn on again without a hard restart”



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Step2 – LAS1 ON

Digital communication test:
Q: can perform configuration and read/write register operation on the LAS this powering condition?
A: Yes, Arif: “to send read command from the control room”

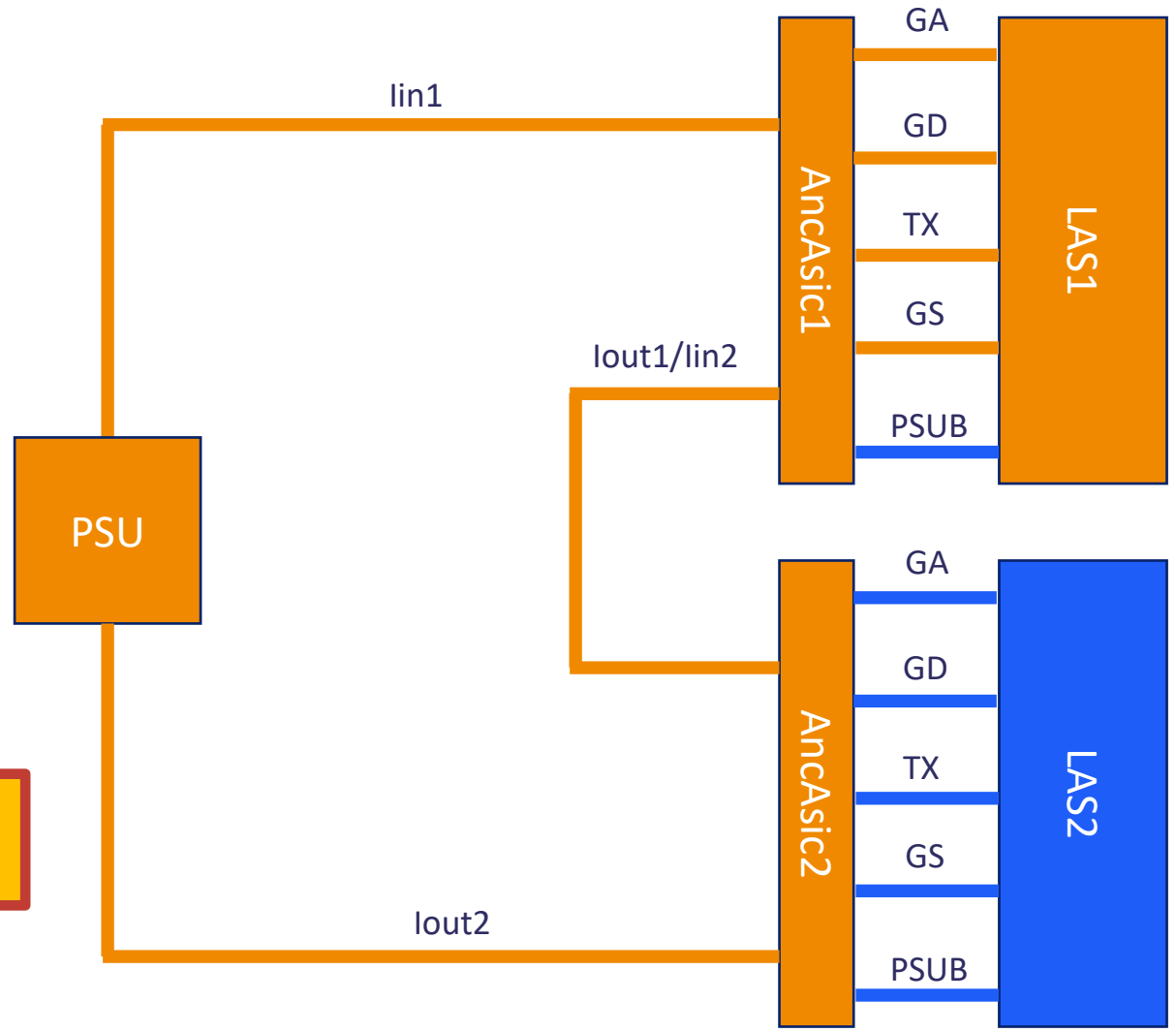
GA, GD, TX, GS are live (nominal).[range: 1.1V to 1.4 V]
PSUB is in-high impedance (off).

Measure V in output for GA, GD, TX, GS.

Shorts: Monitor Over Current Protection (OVC) flag (hardcoded) for GA, GD, TX, GS.

Opens: Q: any way to do it? Like an “Zero Current” flag?

Repeat measurement for under-bias and over bias condition (e.g. min, max).



PSUB supplied by NVG → Iain: “To check with Soumyajit about NVG high-impedance state”

Arif: “The NBVG will be turned off/on by dedicated commands from the control room”

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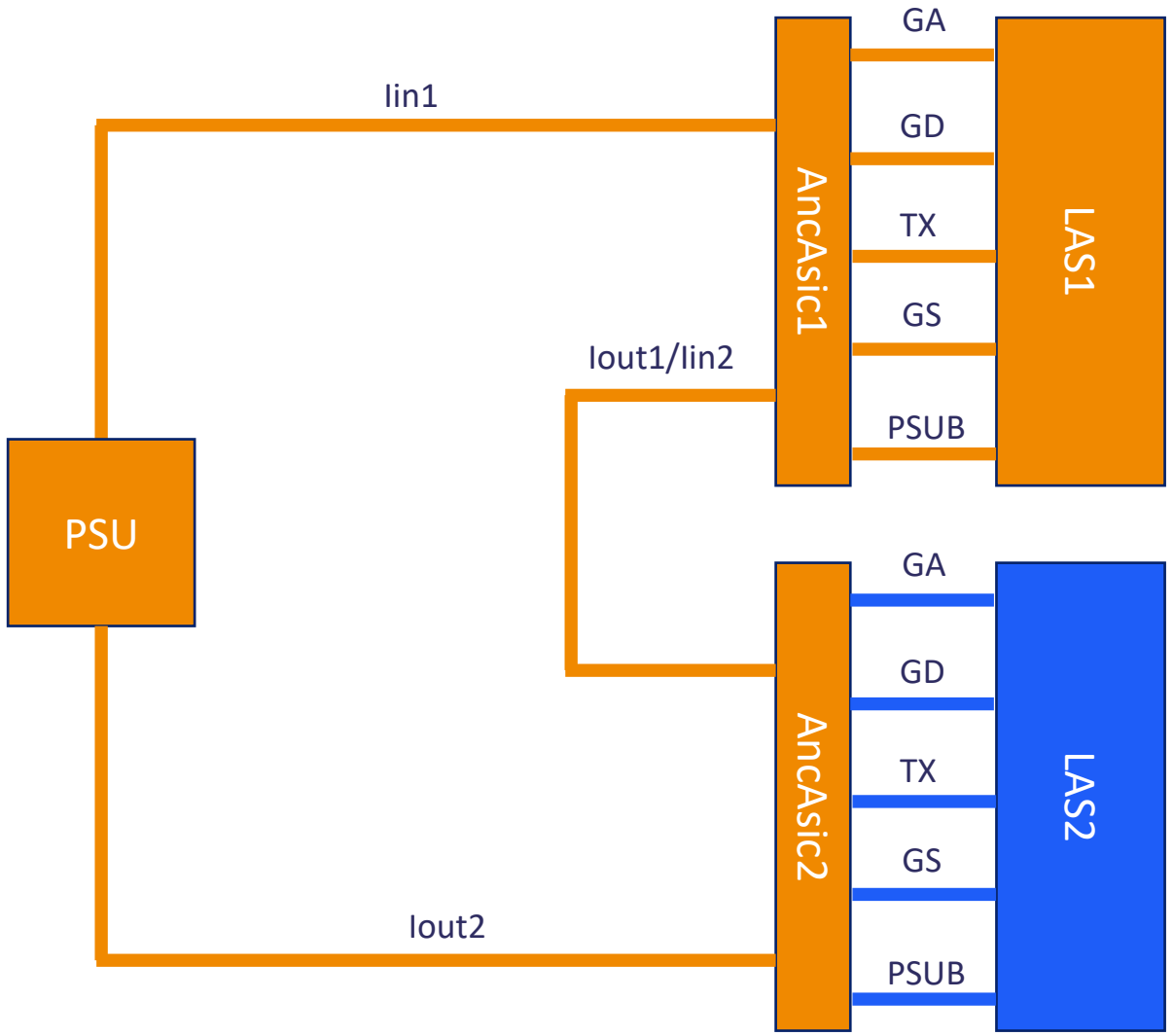
Step3 - LAS1 ON (w PSUB)

GA, GD, TX, GS are live (nominal).
PSUB is live. [range: 0V to -6V(??)]

Measure V in output for GA, GD, TX, GS and **PSUB**.

Monitor Over Current Protection (OVC) flag for GA, GD, TX, GS and **PSUB(?)**.

Q: To perform IV measurement if ADC is implemented?



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Step3 - LAS1 ON (w PSUB) (continued)

GA, GD, TX, GS are live (nominal).
PSUB is live. [range: 0V to -6V(??)]

Measure V in output for GA, GD, TX, GS and **PSUB**.

Monitor Over Current Protection (OVC) flag for GA, GD, TX, GS and **PSUB(?)**.

Q: To perform IV measurement if ADC is implemented?

Q:How to detect an overcurrent in output from the NVG?
(SLDO has the Over Current Protection (OCP) flag)
(NVG may have the ADC to read output current? and output voltage?)
Soumyajit: We are adding an output current monitoring function to the NVG (not present in the current prototype being tested) . The sensed current will be digitized by the monitoring ADC. If required, we can add a digital comparator function to the ADC output that generates an OCP flag.

Q:Is the output range of NVG 0 V to -6V? What granularity do you envisage for the voltage setting?
Soumyajit: "The nominal output range is -1V to -5 V. The voltage can be set by an 8-bit reference DAC (design completed but not included in the current prototype). This results in an effective step size / output voltage resolution of ~20 mV"

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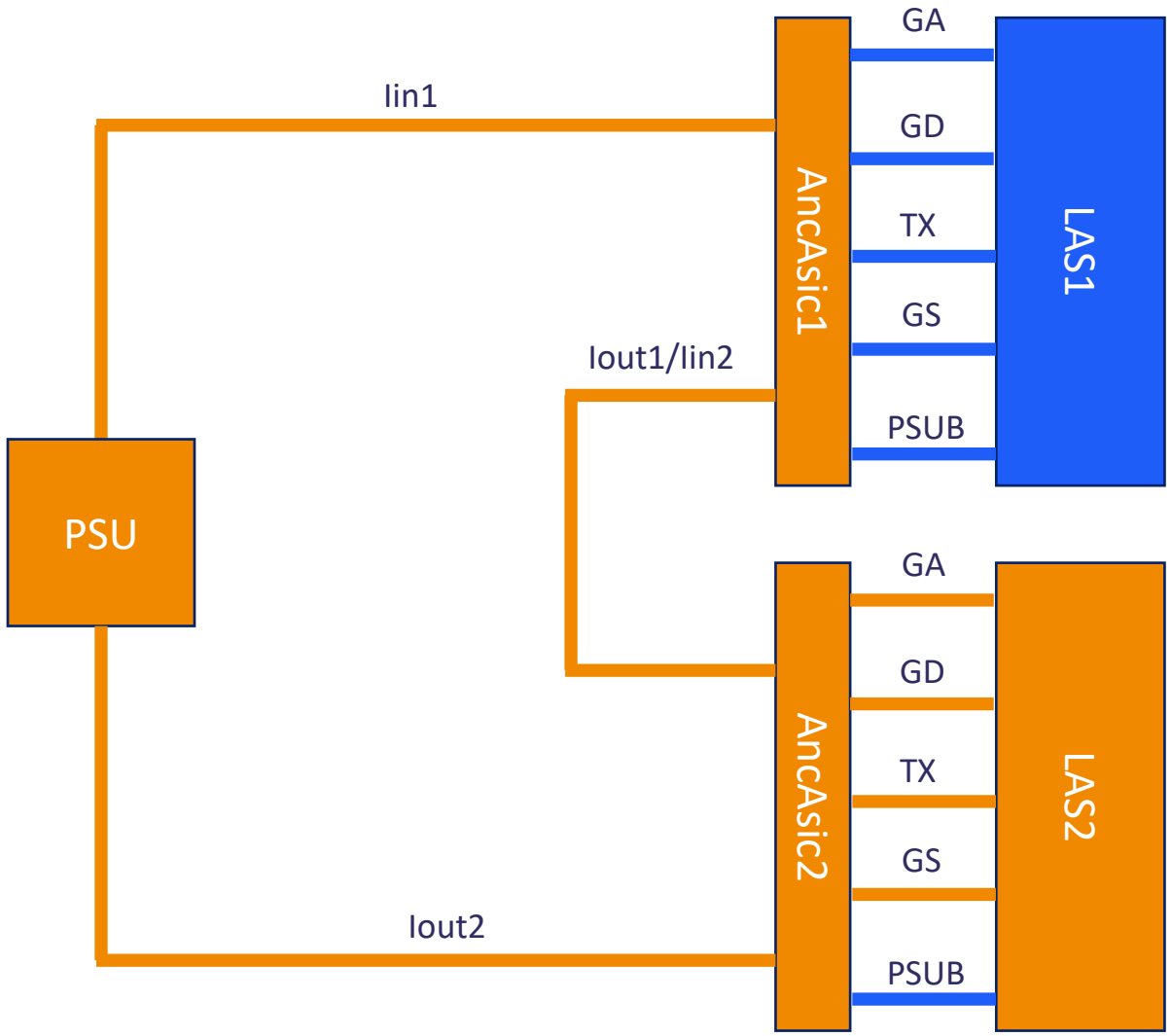
From: "SVT Sensors Inspection and Wafer Probing"

PSUB	Global substrate bias	-2, -1.20, 0

Step4 – LAS2 ON

See description for “LAS1 ON”



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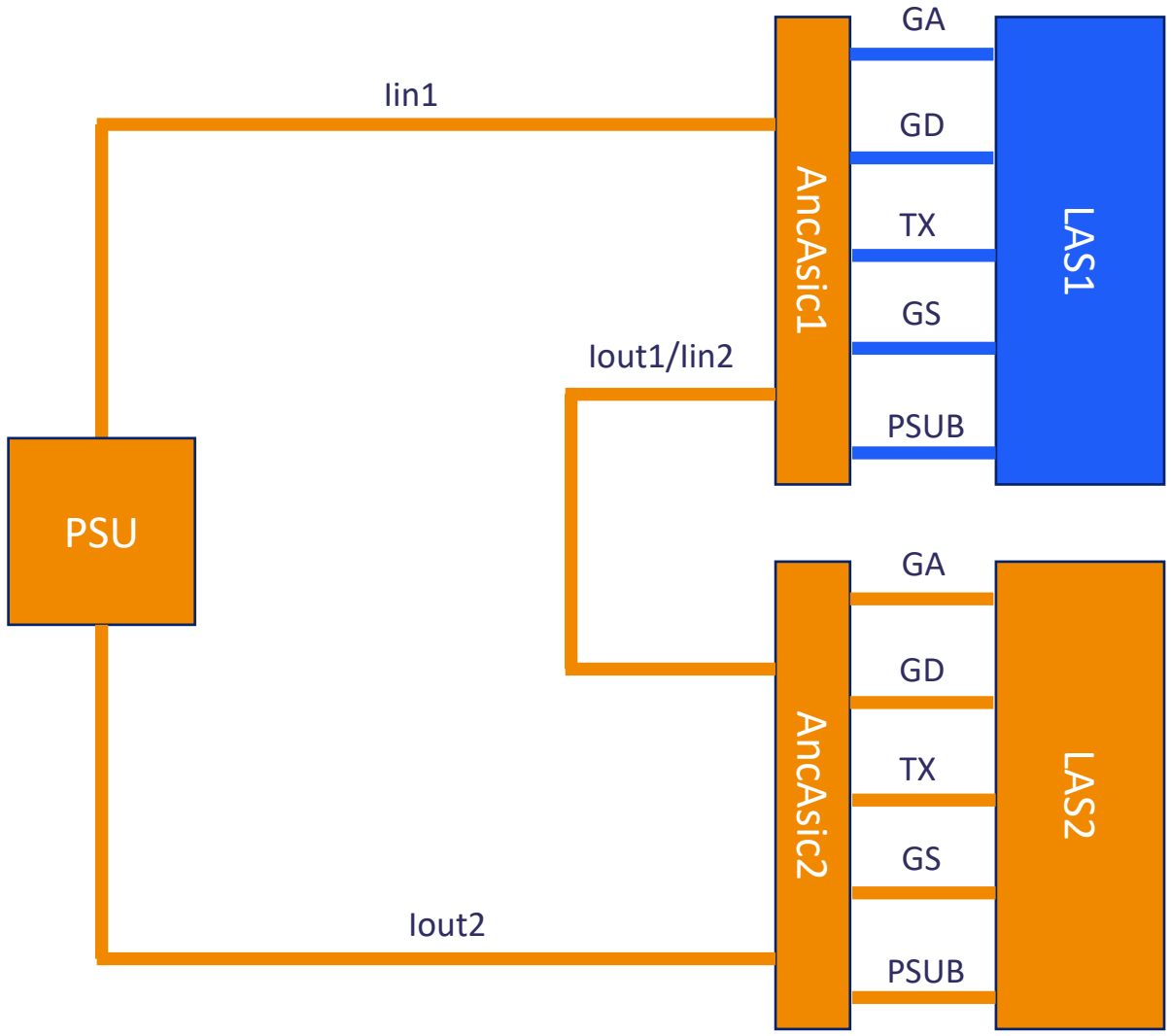
Step5 – LAS2 ON (w PSUB)

See description for “LAS1 ON (w PSUB)”



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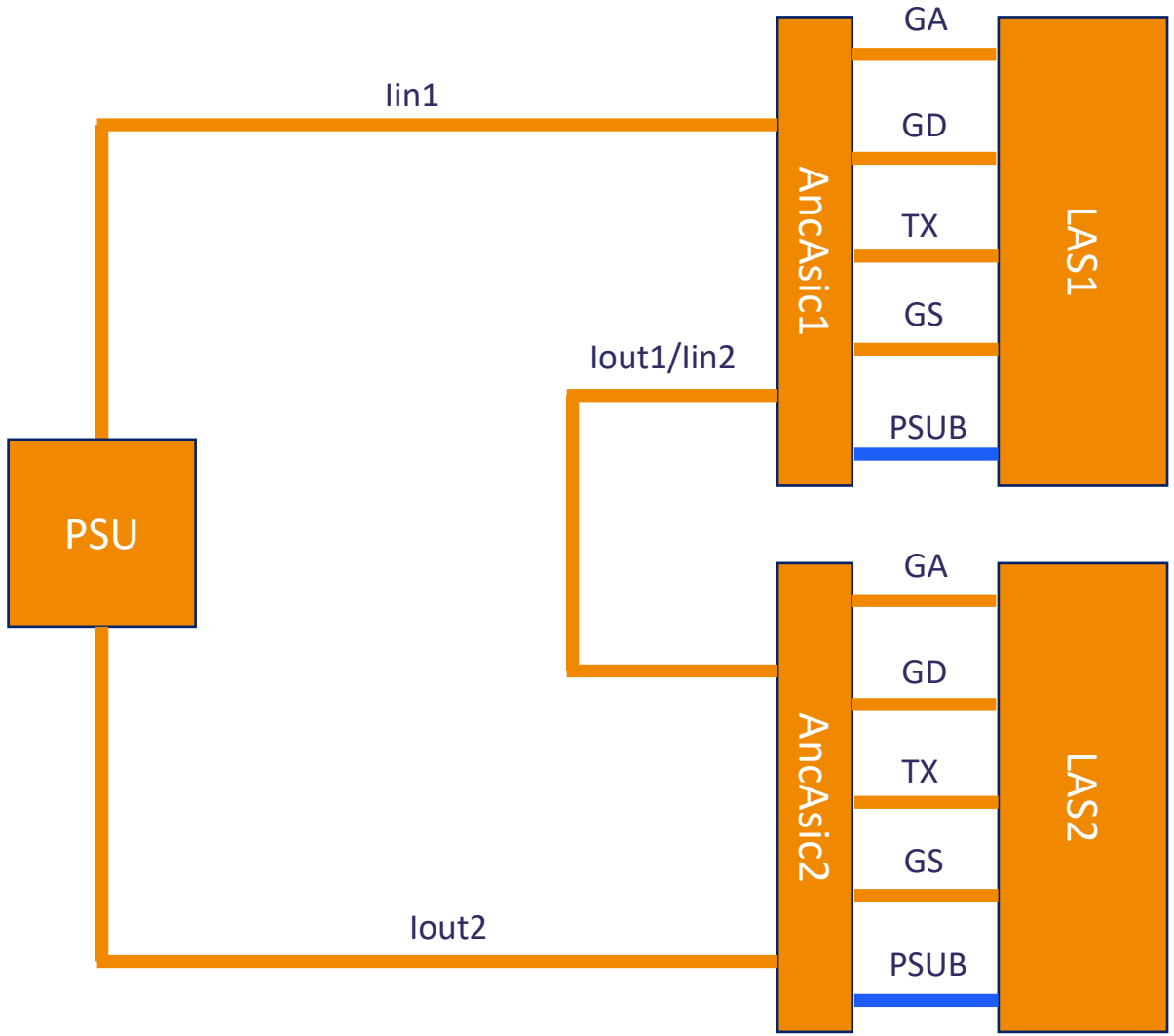
Step5 – LAS1 and LAS2 ON

GA, GD, TX, GS are live (nominal).
PSUB is in-high impedance.

Measure V in output for GA, GD, TX, GS.

Monitor Over Current Protection (OVC) flag for GA, GD, TX, GS.

Repeat measurement for under-bias and over bias condition (e.g. min, max).



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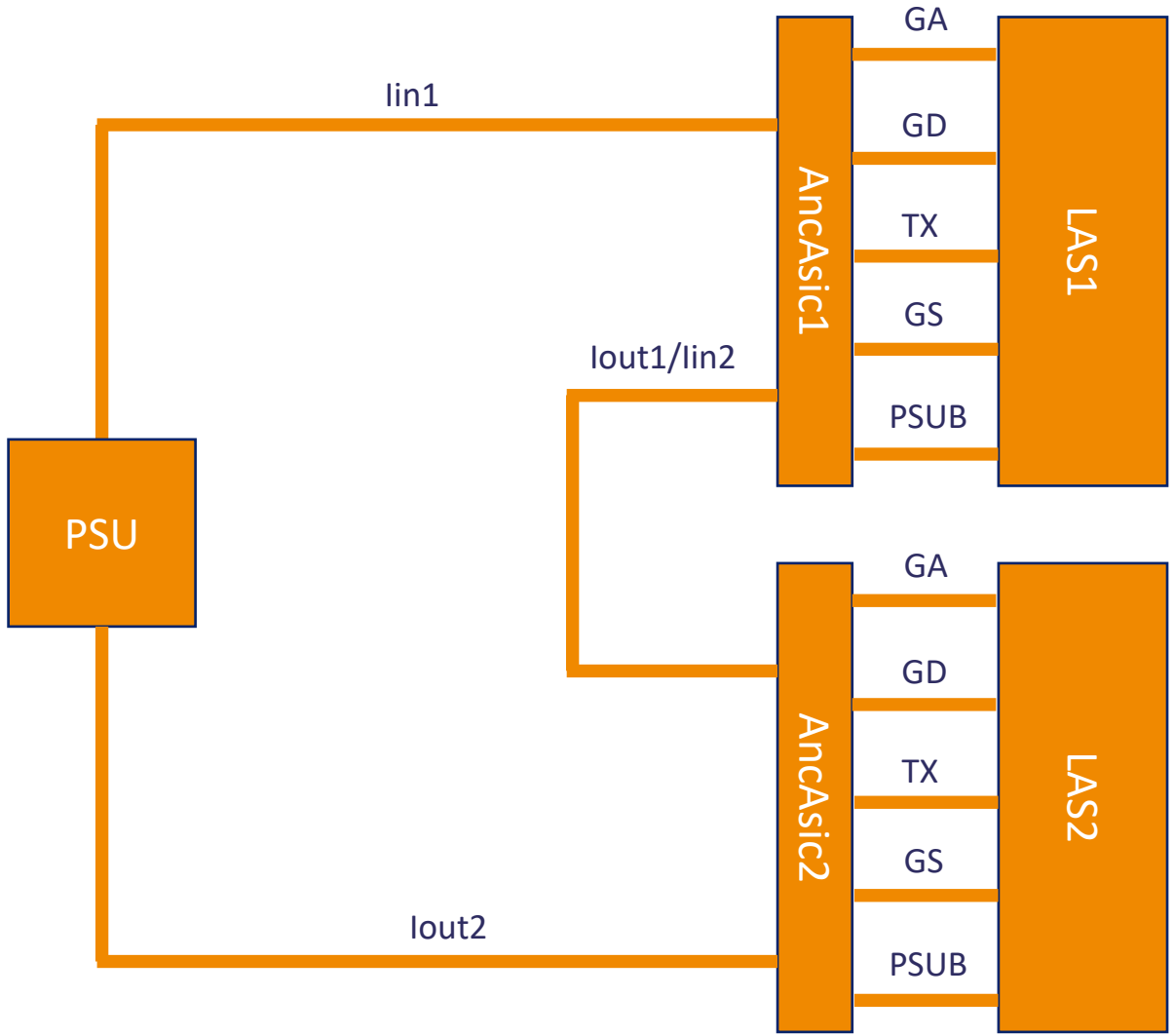
Step6 - LAS1 and LAS2 ON

GA, GD, TX, GS are live (nominal).
PSUB is live.

Measure V in output for GA, GD, TX, GS and **PSUB**.

Monitor Over Current Protection (OVC) flag for GA, GD, TX, GS and **PSUB(?)**.



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Conclusion

Sketched how a powering test on a module could look like based on the existing knowledge of the features implemented on AncAsic.

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Thank you

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