Detector Module
Inspection and Test Plan

Author Names

M.Borri[1], M.Buckland[1], J.Glover[2], J.Liu[3]

Institution(s)
1- UKRI STFC Daresbury Laboratory [UK]
2- University of Birmingham [UK]
3- University of Liverpool [UK]

Abstract

Detector modules for Outer Barrels and Endcaps are pre-assembled and pre-tested and then mounted and electrically interlinked in the final staves and disks. Detector modules are electrically self-contained units. They break-down by design the complexity of a stave and a disk into sub-units. This is beneficial in order to identify faults and rework and reject units before their mounting on staves or disks.

Contents

List of Figures

1. DETECTOR MODULE PROPERTIES

Detector Modules are self-contained units that group together one or multiple pairs that consist of a Large Area Sensor (EIC-LAS) and its corresponding Ancillary ASIC (AncASIC). This electrically coherent unit respects the functional interface between the EIC-LAS and the AncASIC. It reflects the electrical dependency of the EIC-LAS from the AncASIC for clock distribution, digital communication and power network.

The main components of a module are:

- Large Areas Sensor (EIC-LAS)
- Ancillary Asic (AncASIC)
- Flexible Printed Circuit (FPC)
- Epoxy glue
- Electrical interconnects (i.e. wire-bonds, spTAB)
- [Only for Endcaps modules] carbon-fiber support-plate

The following requirements define the quality plan for detector modules.

Pre-assembly requirements			
	Space, equipment and storage		
		Parameter	Value
		Cleanliness of the assembly area	≥ISO6 (estimated)
		Servicing of equipment for electrical interconnection	Active maintenance contracts (estimated)
		Calibration of power supplies and oscilloscopes	Yearly calibration certificates (estimated)
		Environmentally controlled storage of EIC-LAS and AncASIC	Procurement of suitable storage (estimated)
	Components acceptance testing		
Post-assembly requirements			
	Mechanical		
		Parameter	Value
		Mechanical alignment of module components	~100-200 μm (estimated)
		Welding integrity of microelectronics interconnects	If wirebonding: pull force >10 gF (estimated) If spTAB: to be defined
	Electrical		

		Parameter	Value
		AncASIC: Powering tests	Lack of short and open circuits (estimated)
		AncASIC: Digital communication tests	Error free digital communication (estimated)
		EIC-LAS: Powering tests	Lack of short and open circuits (estimated)
		EIC-LAS: Digital communication tests	Error free digital communication (estimated)
		EIC-LAS: In-pixel tests	< 2% of bad pixels (estimated)
		EIC-LAS: Noise occupancy tests	Below maximum noise hit rate (to be defined)

Modules will be graded against a quality scale that combines the results of the post-assembly tests.

2. PROCESSES AND PROCEDURES

2.1. Pre-assembly: Workspace, equipment and storage

The workspace, equipment and storage of detector modules is standardized and monitored.

Cleanliness of the assembly workspace: to check that the cleanliness of the workspace is sufficient to handle and interconnect 50 µm thin sensors with interconnection pads of ~100 µm size. Failure to do so would impact on the module production yield.

Servicing of equipment for electrical interconnection (e.g. wirebonding machines): to check that the equipment used to electrically interconnect the detector modules is reliable and does not develop faults that could lead to major downtime and delays in the production of modules.

Calibration of power supplies and oscilloscopes: to check that the equipment is reliable to supply and measure electrical currents and electrical potentials.

Environmentally controlled storage of EIC-LAS and AncASIC: to prevent deterioration of components after acceptance testing.

2.1.1. Verification Testing

- **Cleanliness of the assembly workspace:** periodic certification of the workspace to meet ISO6 or higher, following the ISO 14644-1 standard.
- **Servicing of equipment for electrical interconnection(e.g. wirebonding machines):** periodic servicing and maintenance of the equipment for electrical interconnection (i.e. wire-bonding machines).
- **Calibration of power supplies and oscilloscopes:** periodic calibration of the equipment.
- **Environmentally controlled storage of EIC-LAS and AncASIC:** to store EIC-LAS and AncASIC in dry storage units.

2.2. Pre-assembly: Components acceptance testing

The components and tools required to assemble detector modules require acceptance testing in order to very their compliance with their individual specifications. This process checks that components are suitable for the production of detector grade modules.

2.2.1. Incoming Inspections or Acceptance Testing

- EIC-LAS and AncASIC acceptance testing: to check that the chips are compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database containing results of verification tests (e.g. visual inspections, metrology and electrical tests) [To clarify post-dicing tests: electrical and metrology?] performed at the EIC-LAS and AncASIC QC sites.
- FPC acceptance testing: to check that the FPC is compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database containing results of verification tests (e.g. visual inspections and electrical tests) performed at the FPC QC sites.
- Epoxy glue acceptance testing: to check that the glue is in date and stored according to the manufacturer's requirements.
- [Only for Endcaps modules] Carbon-fiber support-plate: to check that the Carbon-fiber support-plate is compliant with detector grade requirements. To be assessed via visual inspection and access to a shared database containing results of verification tests (e.g. visual inspections, metrology and electrical insulation tests) performed at the manufacturing sites.
- Jigs and tools to be metrology tested via coordinate measurement machines at metrology workshops before deployment. This guarantees compliance with the mechanical tolerancing specified in their related mechanical drawings. To inspect the position of alignment pins, flatness, perpendicularity.

2.3. Post-assembly: Mechanical test: Mechanical integrity and alignment of module components

The mechanical integrity is assessed by surface examination of visible cracks and glue seepages obstructing interconnection pads.

The relative alignment between the EIC-LAS, AncASIC and the FPC is important to enable the electrical interconnection of the three components. The nominal clearance between components needs to be preserved.

2.3.1. Verification Testing

Visual inspection by microscope; Optical metrology.

2.4. Post-assembly: Mechanical test: Welding integrity of microelectronics interconnects

The welded joints that are required by the electrical interconnects (wirebonds and/or spTABs) are responsible for the robustness of the module electrical interconnection.

2.4.1. Verification Testing

Visual inspection by microscope; Impedance tests; Pull/shear tests on interconnects.

2.5. Post-assembly: Electrical test: AncASIC: Powering test

Impedance measurements: to check for short circuit and open circuit defects.

Power consumption measurements: to check that the device operates within the functional limits of its power domains.

2.5.1. Verification Testing

Impedance measurements: To measure the impedance of the power rail without applying any supply voltage. Measurement performed by probe testing on dedicated FPC pads.

Power consumption measurements: To set the supply current(s) and voltages(s) to the nominal value(s) and to measure the associated current(s); To repeat the measurement with the supply voltage(s) over-biased and under-biased (e.g. min, max) with respect to the nominal value(s). Measurements performed by keeping in high impedance mode all the shunt low dropout (sLDO) regulators and by turning off the negative voltage generator (NVG).

2.6. Post-assembly: Electrical test: AncASIC: Digital communication tests

Configuration and register read-back measurements: To check that the device can be configured and it communicates.

2.6.1. Verification Testing

Configuration and register read-back measurements: To configure the device and to measure the power consumption of the device after configuration. To write and read back a known value on a selected register multiple times without errors;

2.7. Electrical test: EIC-LAS: Powering tests

Powering tests: The EIC-LAS is powered via the AncASIC. The assessment of the EIC-LAS powering status is assessed via build-in features of the AncASIC.

Powering tests on the EIC-LAS check that the device operates within the functional limits of its power domains (e.g. min, nominal, max).

Via the AncASIC, it is possible to detect short circuit defects (Over Current Protection (OCP) flag).

It is not possible to detect directly any open circuit defects. Open circuit defects can be inferred only indirectly via one of the other complementary tests to assess a lack of functionality on the digital or analogue circuitry of the EIC-LAS.

2.7.1. Verification Testing

Powering tests: First part, to switch on the 4 sLDOs (global analogue, global digital, serialisers, services) [output range: +1.1 V to +1.4V] and to keep the NVG off.

To read the output voltage for each of the 4 SLDOs (global analogue, global digital, serialisers, services).

Shorts: to check that the over current protection (OCP) flag is not triggered, scan voltage from min to max monitoring the OVC flag.

Second part, to switch on the NVG [output range: 0 to -6 V(??)].

To read the voltage and current provided by the NVG via the internal ADC of the AncASIC (Note: ADC implementation is under discussion. To think of alternative if ADC is not implemented).

2.8. Post-assembly: Electrical test: EIC-LAS: Digital communication tests

Configuration and register read-back: To check that the device can be configured and communicates;

2.8.1. Verification Testing

Configuration and register read-back: To configure the device and read back a register. Furthermore, to write and read back a known value on a selected register multiple times without errors.

To repeat at min, nominal, max powering configurations.

2.9. Post-assembly: Electrical test: EIC-LAS: In-pixel tests

Digital scan: to check the response of the in-pixel digital circuity and the readout path through the high-speed data links.

Digital white frame: to check which pixels cannot be masked.

Analogue scan: to check the response of the in-pixel circuity (analogue and digital) and the readout path through the high-speed data links.

Threshold scan: to check the threshold value of the in-pixel comparator and the noise of each pixel in units of electrons.

Threshold tuning: to adjust the in-pixel comparator to a certain threshold value with a narrow spread across all pixels.

2.9.1. Verification Testing

Digital scan: To inject a known number of digital pulses in the in-pixel digital circuitry of each pixel. To count the number of recorded hits detected in each pixel.

Digital white frame: To mask all pixels and inject in each of them a known number of digital pulses in the in-pixel digital circuit. To count the number of recorded hits in each pixel. A correctly masked pixel shows 0 hits.

Analogue scan: To inject a known number of analogue pulses with fixed amplitude in the in-pixel analogue circuitry of each pixel. To count the number of recorded hits detected in each pixel.

Threshold scan: To scan the amplitude of analogue pulse from low to high. For each amplitude, to inject a fixed number of pulses in each pixel and record the number of detected hits. Perform the first derivative of the obtained S-curve to extract the associated Gaussian. To extract the mean value for threshold measurement, and the standard deviation for the noise measurement.

Threshold tuning: To scan iteratively the in-pixel settings/registers (e.g. VCASN, ITHR) to set the voltage as close as possible to the target value.

2.10. Post-assembly: Electrical test: EIC-LAS: Noise occupancy tests

Noise occupancy measurement: To check the noise occupancy of the device and to determine noisy pixels.

2.10.1. Verification Testing

Noise occupancy measurement: To readout the pixel matrix for a defined total number of triggers. To calculate the noise occupancy of each pixel by dividing the number of hits by the total number of triggers.

3. EXPERIMENTAL/TEST SETUPS

3.1. Post-assembly: Mechanical tests

Visual inspections: to be performed via microscopes and/or optical metrology equipment.

Pull/shear tests on interconnects: to be performed with dedicated commercial off the shelf pull/shear test equipment.

3.1.1. Resource Requirements

Visual inspections: This is a one person task using a microscopes and and/or optical metrology equipment.

Pull/shear tests on interconnects: This is a one person task using the pull/shear test equipment.

3.1.2. Test Conditions

Visual inspections: Good lighting conditions.

Pull/shear tests on interconnects: Good lighting conditions.

3.1.3. Equipment

Visual inspections: Microscopes and/or optical metrology equipment.

Pull/shear tests on interconnects: pull/shear test equipment.

3.2. Post-assembly: Electrical tests

The electrical tests performed on detector modules will be performed by means of an automated test system. A sketch of the setup is shown in Fig.1.

3.2.1. Resource Requirements

The test system will consist of a custom made printed circuit board (PCB) for data acquisition (DAQ). This DAQ card will perform readout and control operations on the detector module. Interface and adapter cards will be used to connect the module to the DAQ card and to the commercial off-the-shelf power supplies.

Tests will be automated via scripts running on a PC. The PC will control the peripheral DAQ card and the power supplies. The software of the system will combine a series of scripted scans that will be executed sequentially as part of the qualification tests on the module. Quality factors will be extracted from the tests using fiducial cuts. They will be used to accept or reject modules.

3.2.2. Test Conditions

Electrical tests on detector modules will be performed at room temperature and in a dark environment to avoid the undesired noise produced by photo-generated currents.

It is under consideration the adoption of a metal cooling plate to support the module during the post assembly qualification tests. The metal cooling plate will regulate the temperature preventing the EIC-LAS to exceed +40C and the AncASIC to exceed +80C. The plate will be connected to a chiller with water as coolant.

3.2.3. Equipment

Tests will be automated via scripts running on a PC. The PC will control the peripheral DAQ card and the power supplies.

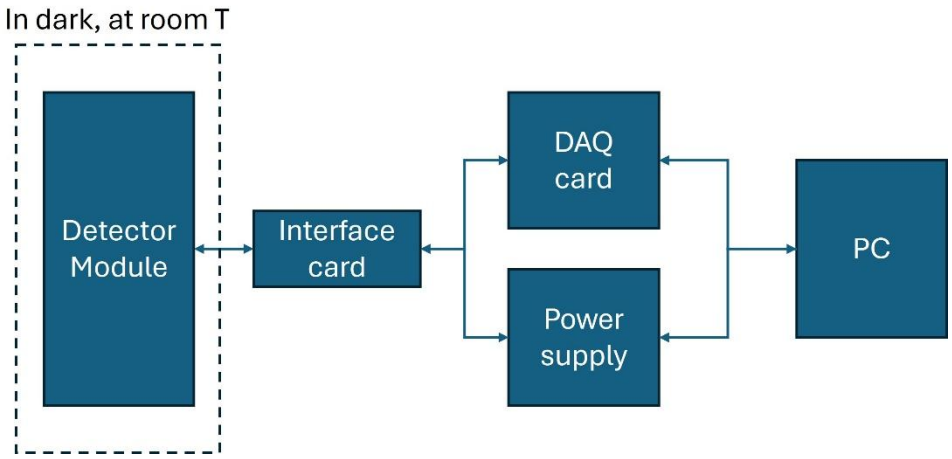

Figure 1. Set-up to perform electrical tests

4. ENVIRONMENT, SAFETY & HEALTH CONSIDERATIONS

All procedures described in this document are carried out in accordance with the **Environment, Safety, and Health (ES&H)** policies of the relevant laboratories and work areas. Activities are implemented following the established **Work Planning and Control frameworks** of the participating institutions:

- **At Lawrence Berkely National Laboratory (LBNL)**: Work is carried out according to the Integrated Safety Management (ISM), ensuring compliance with U.S. Department of Energy (DOE) regulations and the safe execution of experimental activities.
- **At UKRI STFC Daresbury Laboratory**: Activities are conducted under the UK Research and Innovation (UKRI) Health and Safety (H&S) policy. In a federated model, the Science and Technology Facilities Council (STFC) defines its own management system described by the STFC H&S Management Arrangements.
- **At University of Birmingham**: Work is regulated by University's Health and Safety policy, which defines institutional requirements for risk assessment, safe laboratory practice, and personnel protection.
- **At Purdue University:** Activities comply with the university's Environmental Health and Safety (EHS) regulations, ensuring adherence to national regulations for laboratory safety and radiation protection.

5. RECORDS AND DOCUMENTATION

5.1. Manufacturer/Producer Records

EIC-LAS: reports with acceptance tests performed by the responsible EIC-LAS QC sites within the SVT collaboration.

AncASIC: reports with acceptance tests performed by the responsible AncASIC QC sites within the SVT collaboration.

FPC: reports with acceptance tests performed by the responsible FPC QC sites within the SVT collaboration, and external manufacturers.

Technical datasheets of glues for Control of Substances Hazardous to Health (COSHH).

5.2. Deliverable Documentation and Records

Inspection sheets; Data files containing results of electrical tests; Database entries;

6. REFERENCES

SVT Sensors Inspection and Wafer Probing Test Plan - I.A. Cali1, A.Kostina2, L.Tomasek2