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Detector Module: Inspection and Test Plan: upate

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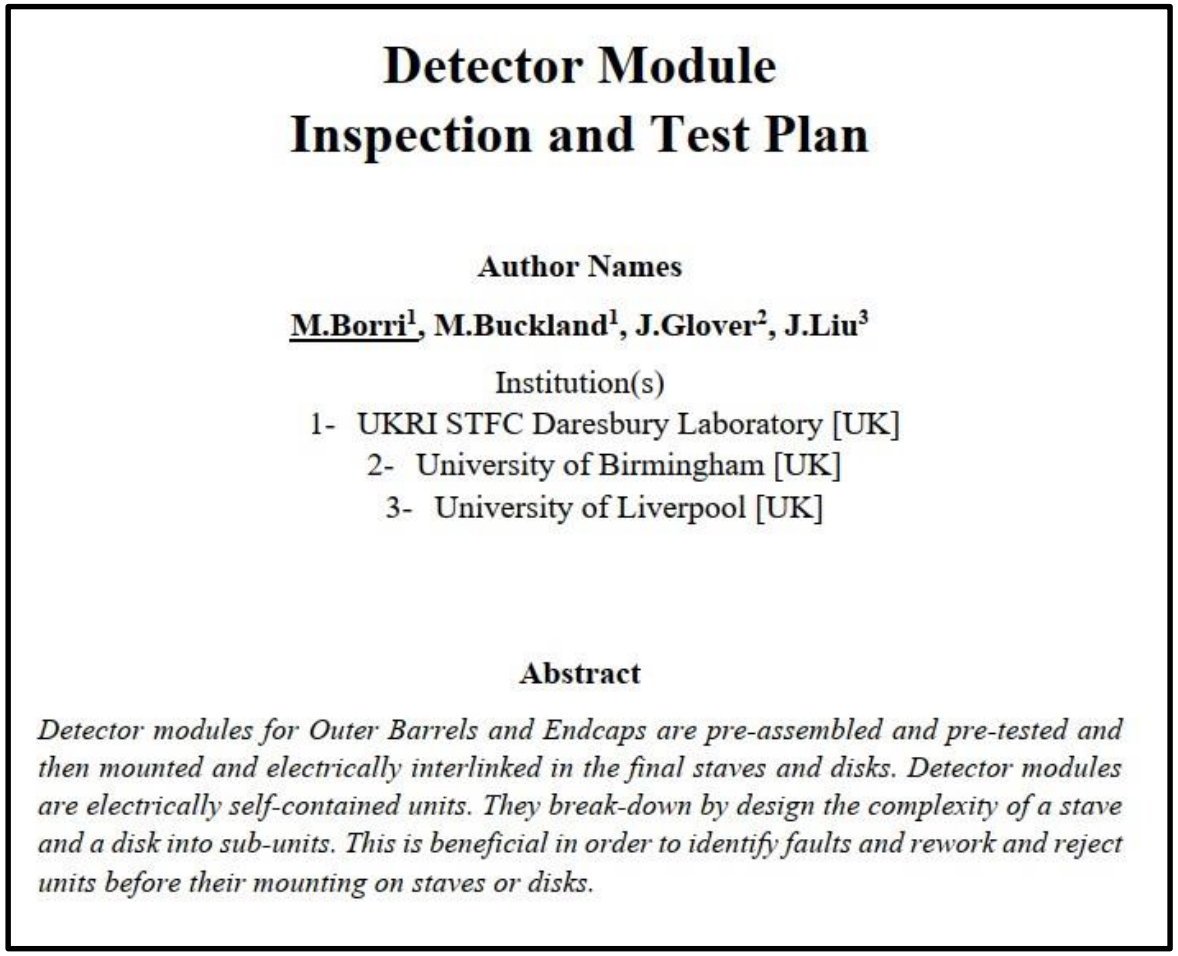
Outline

- Overview of Detector Module ITP;
- Baselined tasks:
  - OB module air tightness;
  - Disk module: carbon fibre plate;
  - Powering tests on detector modules;
- Open points:
  - Acceptance tests of LAS and AncAsic;
  - Grounding AncAsic – LAS;
- Conclusion;



Detector Module
Inspection and Test Plan

Author Names

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Institution(s)
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3- University of Liverpool [UK]

Abstract

Detector modules for Outer Barrels and Endcaps are pre-assembled and pre-tested and then mounted and electrically interlinked in the final staves and disks. Detector modules are electrically self-contained units. They break-down by design the complexity of a stave and a disk into sub-units. This is beneficial in order to identify faults and rework and reject units before their mounting on staves or disks.

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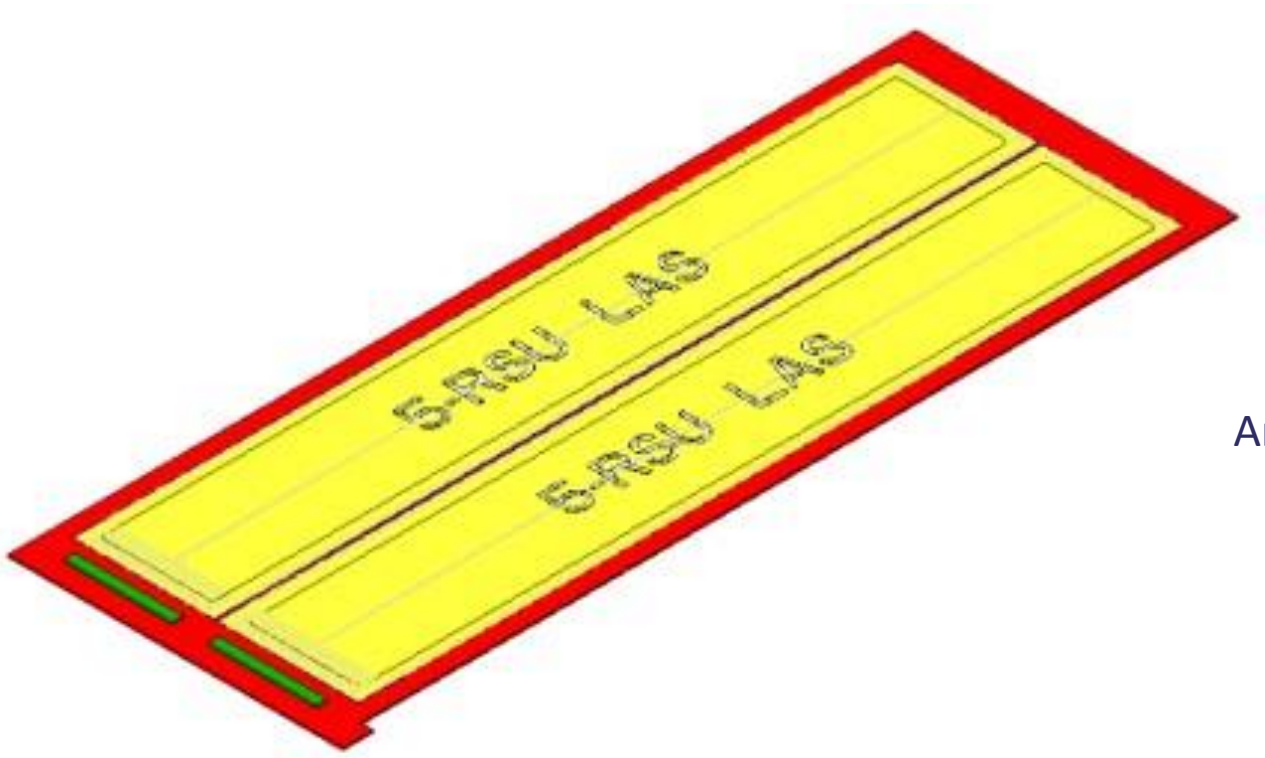
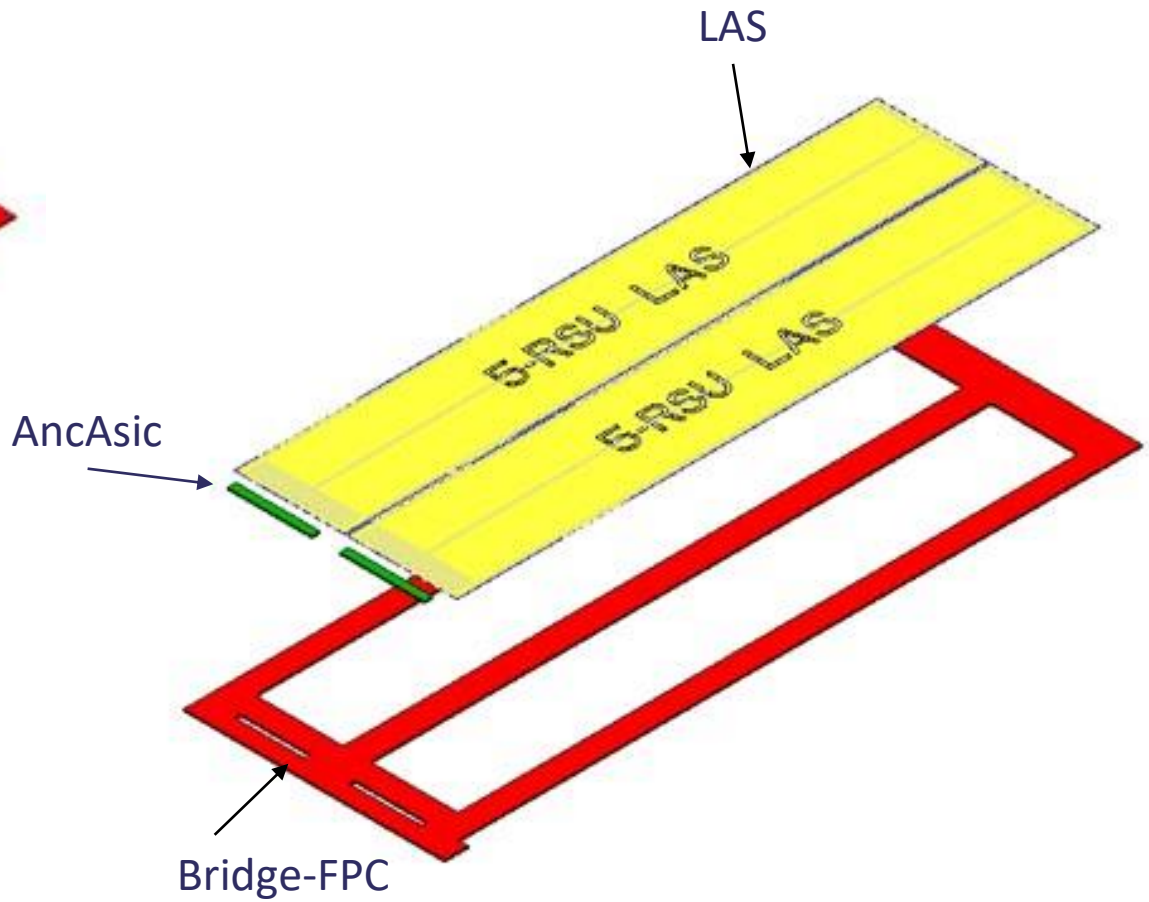
Detector module: barrels





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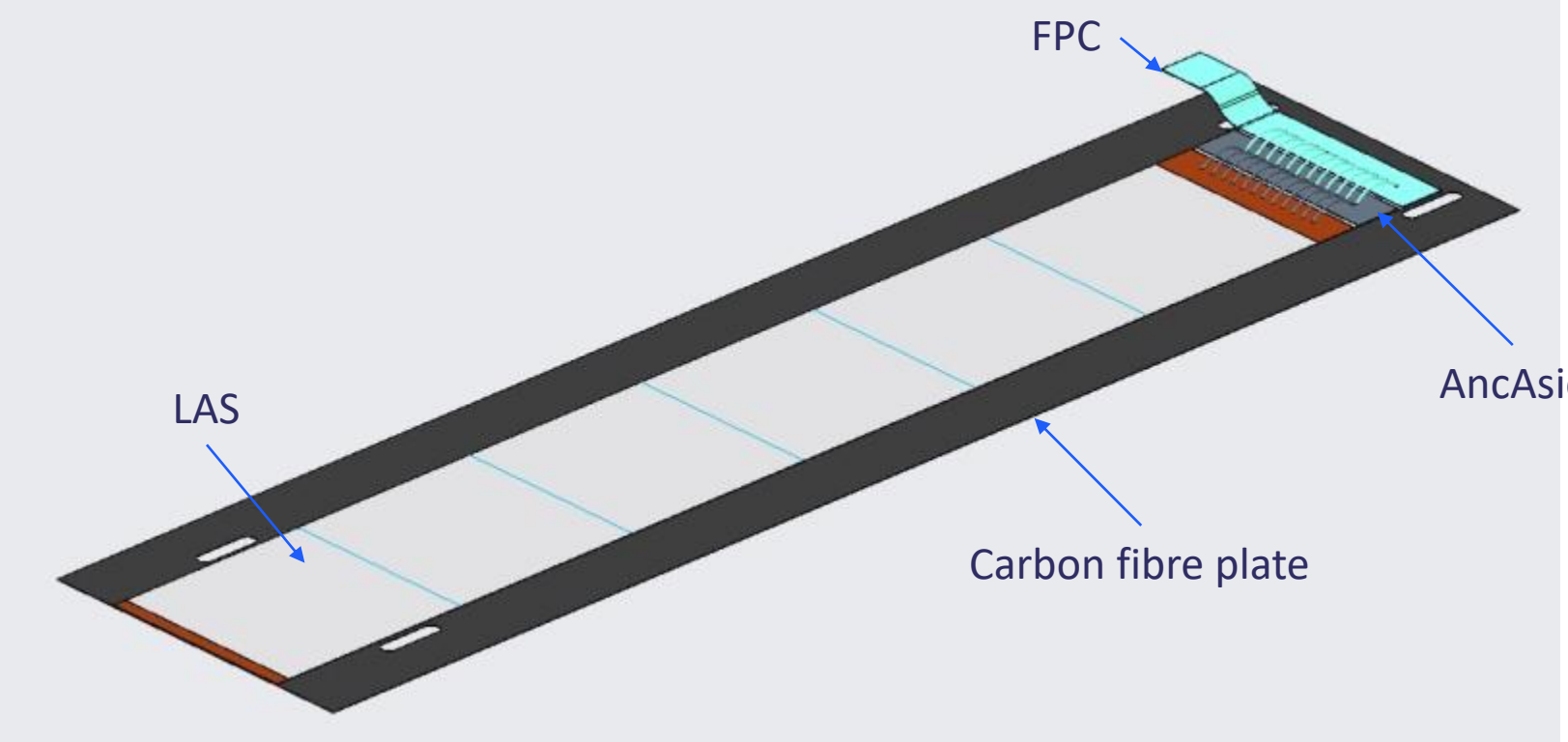
Detector module: endcaps



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ITP overview

Contents

- First version shared with reviewers on 21/11/2025.
- Discussions, investigations, changes.
- Latest release distributed on 05/12/2025 (only to LG).

Baselined items

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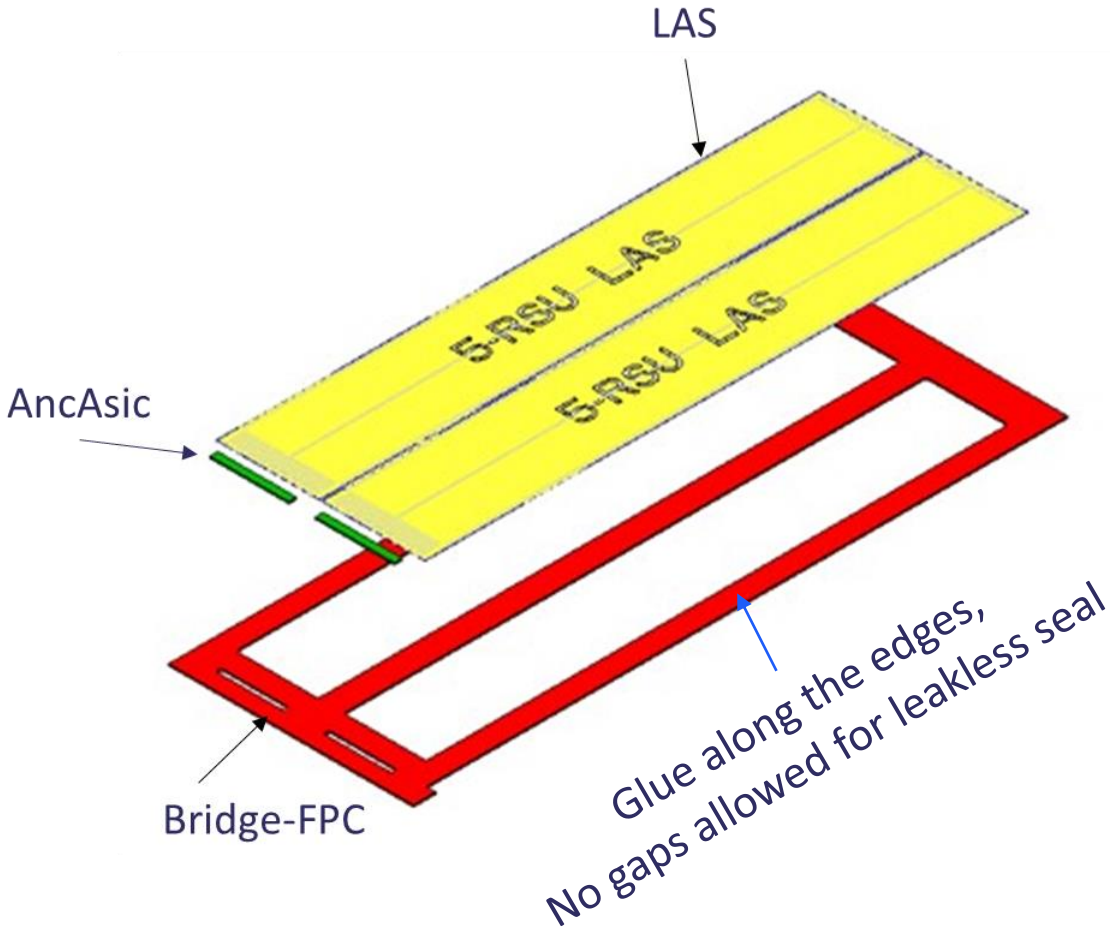
OB module: air tightness

- This is about uniformity of glue distribution along the edges of Si chips.
- Difficult and impractical test to do
  - To fix by design.
- Use “design for manufacturing principle” to remove the need of this test.
- To modify design to avoid this test:
  - Mods mainly affect FPC design



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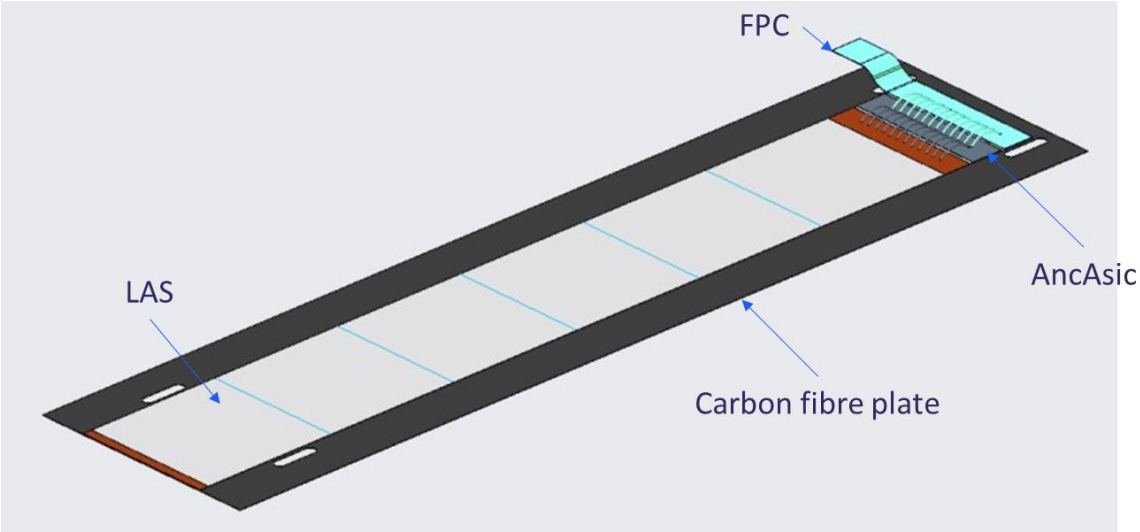
Disk module: carbon fibre plate (CFP)

- This is about avoiding shorts between carbon fibre support and LAS.
- Quality of manufacturing of CFP.
- Mitigation factors during module assembly, like epoxy selection and distribution (LAS CFP interface).



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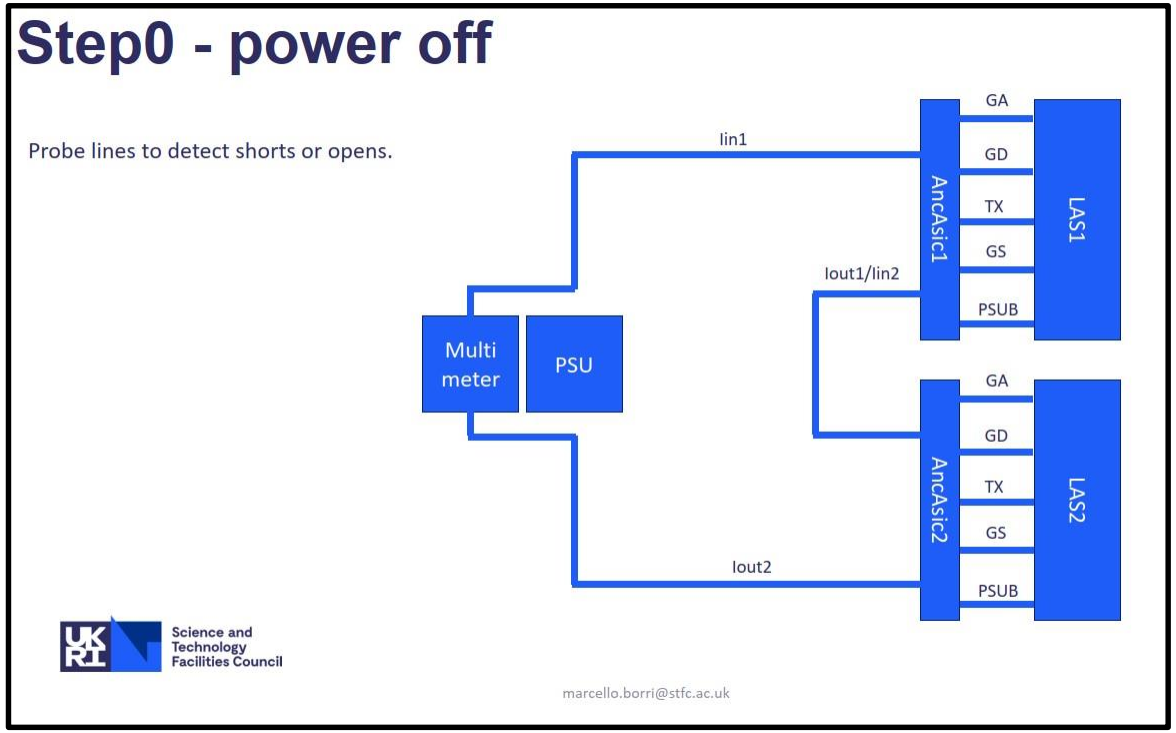
Powering tests on detector modules

Captured in dedicated presentation.



See my set of slides on powering tests

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Open points

Acceptance tests on LAS and AncAsic

Principle:
Need a reliable assessment of the chip quality before module assembly.

Criteria:
- Mechanical integrity [e.g. metrology on dimensions]
- Electrical integrity

How critical are the dimensions for us?
(A topic of its own?)

Current workflow:
- Wafers are probe tested at delivery from the foundry.
  [Assess processing yield from foundry]
- Post-processing: wafers are sent to thinning and dicing.
- Chips are sent to module assembly.

Post processing yield for 50um thin Si chips?
(yield of thinning to 50 um thick chips)

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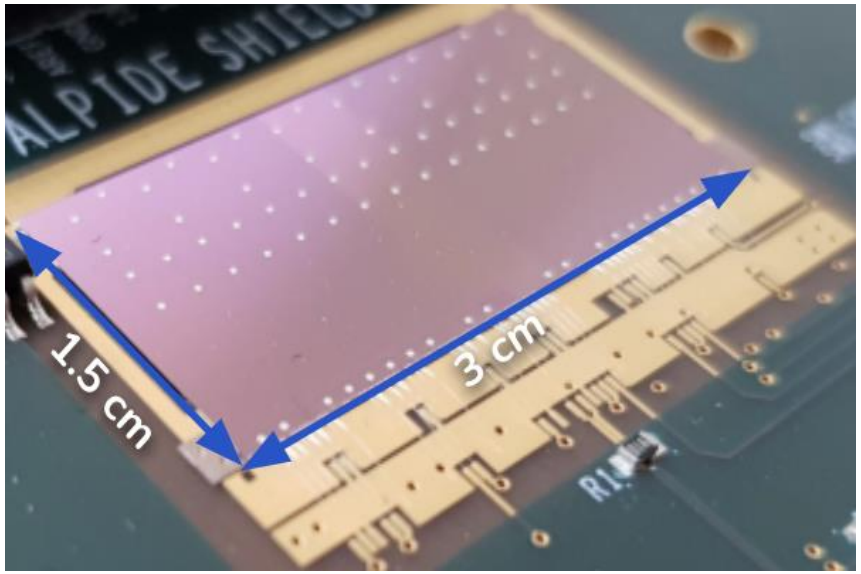
ALICE ITS2 – case study

+ spin-outs e.g. SPHENIX MVTX, R3B-TRT

See ALICE ITS2 TDR (page 46 "3.2 Thinning and dicing", page 48 "3.3 Single chip tests"): https://iopscience.iop.org/article/10.1088/0954-3899/41/8/087002/pdf

[…] The wafers will be post-processed, thinned and diced to obtain individual Pixel Chips. **Each chip will be tested and inspected prior to the assembly into larger modules.** […]
[Dimensional compliance is important for this detector].

[…] The exact yield factors for each of the processing steps (production, dicing, thinning, etc.) prior to the single chip tests are not yet known.[…]



ALPIDE yield (average)

sensors/wafer	46
gold [%]	30
silver [%]	30
bronze [%]	7.5
mech. grade [%]	32.5

Not considered suitable parts for detector grade modules

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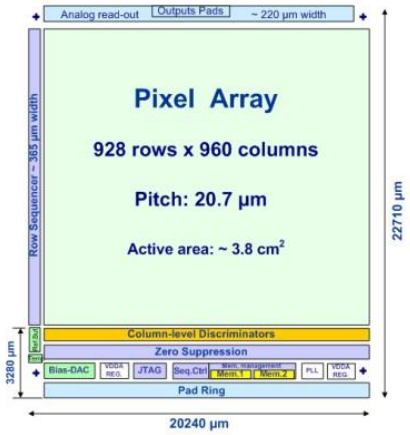
STAR PXL – case study

Do acceptance tests at module assembly sites?

See “The MAPS based PXL vertex detector for the STAR experiment”
“3 Detector production” page 3
https://iopscience.iop.org/article/10.1088/1748-0221/10/03/C03026/pdf

[…] **The 50µm thinned and diced sensors**, typically curved due to their reduced thickness, **are positioned on a custom made vacuum chuck and contacted through pins**, which are mounted on a dedicated electronics probe card and designed to deal with the uneven pad ring surface: **the sensor is tested for functional operation**, fully characterized in terms of noise and operating thresholds through built-in test functionalities and the readout is tested at full speed (160 MHz). **The yield of sensors within specifications ranged from 46% to 60% throughout the probe testing campaign** […]



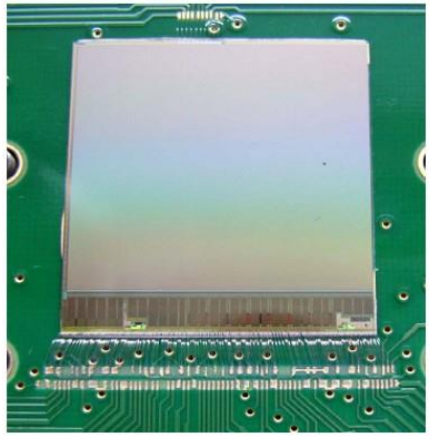


Figure 1. Functional block diagram of ULTIMATE (left) and Picture of the sensor on its PCB (right).

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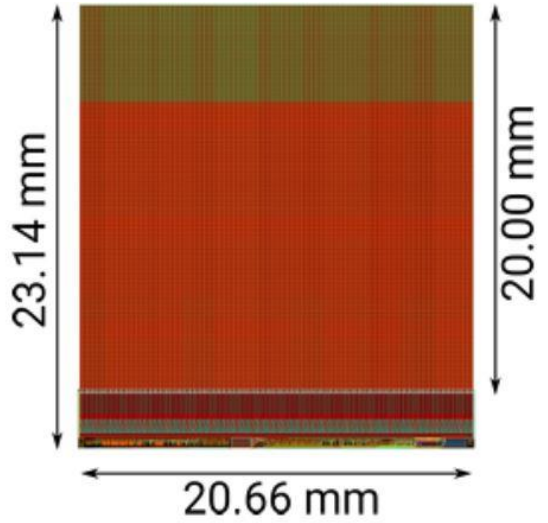
Mu3e – case study

See “Technical design of thephaseIMu3eexperiment”
“7.4. Pixel tracker construction and quality control” page19
https://www.sciencedirect.com/science/article/pii/S0168900221006641

[…] In case of the MuPix chips**, electrical testing** will take place on the wafer, and **on single die after dicing**, using appropriate probe cards […]



50um thin

Fig. 2. The MuPix10 layout: Active matrix at the top and periphery at the bottom. The color change in the active matrix is a feature of the routing scheme, see section 4.5

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CBM MVD – case study

See “The prototype of the Micro Vertex Detector of the CBM Experiment” “2.1. Sensor integration” https://www.sciencedirect.com/science/article/pii/S0168900213010504

2013

[…] The sensors were only visually inspected prior to assembling **[3]** but electrical tests were done only after bonding […]
[3] - Probe tests were not performed since probe cards had not been delivered in time.

[…] However, accounting for **a yield of 65% after sensors thinning** given by the sensor supplier, the assembly process was not observed to significantly further reduce this yield […]

2022

https://repository.gsi.de/record/246516

Information | References (0) | Citations (0) | Keywords | Usage statistics | Files | Plots | Holdings

Report GSI-2022-00549

Technical Design Report for the CBM: Micro Vertex Detector (MVD)

Klaus, P. (Editor) ; Koziel, M. (Editor) ; Michel, J. (Editor) ; Muentz, C. (Editor) ; Stroth, J. (Corresponding author) ; Deveaux, M.

2022
CBM Collaboration

CBM Collaboration 157 p. (2022)

Report No.: 1

Abstract: Approved Technical Design Report for the Micro Vertex Detector of the Compressed Baryonic Matter experiment at FAIR.

Note: BMBF ErUM-FSP-T06: C.B.M.@FAIRBilateral Contract GSI – Goethe University FrankfurtHIC for FAIRHelmholtz Forschungsakademie Hessen fuer FAIRIN2P3-IPHC Strasbourg

Restricted:

PDF

Acceptance tests on LAS and AncAsic?

- **Consistent approach in literature** on sensor probe testing after thinning and dicing.
- **SVT has a different approach** from the standard in our field, is it relaxing QC on parts?
- **Potential negative impact on detector module production** for SVT barrels and disks.

Is wafer thinning and dicing understood to the necessary level?

LAS areas will be ~5 or ~6 times grater than ALPIDE or Ultimate... potential for lower yield after thinning and dicing?

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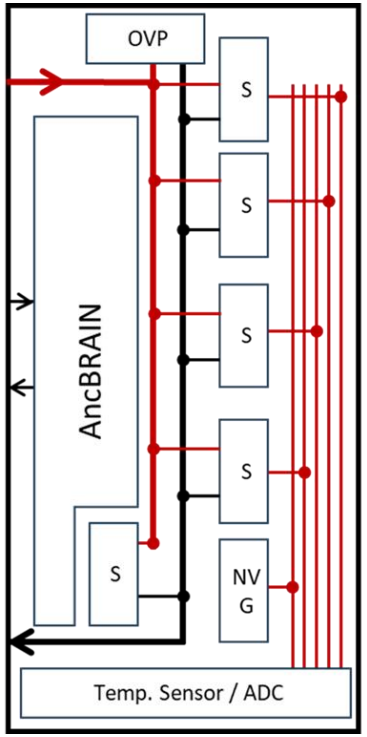
Grounding: AncAsic – LAS

Common gnd? Yes?
Or common analogue gnd
and common digital gnd? No?



GSVDD/GSVSS

GAVDD/GAVSS

GDVDD/GDVSS

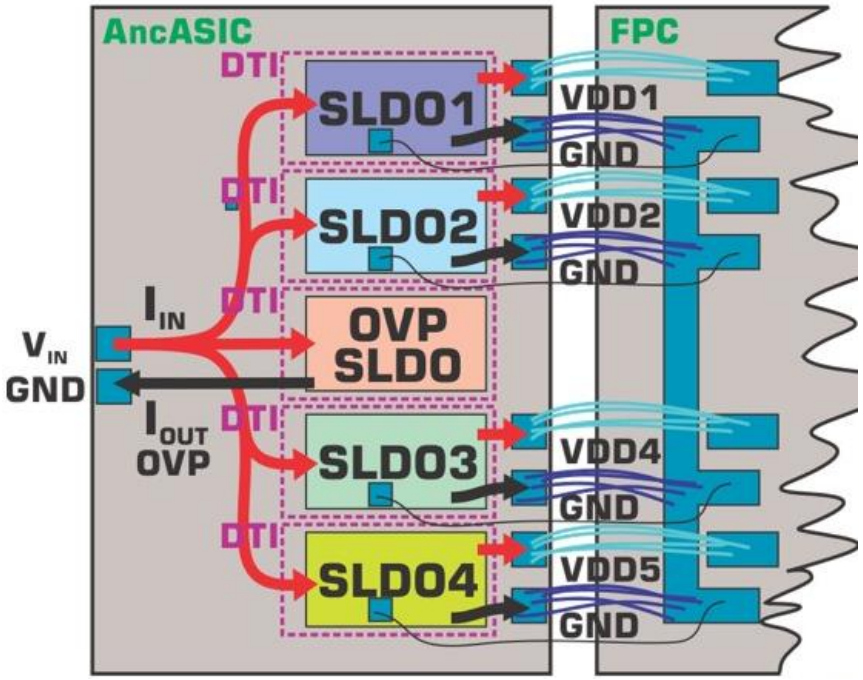
TXVDD/TXVSS

PSUB

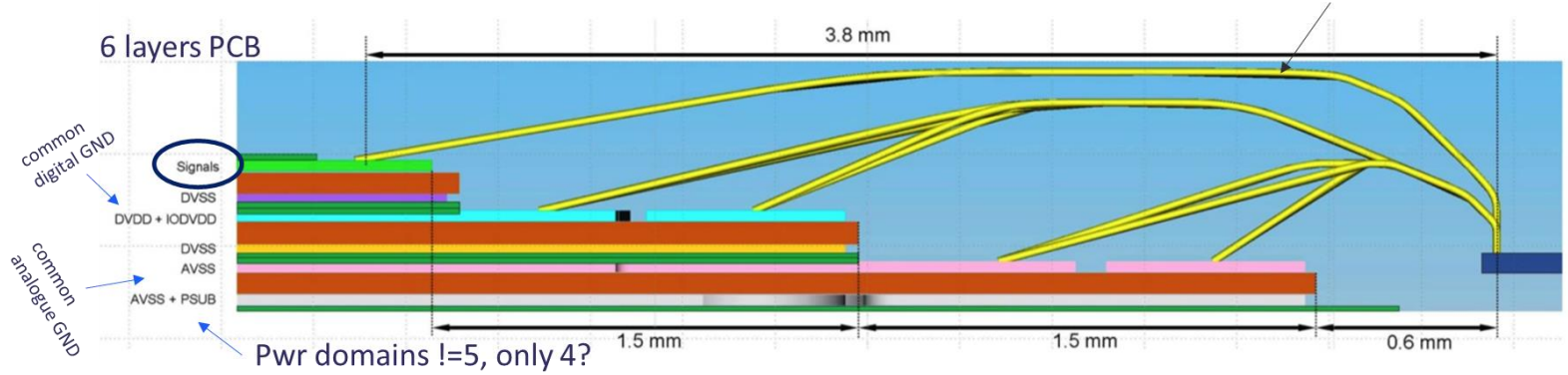
HS DATA

CTRL,CLK, ETC

G.Deptuch https://indico.bnl.gov/event/30317/



MOSAIX (From ITS3 TDR)



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Conclusion

- Latest release of ITP was edited following comments from reviewers: Laura, Nikki, Vallary, Iain.

- ITP and module benefitted from this exercise, which contributed to increase their maturity.

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Thank you

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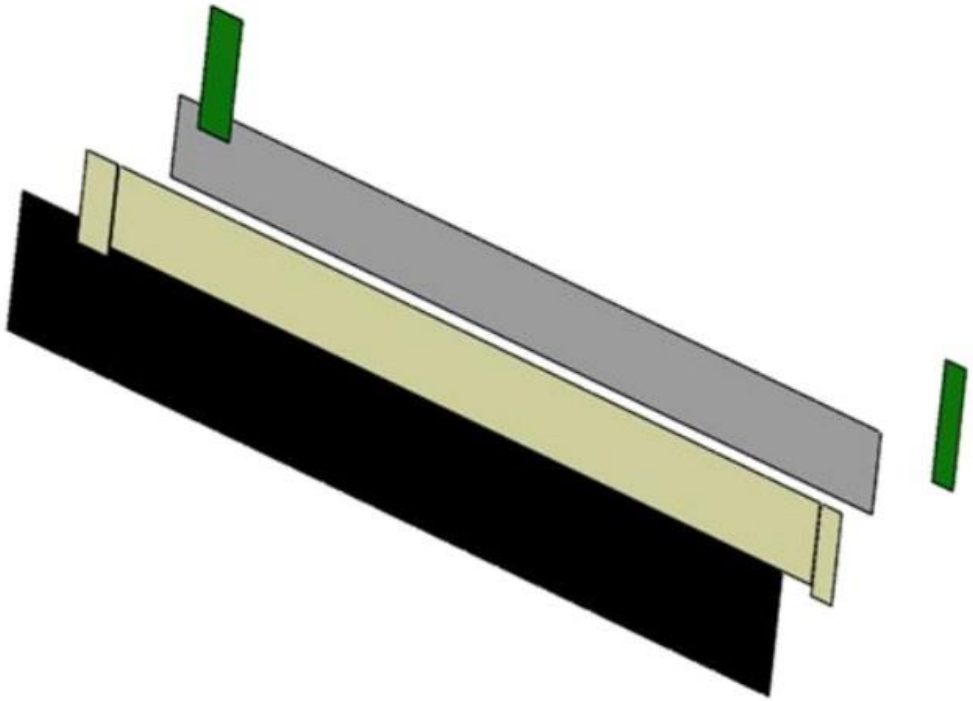
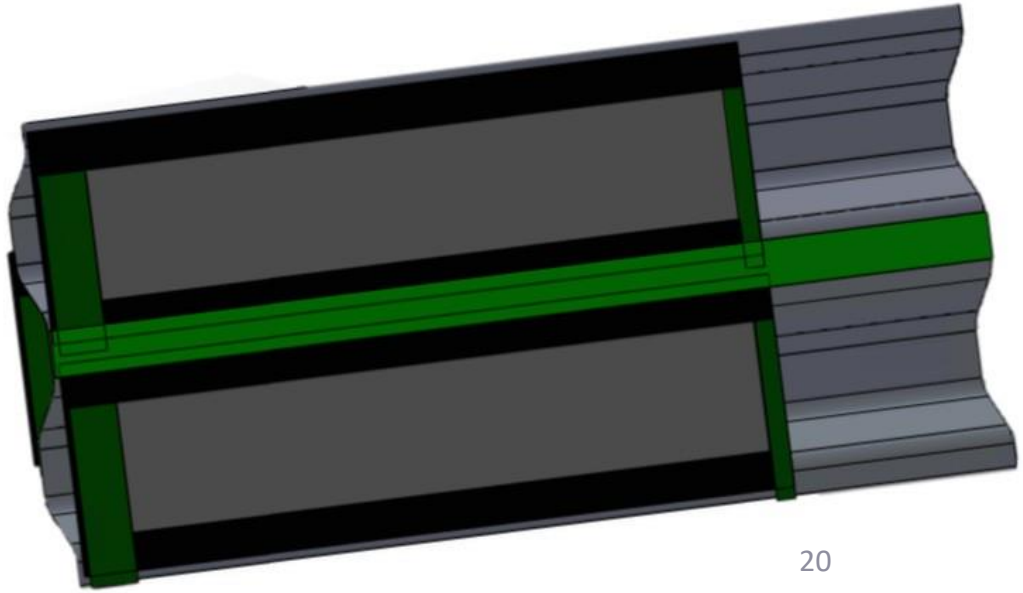
Detector module: endcaps





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