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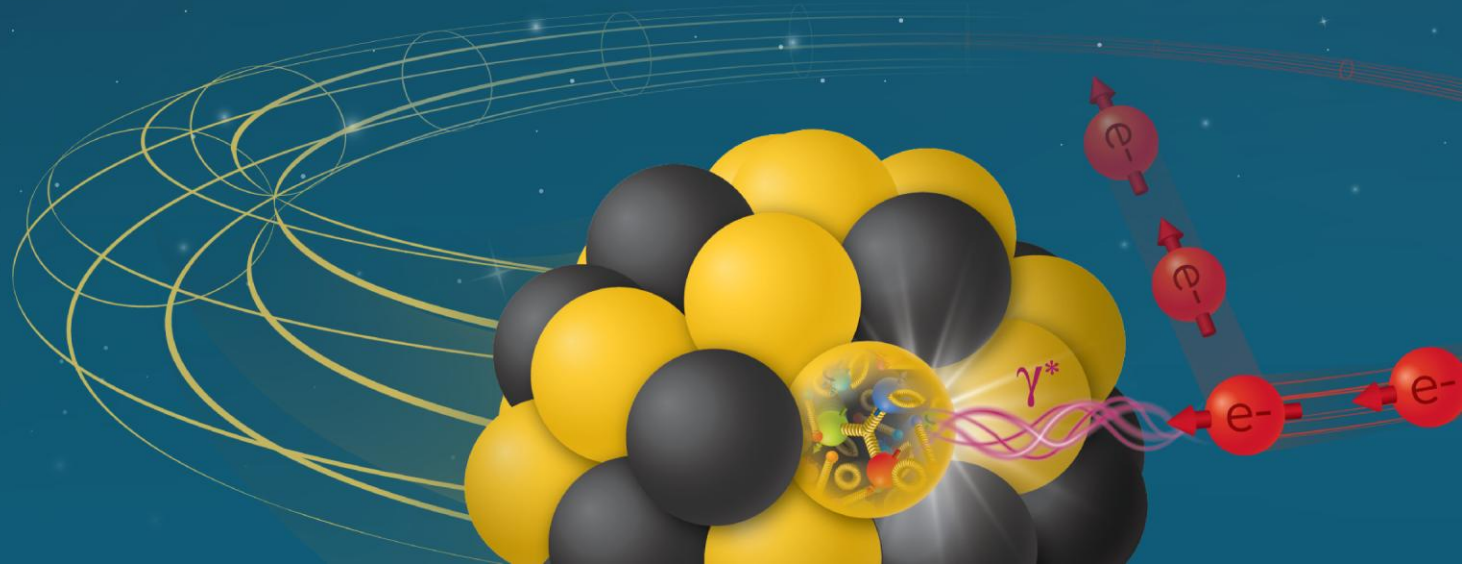
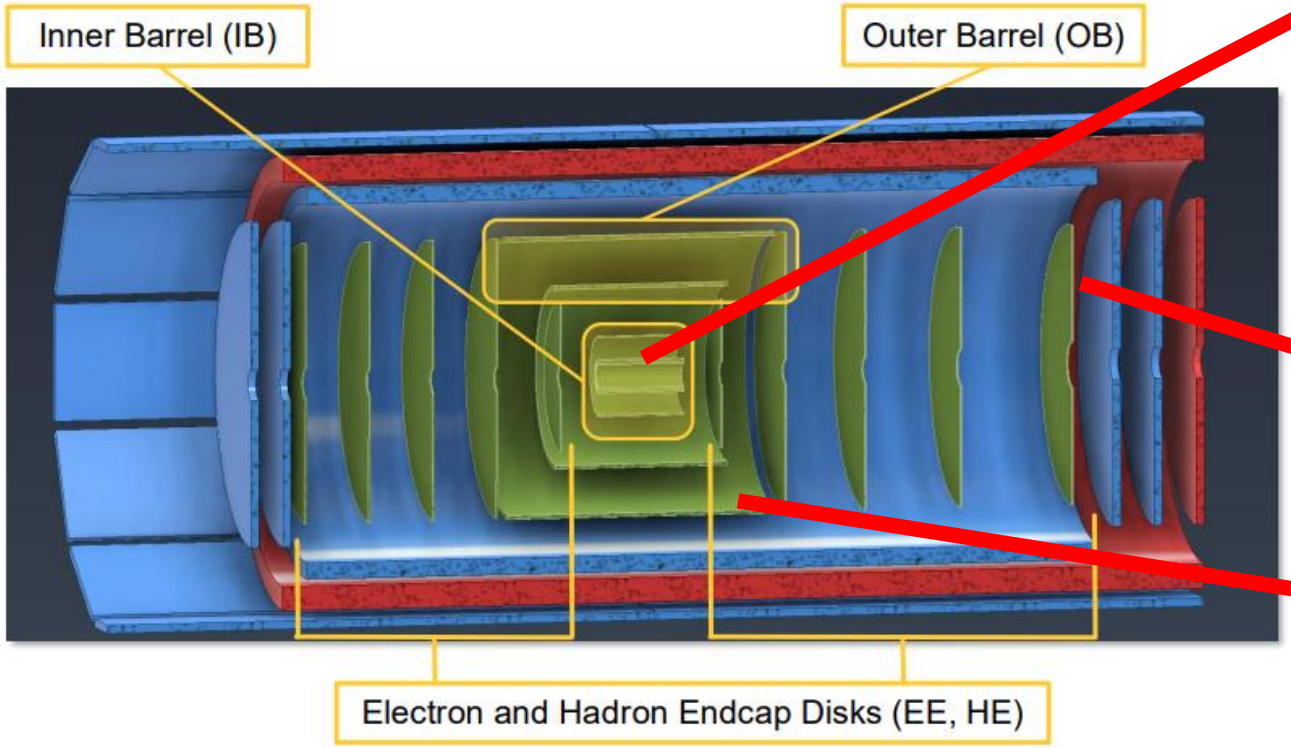
# Outer Barrel System




Electron-Ion Collider

# Introduction

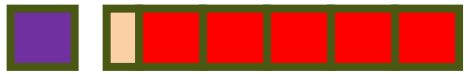
## SVT Silicon Scheme




### Inner Barrel

- Thinned silicon bent around beampipe
- Use wafer-scale MOSAIX from ITS3

### Outer Barrel and Discs



- Smaller Version of MOSAIX with minimum necessary changes (EIC-LAS)
- Supporting AncASIC

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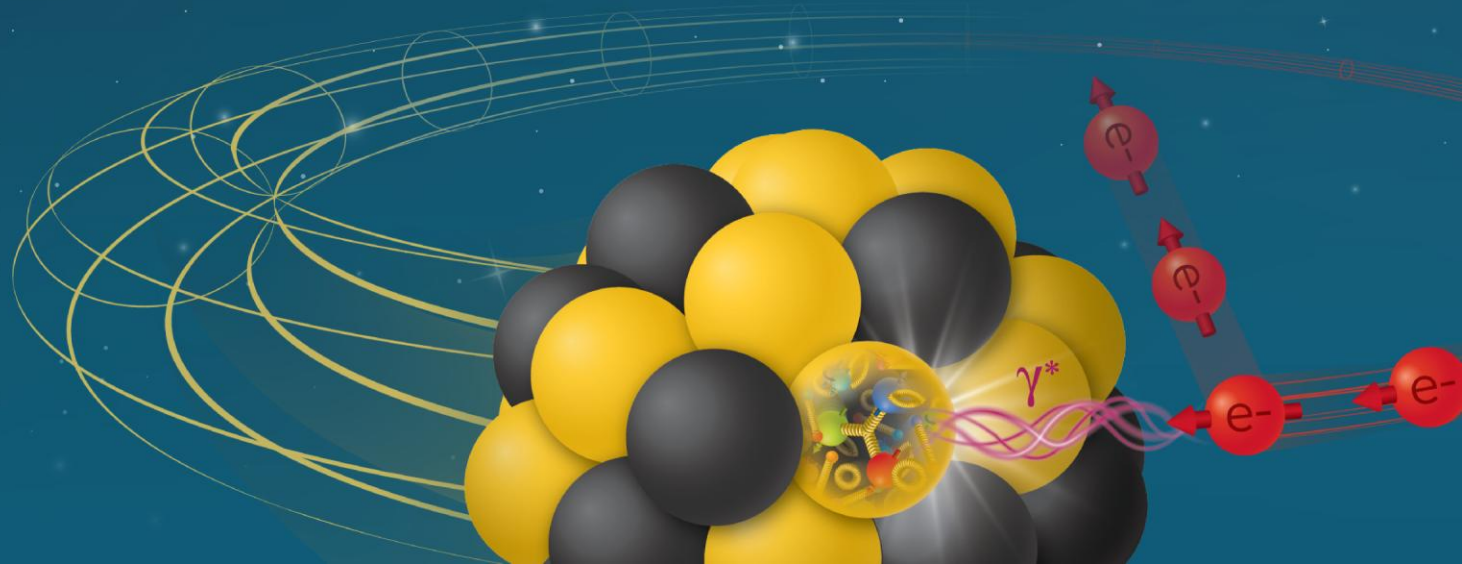
# AncASIC and LAS

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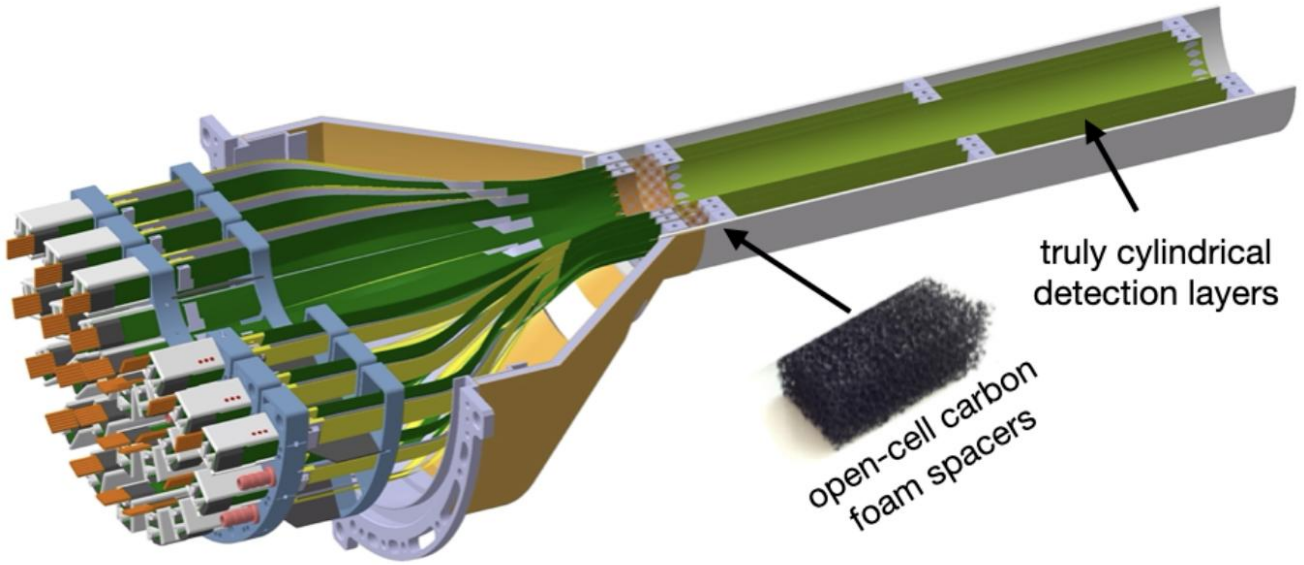
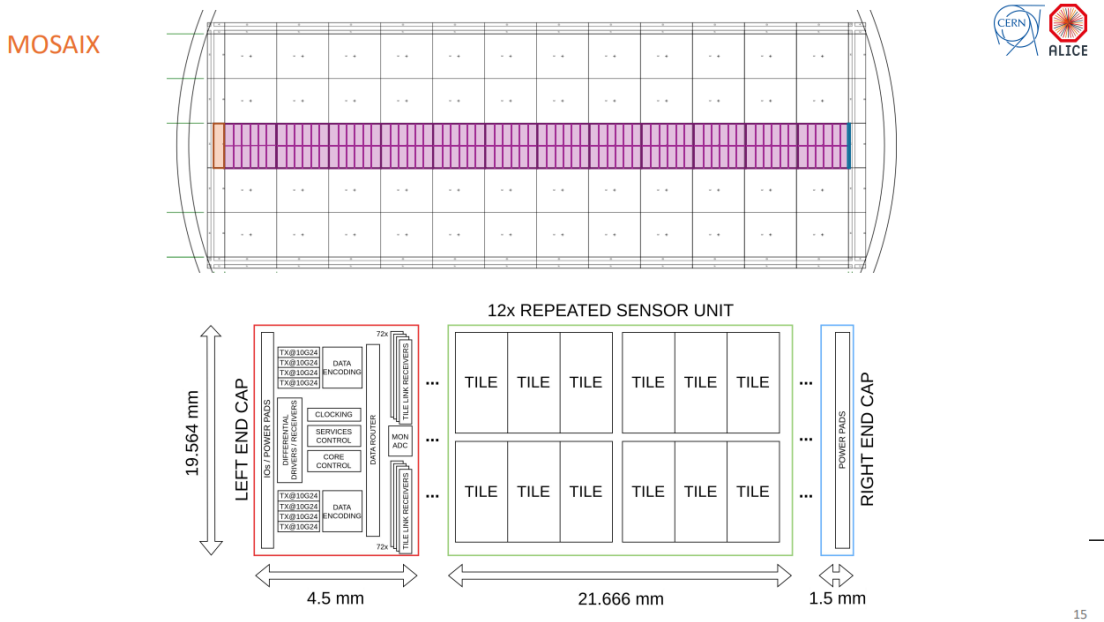
# Ancillary ASIC

## Why AncASIC?

- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control
  - Point-to-point powering
  - Precise negative back bias
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency
- For these reasons, develop supporting ASIC instead




https://ep-news.web.cern.ch/content/alice-its3-clears-major-milestone






https://indico.cern.ch/event/1381495/contributions/5988486/attachments/2869319/5164357/TWEPP2024.PVL.v11.pdf

# Ancillary ASIC

## Why AncASIC?

- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control → Serialised Slow Control interface from EIC-LAS to lpGBT
  - Point-to-point powering → SLDO for serial powering
  - Precise negative sensor bias → Local Negative Voltage Generator
- May be technically unfeasible to integrate these features in the LAS
- Limited prototyping
- MOSAIX schedule is an external dependency
- For these reasons, develop supporting ASIC instead

→ Develop independent supporting chip
- Development decoupled from MOSAIX availability
- No modification of MOSAIX needed
- 110nm XFAB process
- 4 MPW runs a year
- Cost effective

# Ancillary ASIC

## Why AncASIC?

- Some MOSAIX/LAS features require adaptation to stave/disc operation:
  - Point-to-point slow control
  - Point-to-point powering
  - Precise negative back bias
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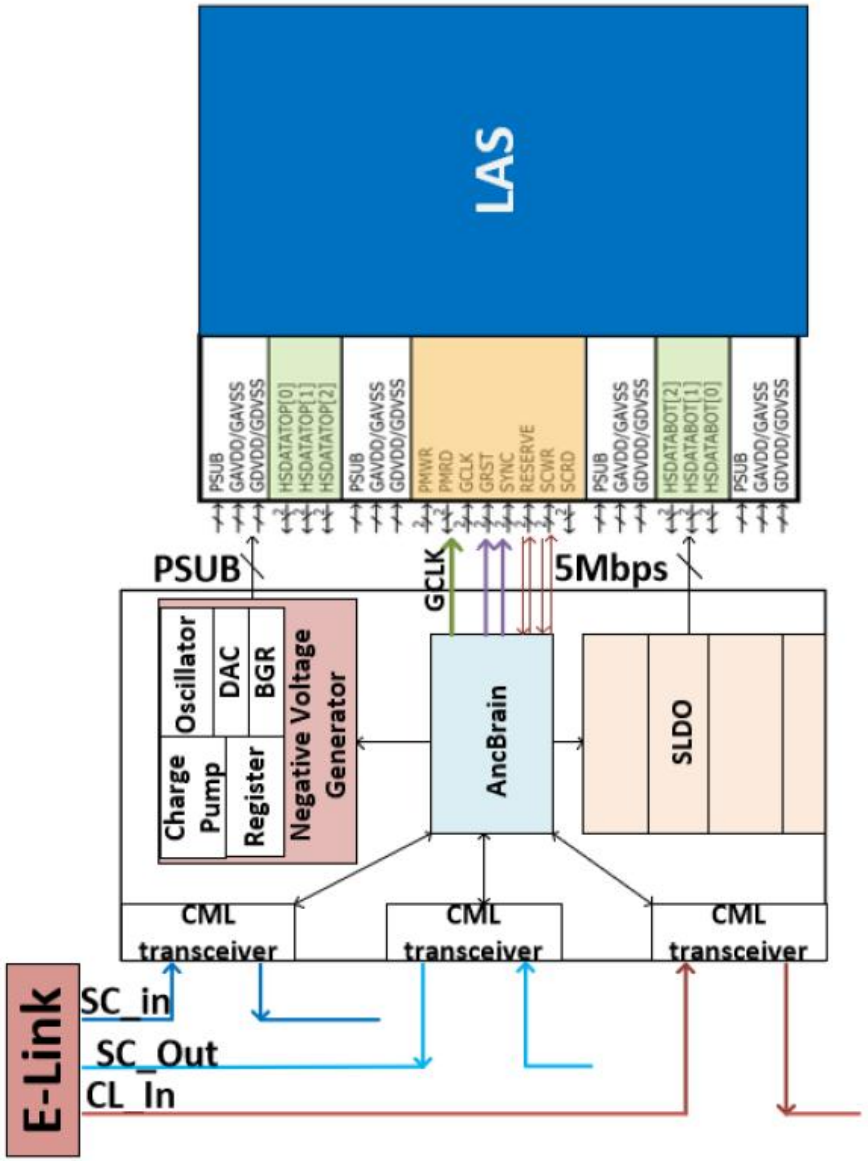
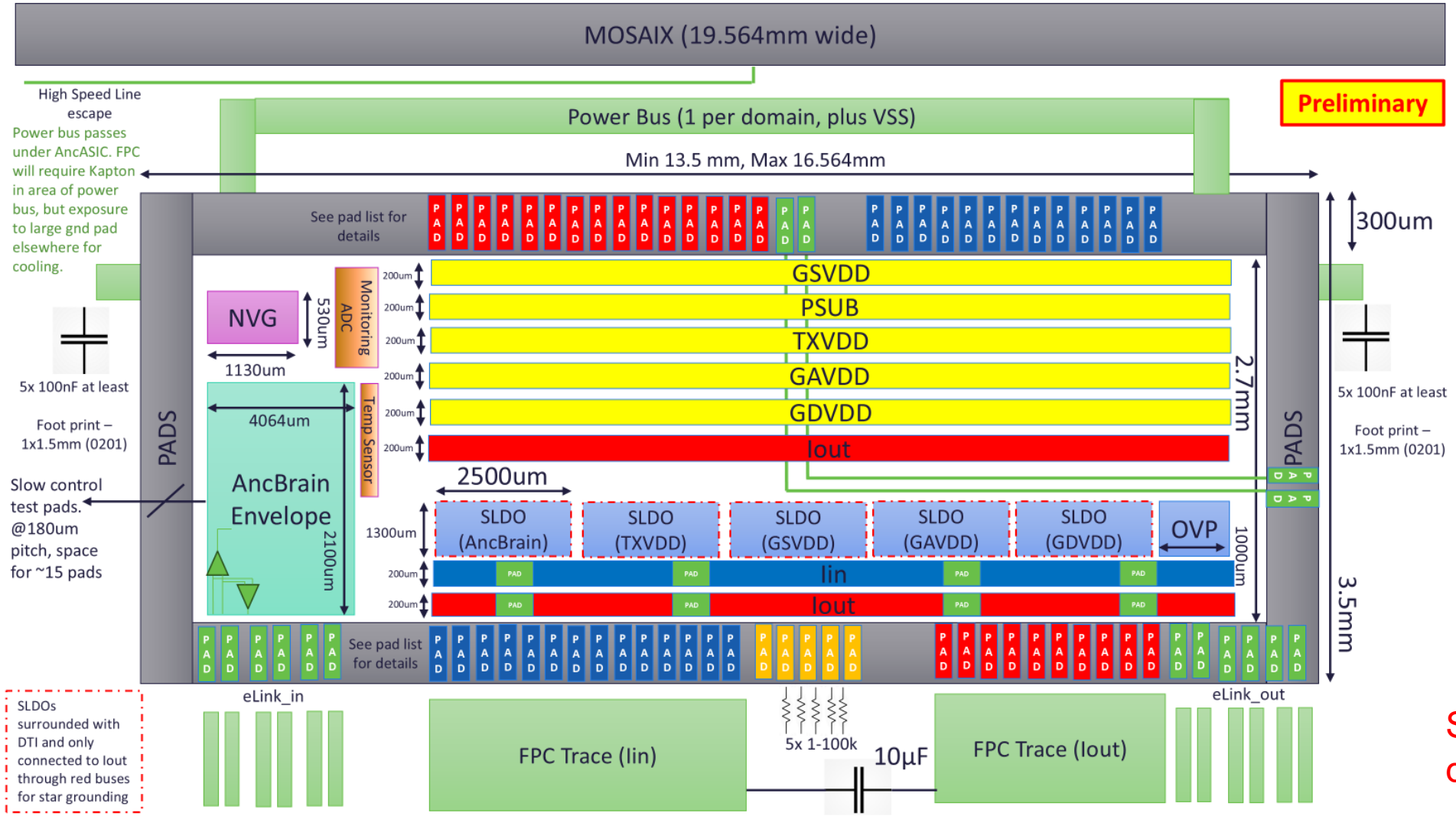


# AncASIC - Updated Plan




Still being developed…

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# FPC

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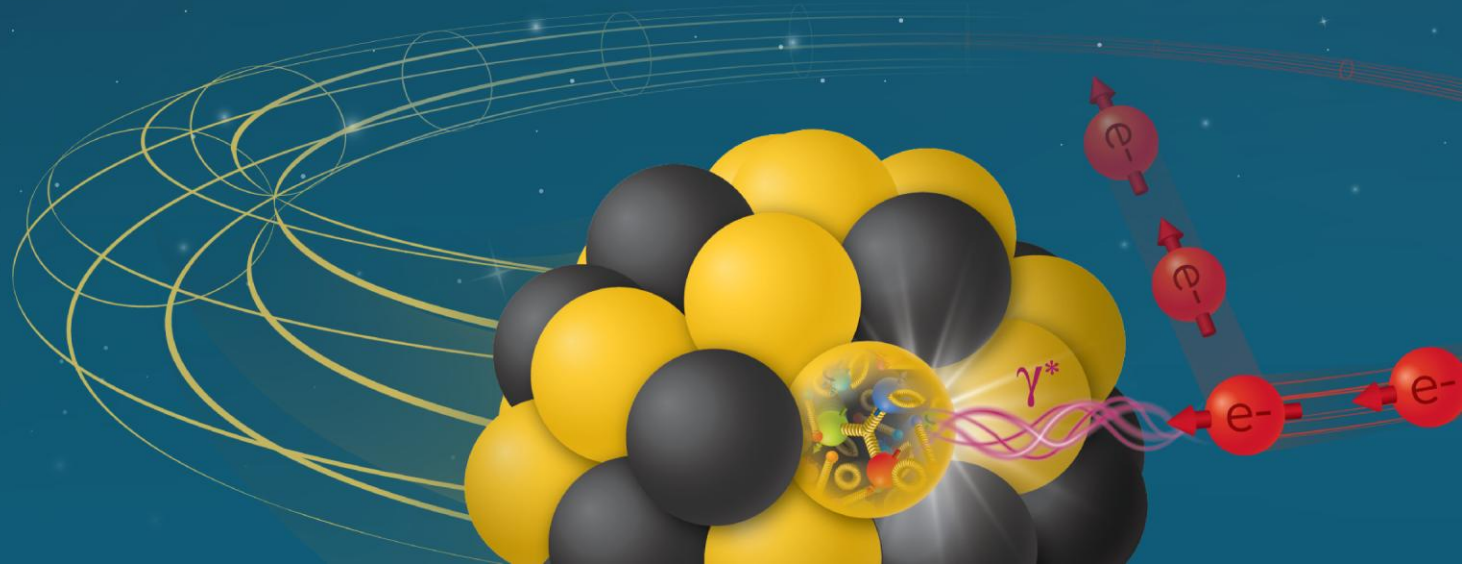
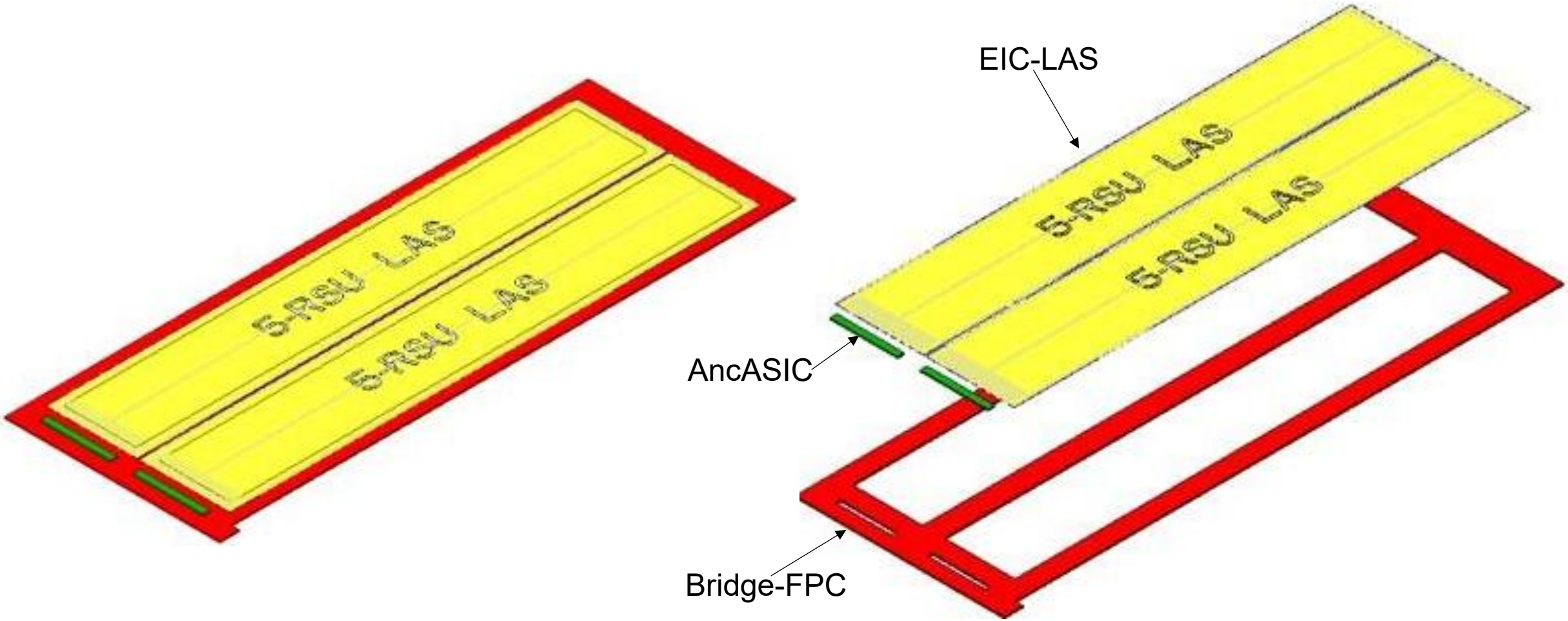


# OB Module on Bridge-FPC

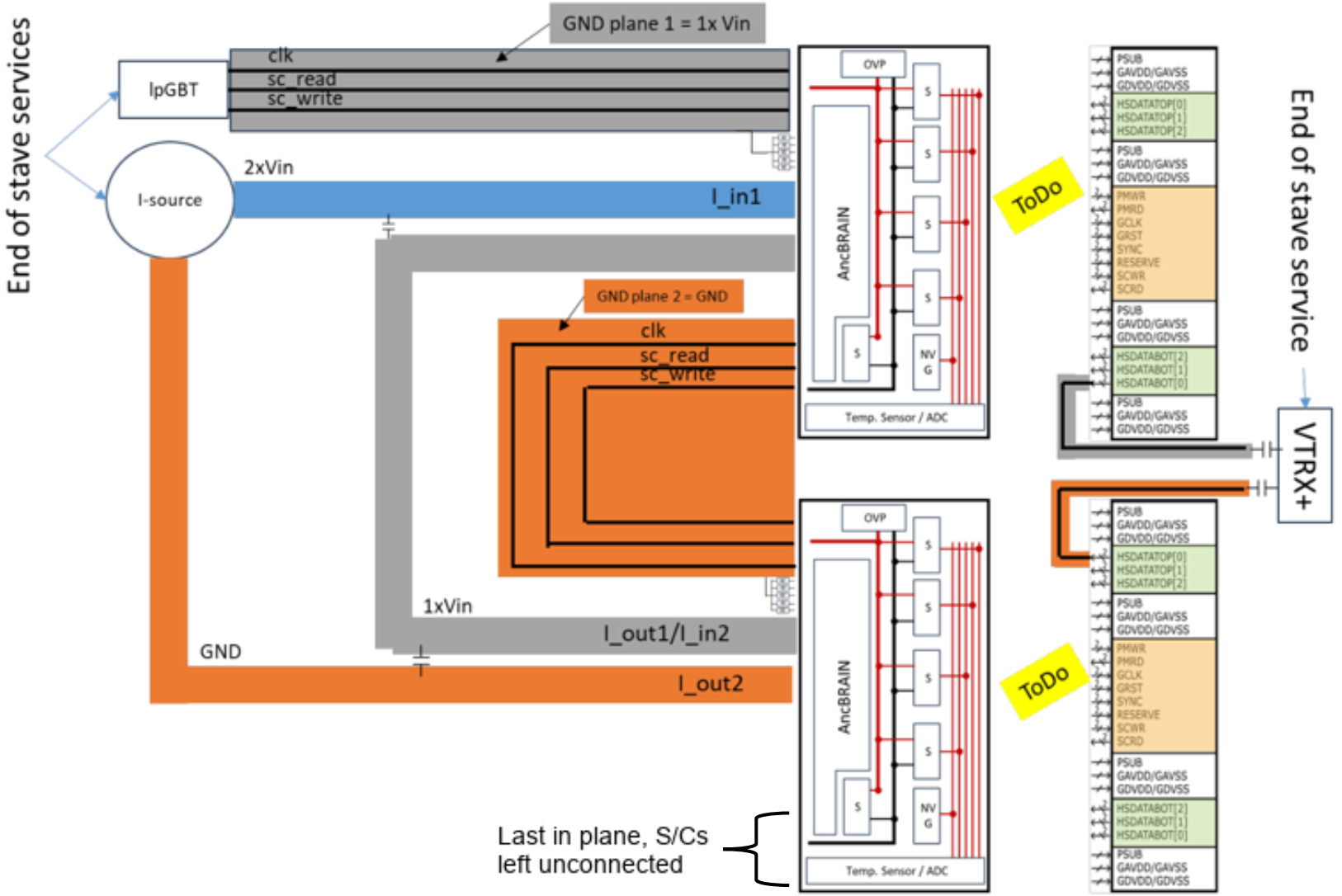


# OB Module Connections

Topological sketch

I_in = const

clk, sc_read, sc_write:
AC or DC coupled?

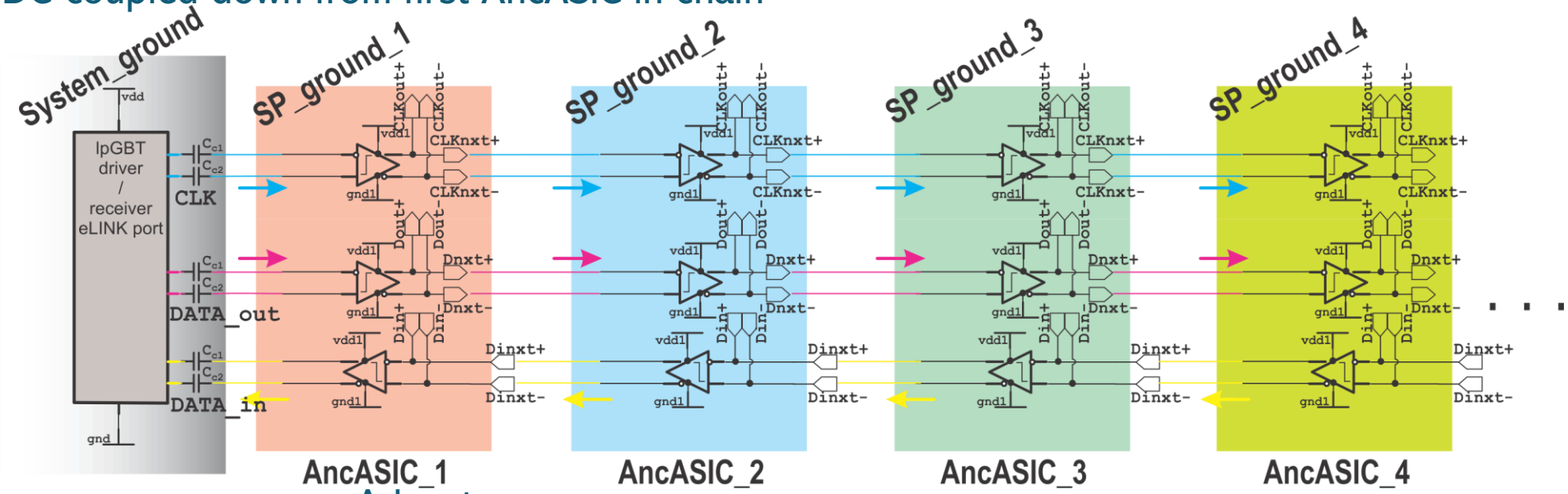


# From and To AncBrain

## Summary (ePortTX.pptx / ePortRx.pptx)

Main questions:

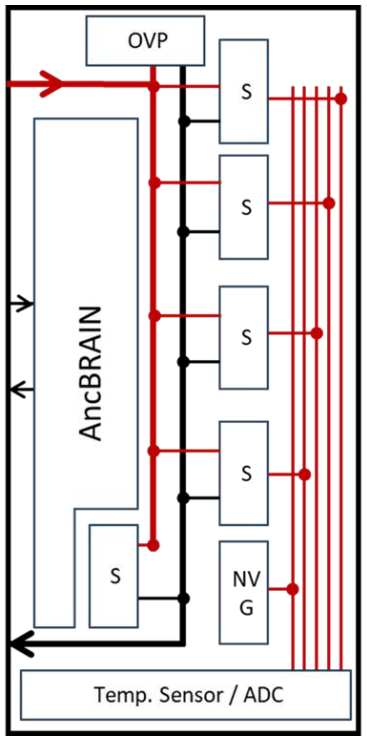
- (2) where AC and DC coupling should be used and how wired to EPort Group / eLinks ?
  - Proposal:
    - AC-coupled only to lpGBT (up-link and down-link), with coupling capacitors next to lpGBT
    - DC-coupled down from first AncASIC in chain




Advantages:

- Best for long chain of AncASICs,
- All but first AncASIC can entirely stop transmission

# Grounding: AncAsic – LAS




GSVDD/GSVSS

GAVDD/GAVSS

GDVDD/GDVSS

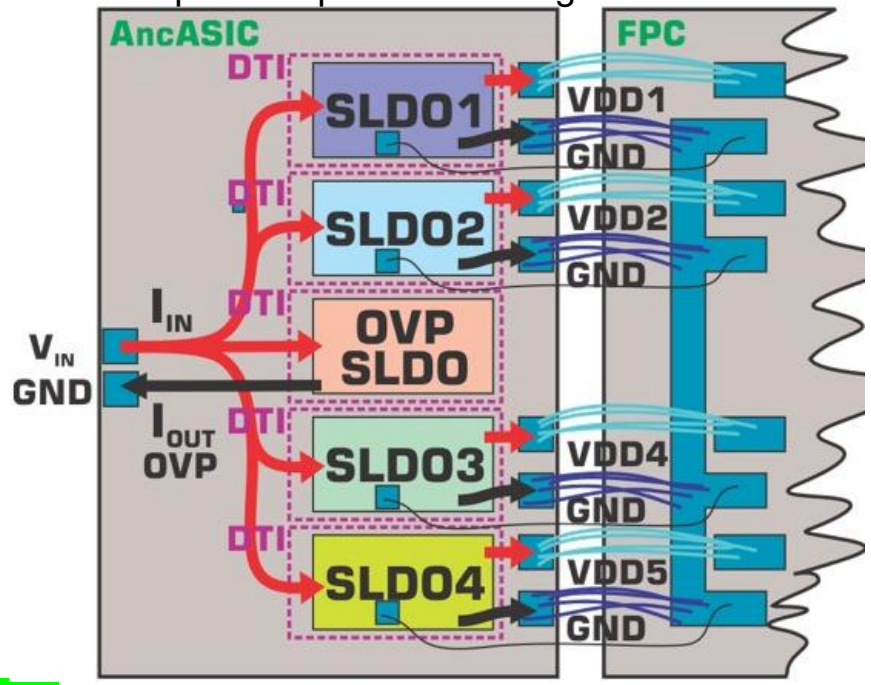
TXVDD/TXVSS

PSUB

HS DATA

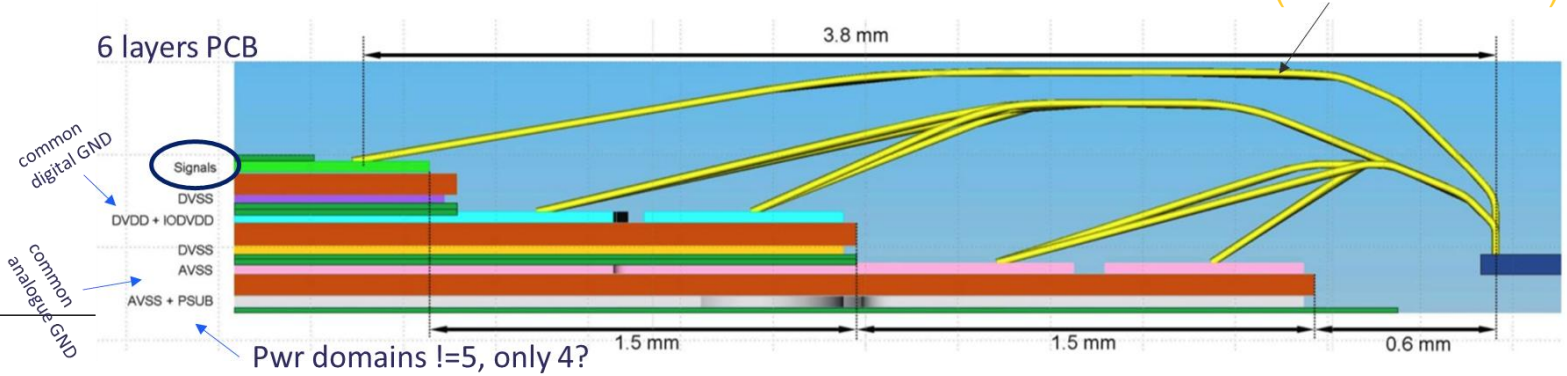
CTRL,CLK, ETC

G.Deptuch https://indico.bnl.gov/event/30317/




Common gnd? Yes?
Or common analogue gnd
and common digital gnd? No?

MOSAIX (From ITS3 TDR)



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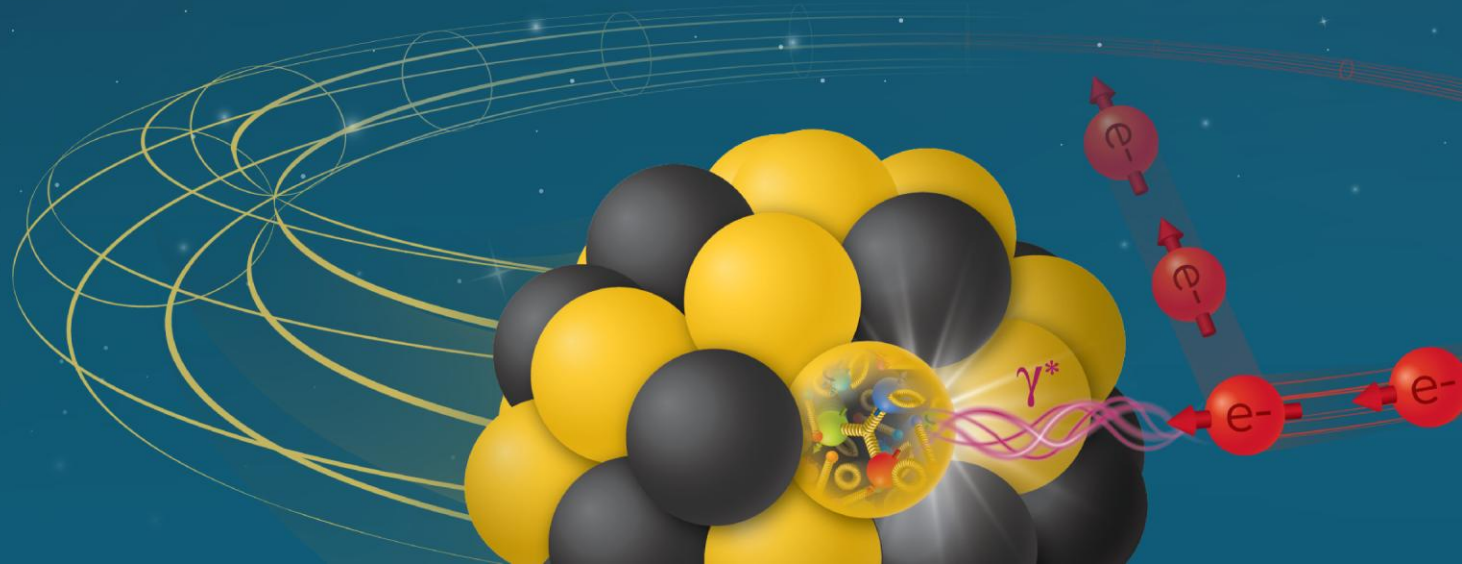
# Beyond the FPC…

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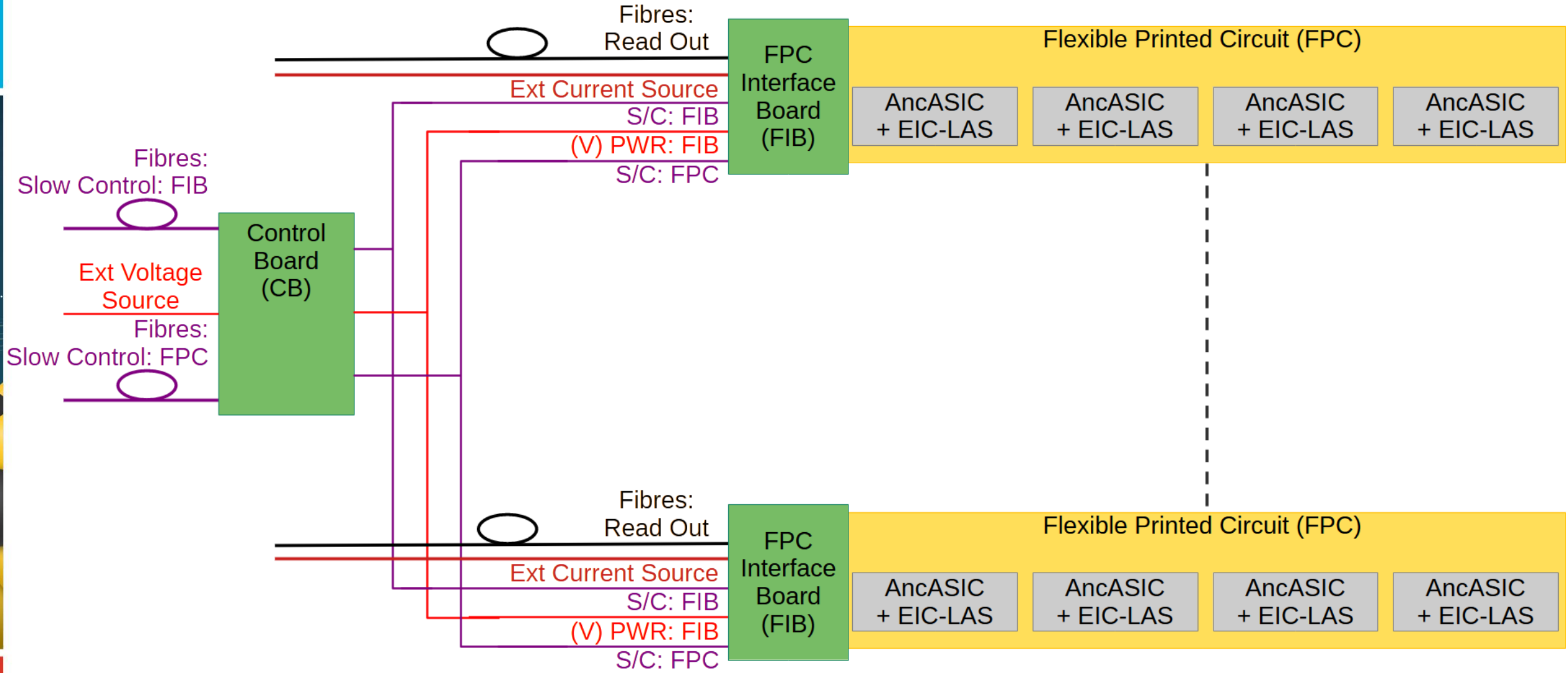
# Basic OB/Disk architecture



# Beyond the CB and FIBs

- All connections exiting the SVT volume go via a patch panel (PP).
  - e-side and h-side PP used on all staves.
- From the PPs:
  - FIB power connects to current sources (1 channel per L3 FIB, 2 channels per L4 FIB).
  - FIB fibres (HS data) connect to a data aggregator board. Prior to being received at the control room.
  - CB power connects to voltage sources (1+ CB per channel).
  - CB fibres (S/Cs) connect to an aggregator board.