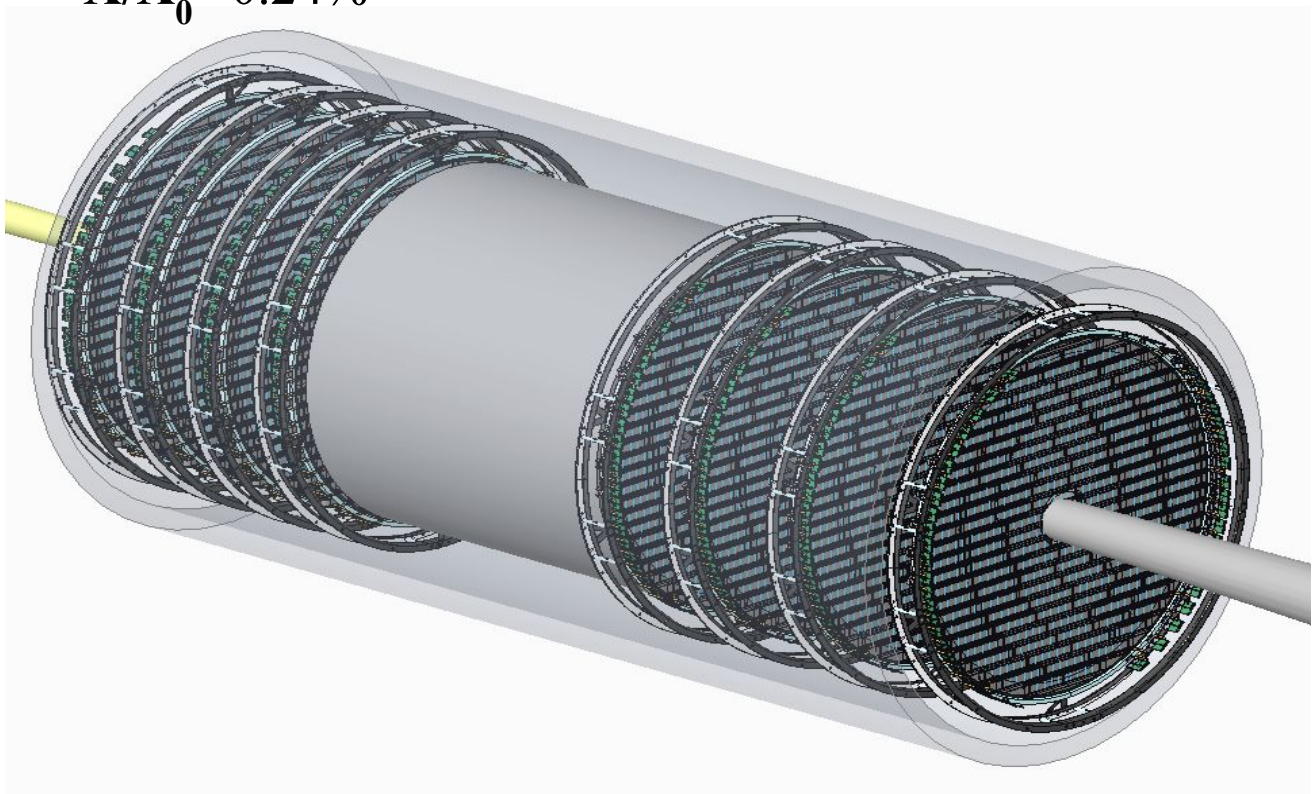
ePIC SVT Disk Architecture

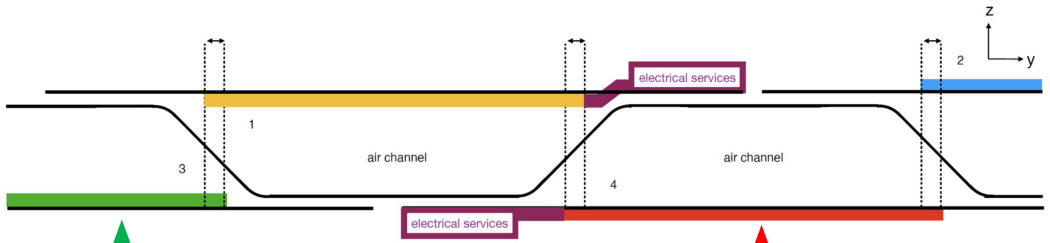
Nicole Apadula, Elaine Buron, Ernst Sichtermann,
Joe Silber, Zhenyu Ye

Lawrence Berkeley National Laboratory

ePIC SVT Disks

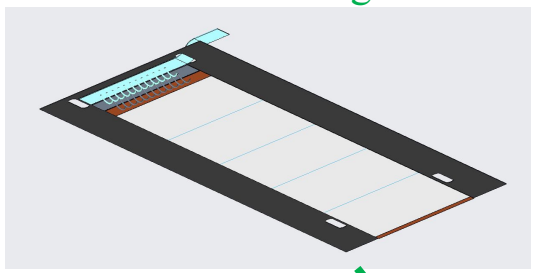
- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **X/X_0** ~0.24%

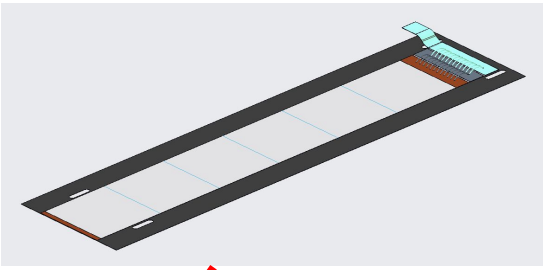


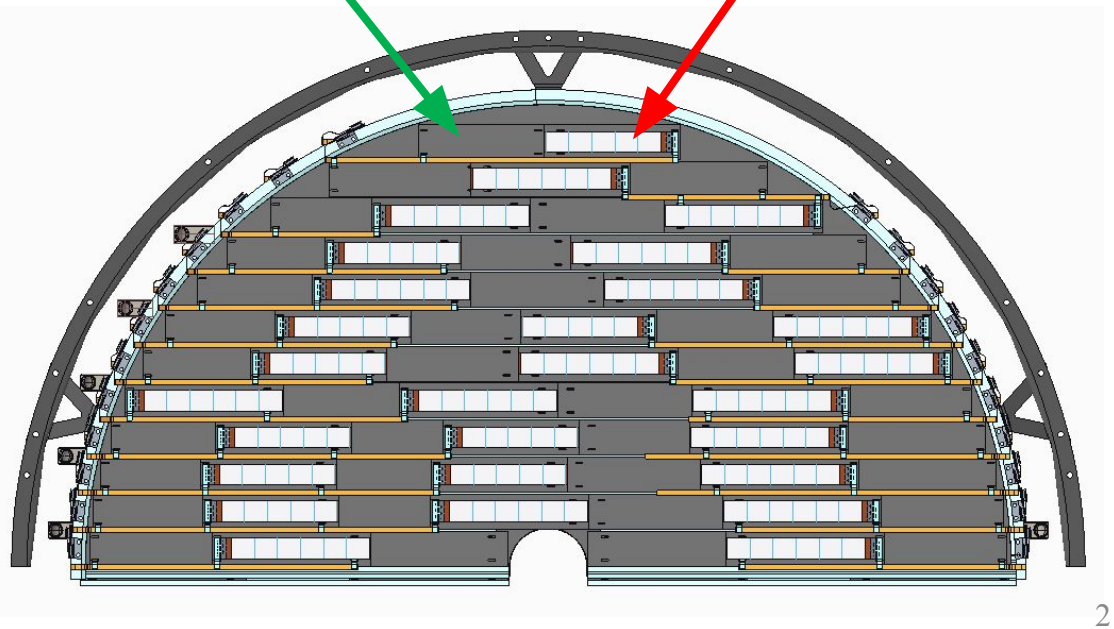


Sensor Inward Facing Module

Sensor Outward Facing Module



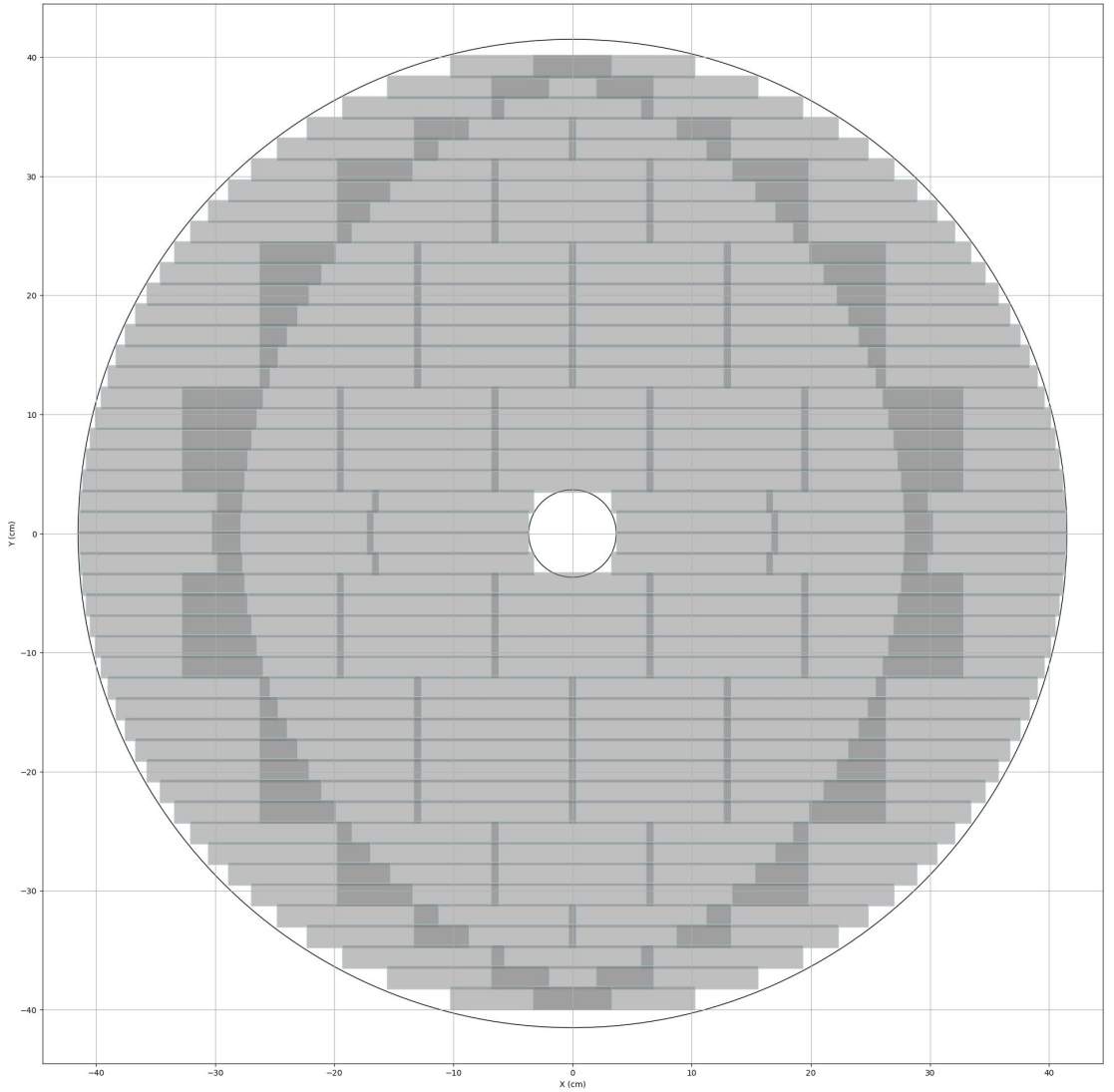




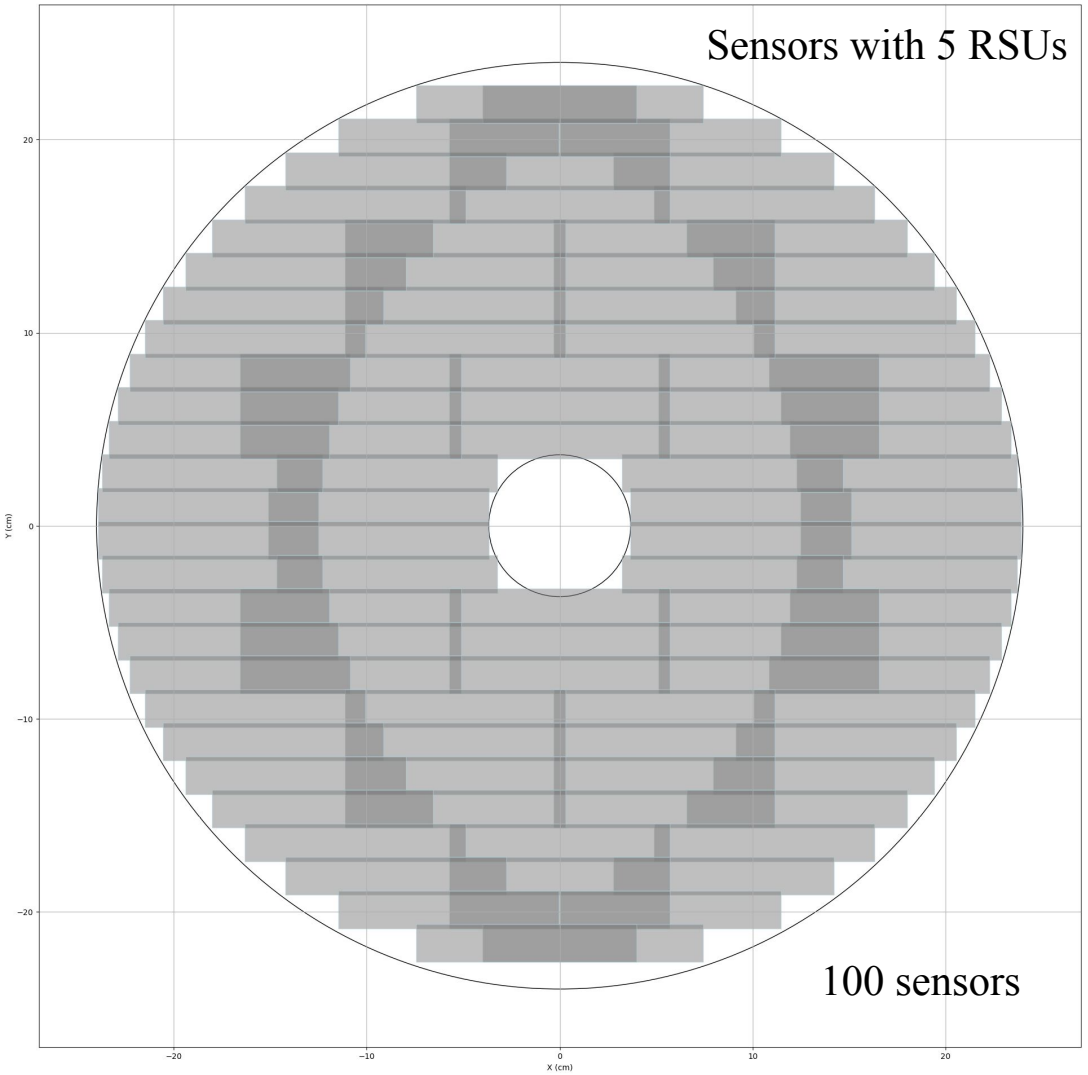
ePIC SVT Disks

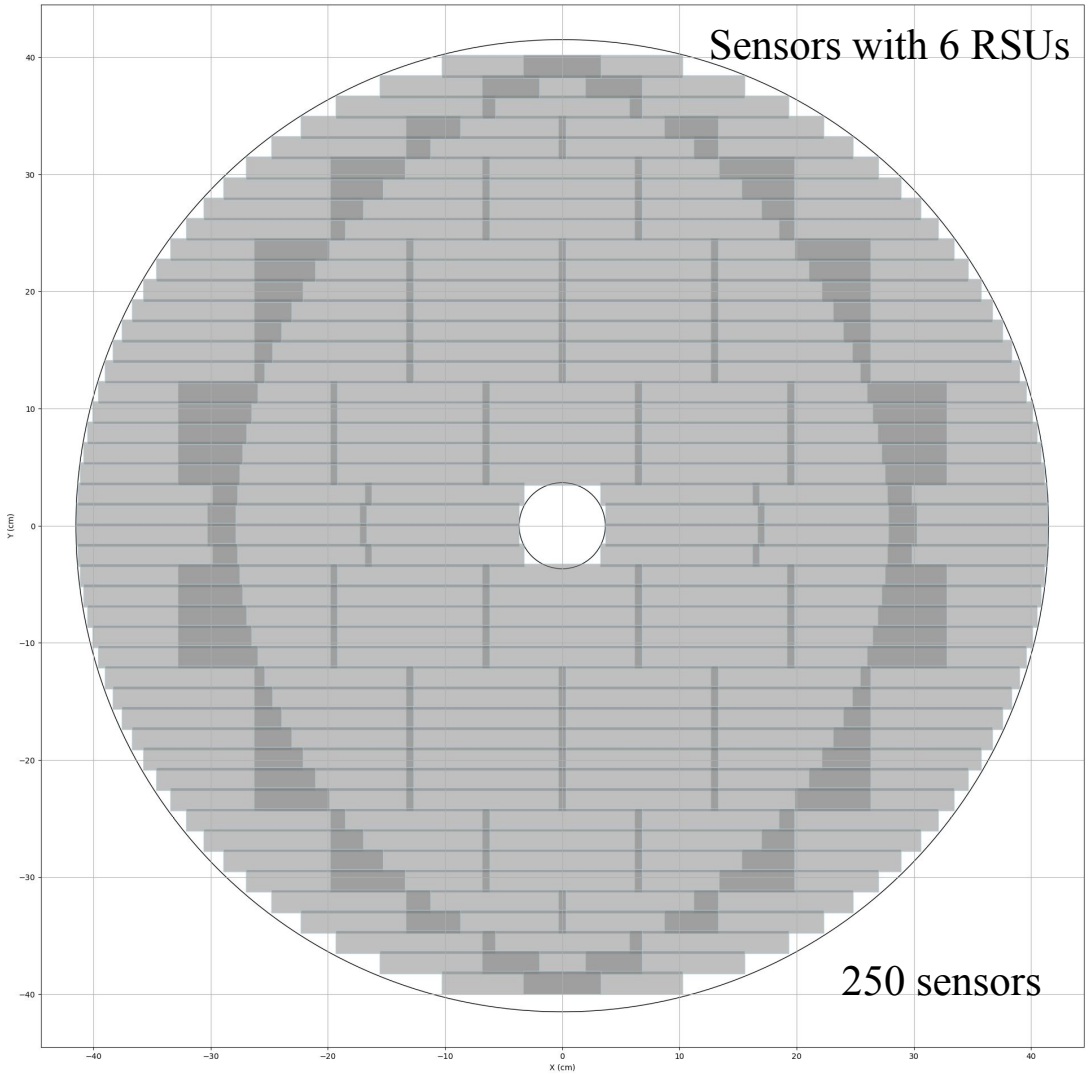
Sensor placement strategy for disks: minimum overlap in the inner region, maximum in the outer region; symmetric in x if possible; LEC at larger radius than REC.

- For rows covered by the beam pipe, start filling the first sensor at $x=\sqrt{(R_{in}^2-y^2)}$, so that the edge of the sensor is the closest possible to the beam pipe.
- Place the other sensors with an overlap of 6 mm to the previous one to avoid gaps covered by active sensor areas.
- Stop when the last sensor would be outside of the disk. Place the last sensor at $x=\sqrt{[R_{out}^2-(y+\text{sensor height})^2]}$-sensor length, so that the edge of the sensor is at the outer radius of the disk.
- The sensors at the edge of the disks will connect via an edge FPC to the corresponding FPC interface board (FIB). The other sensors will connect via bridge and main FPCs to the FIB (see page 10&11).
- The length of the main FPC may need to vary depending on y.



ePIC SVT Disks - ED0/HD0, ED1/HD1

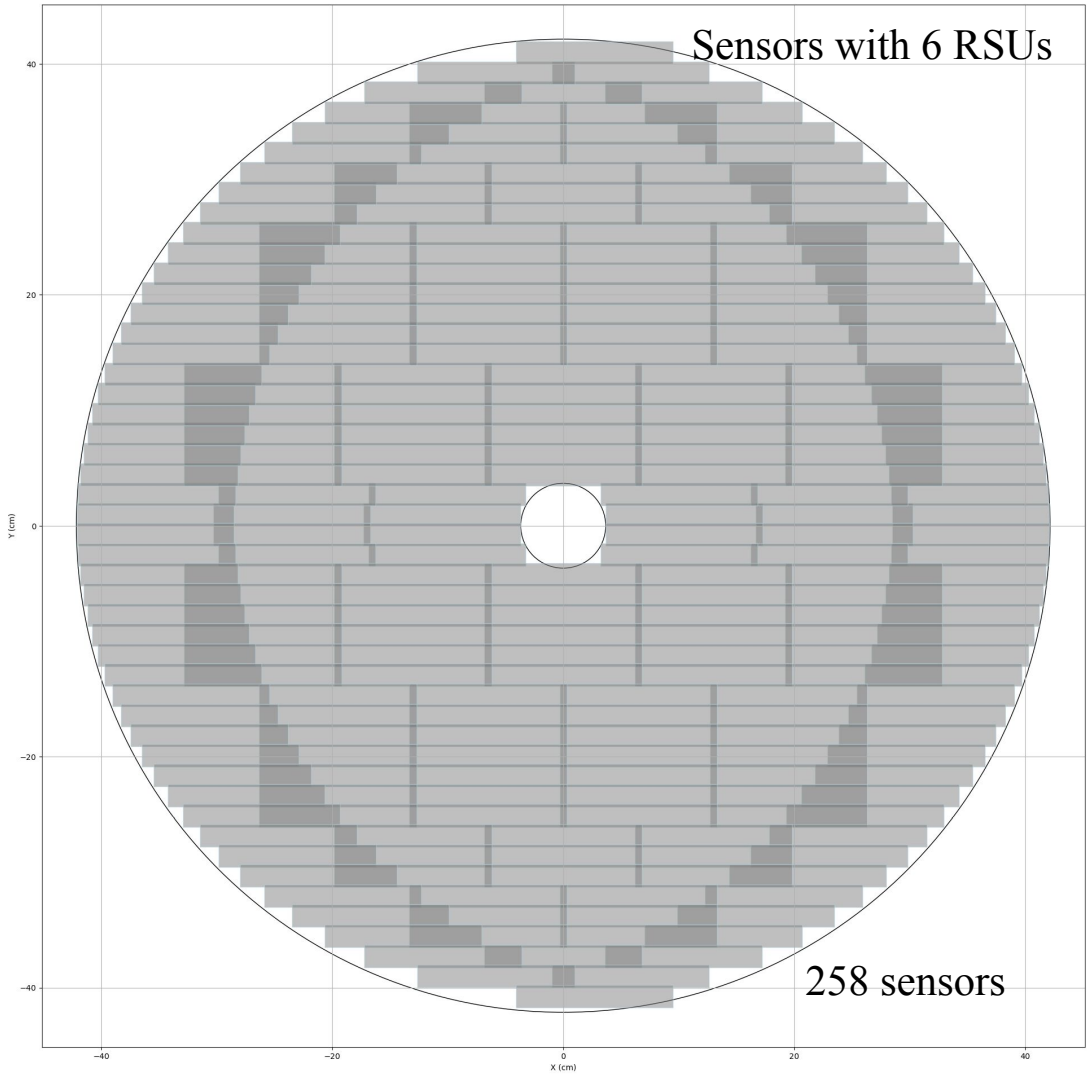




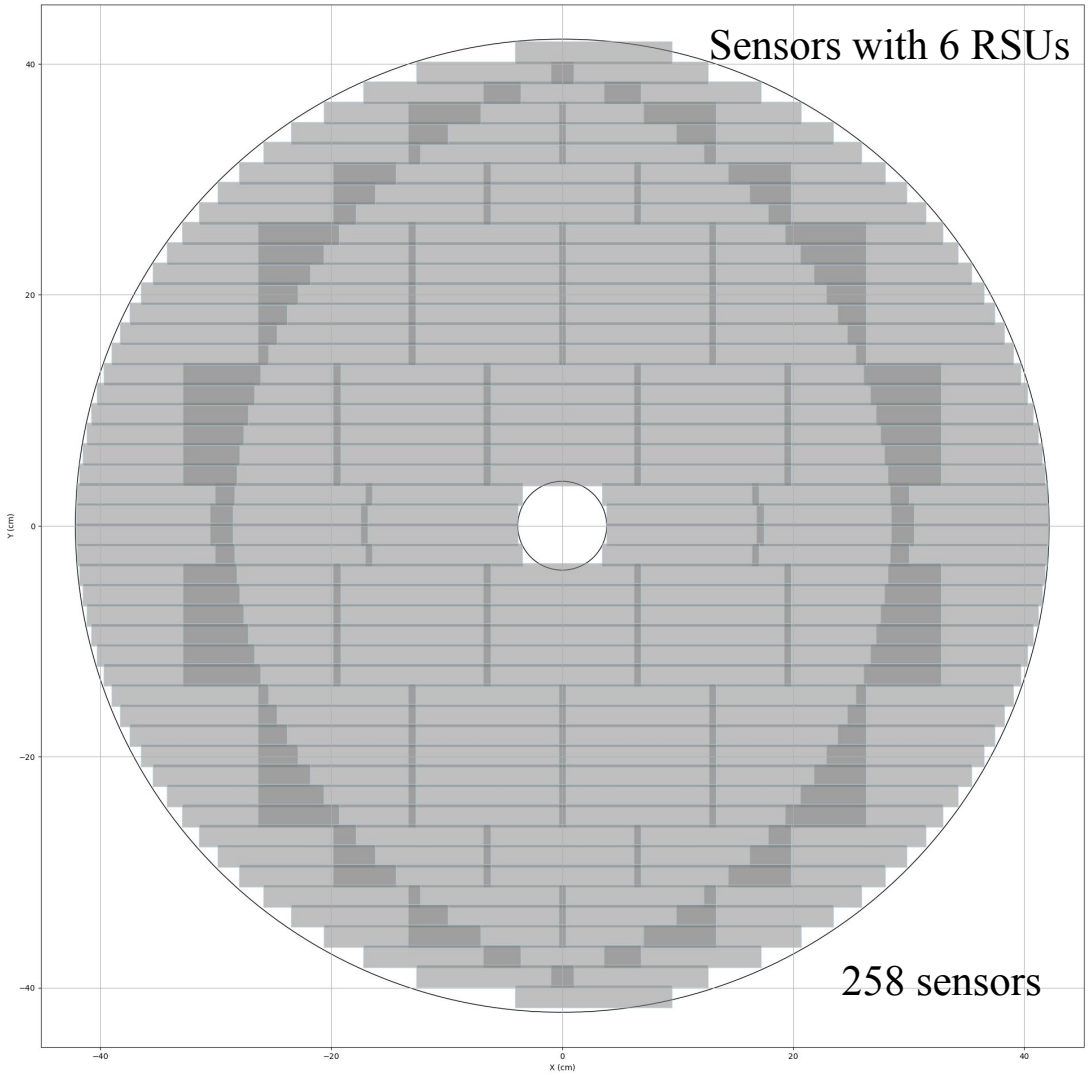
Region	Disk	|z| (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE/HE	ED0/HD0	250	36.76	240	0.24%

Region	Disk	|z| (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE/HE	ED1/HD1	450	36.76	415	0.24%

ePIC SVT Disks - ED2/HD2

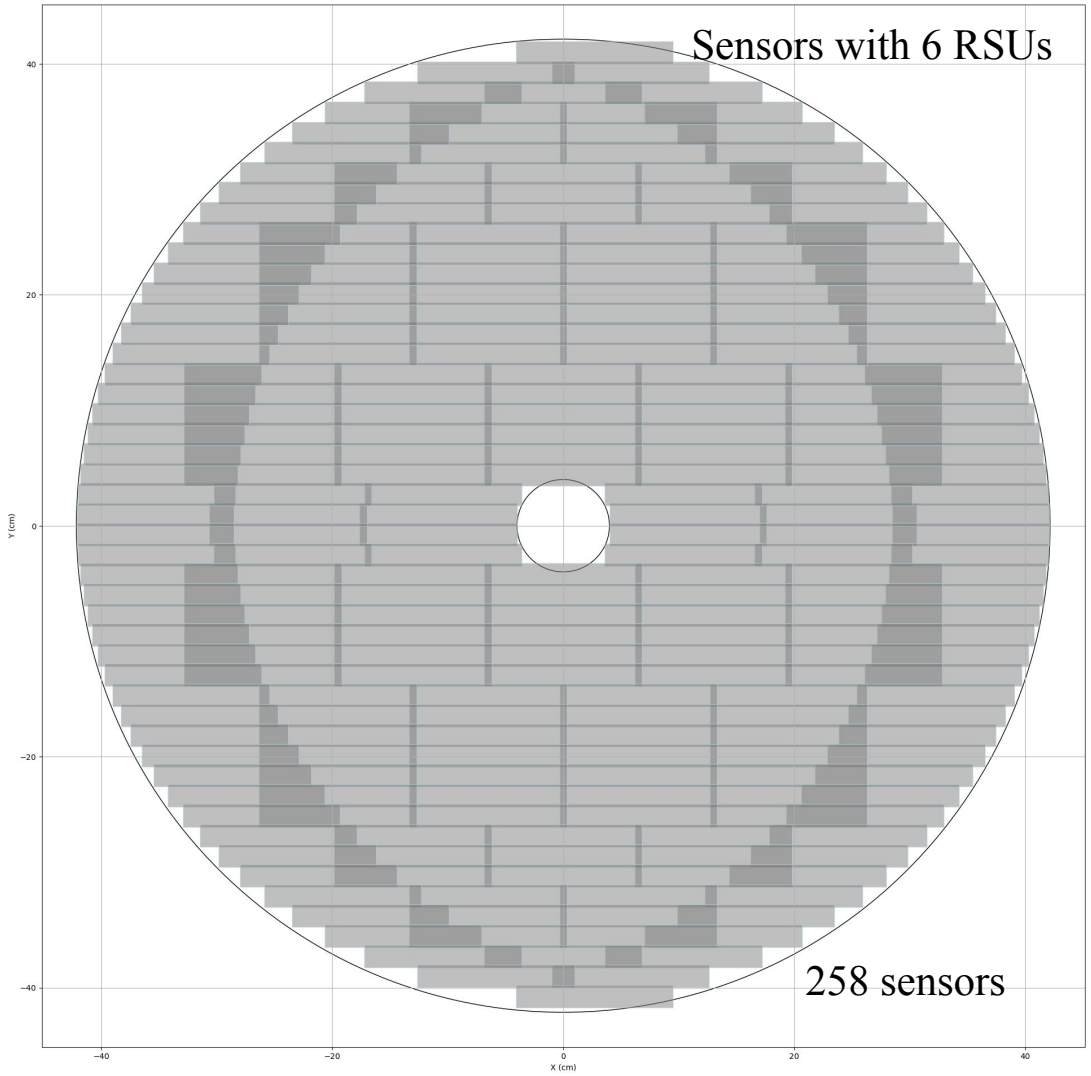


Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED2	-650	36.76	421.4	0.24%

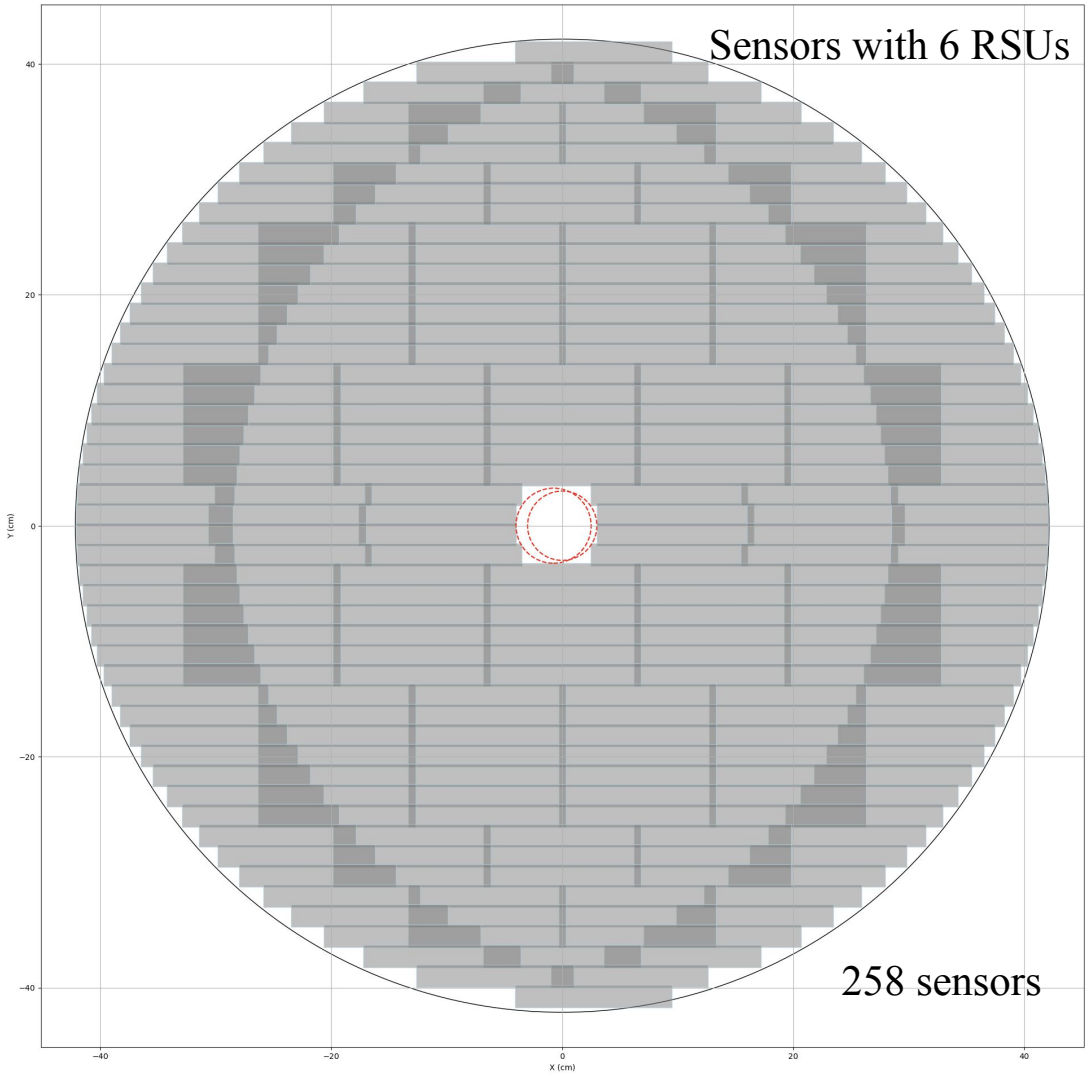


Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD2	700	38.46	421.4	0.24%

ePIC SVT Disks - ED3/HD3

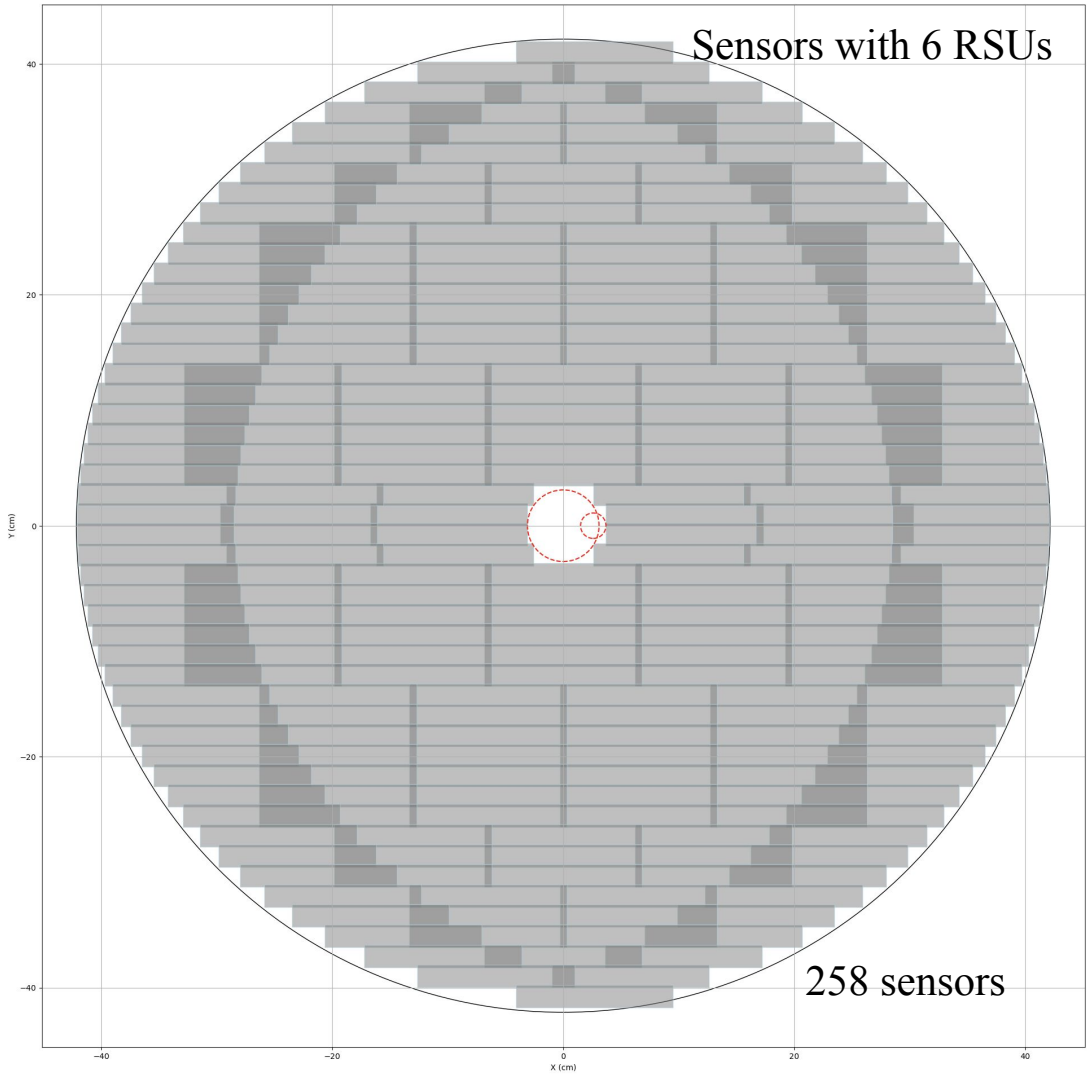


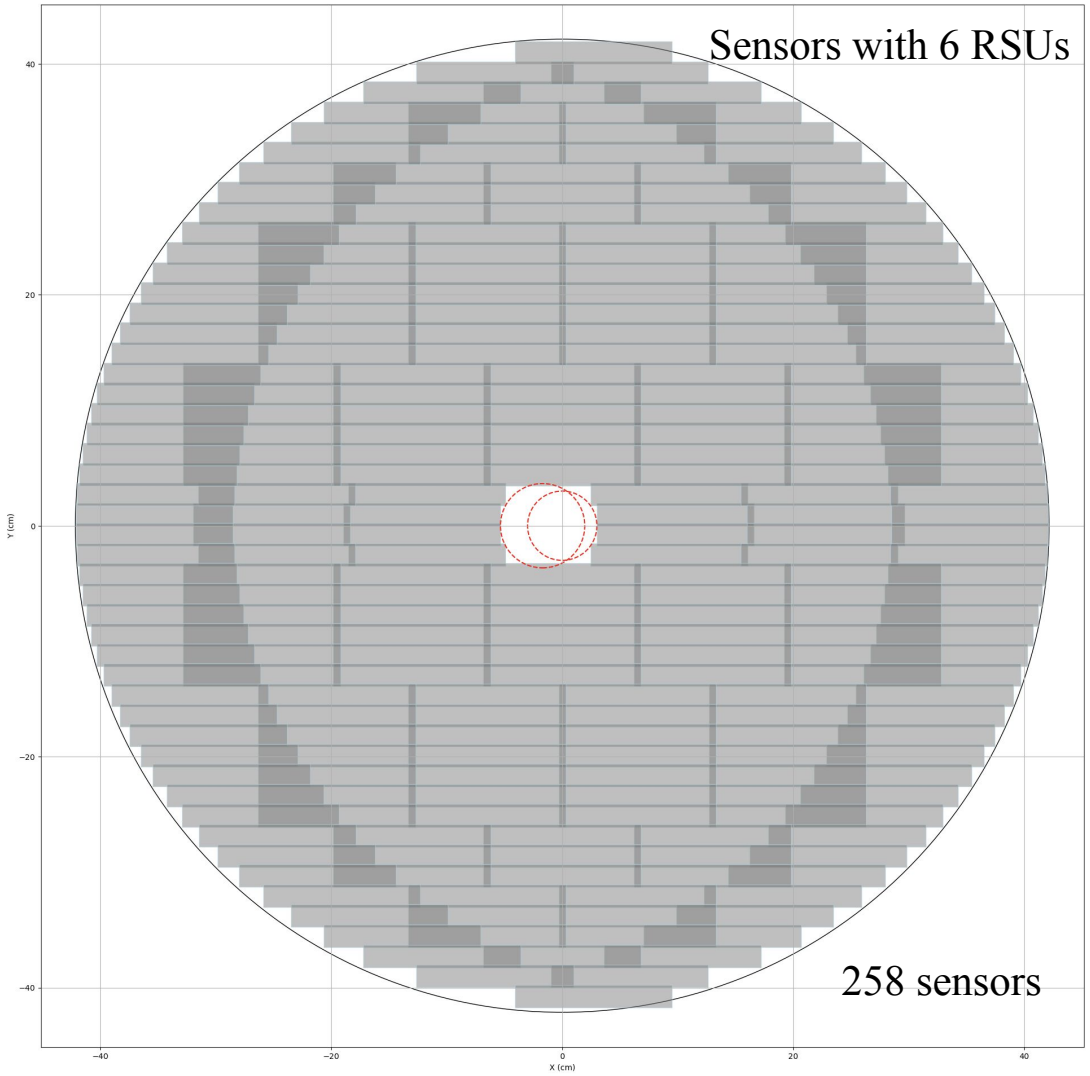
Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED3	-850	40.0	421.4	0.24%



Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD3	1000	30.0 @ C=(0,0) 32.5 @ C=(-7.5,0)	421.4	0.24%

ePIC SVT Disks - ED4/HD4





Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
EE	ED4	-1050	31.0 @ C=(0,0) 11.0 @ C=(26,0)	421.4	0.24%

Region	Disk	z (mm)	Inner radius (mm)	Outer radius (mm)	X/X0
HE	HD4	1350	30.0 @ C=(0,0) 36.5 @ C=(-17,0)	421.4	0.24%

ePIC SVT Disk Architecture

ePIC SVT - disk and barrel power and readout architecture
Sichtermann, Glover, Silber

Rev	Date	Author	Description
v1	2025-10-09	Joe Silber (LBNL)	imported original diagram from Ernst, added details on sizes, counts, and connection interfaces
v2	2025-10-15	Joe Silber (LBNL)	visual cleanup, approx dims on furcation tubes, power wire pairs, and CB-FIB ribbon
v3	2025-10-16	Joe Silber (LBNL)	incorporated comments from Nikki on barrel vs disk variations; made MFPC and bridge connections more visually clear
vx			in-progress – added ref links

Nomenclature

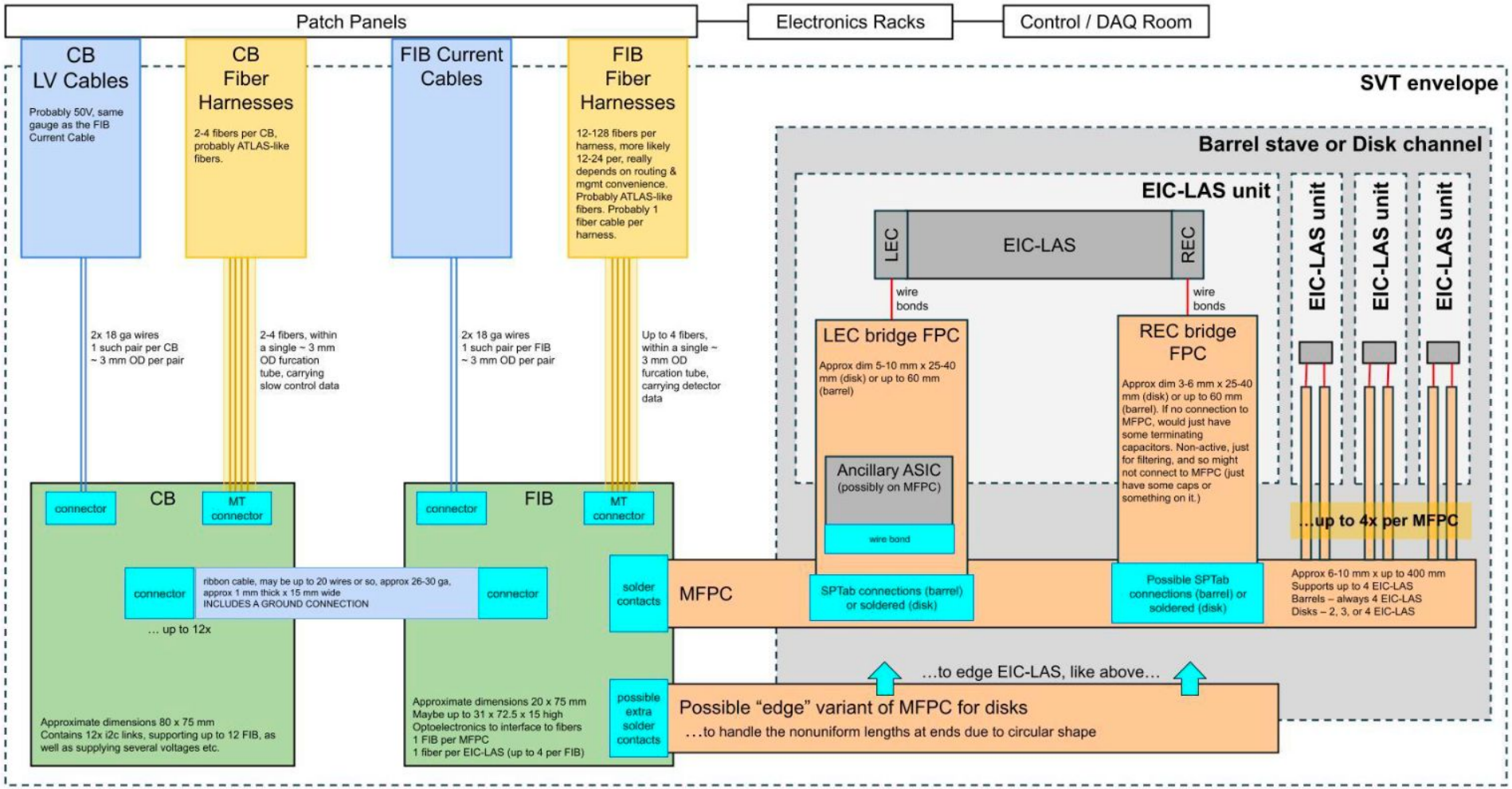
FPC … Flexible Printed Circuit
CB … Control Board
FIB … FPC Interface Board
LV … Low Voltage
MFPC … Main FPC
BFPC … Bridge FPC
SPTab … bonded overlapping Al/Kapton

Notes

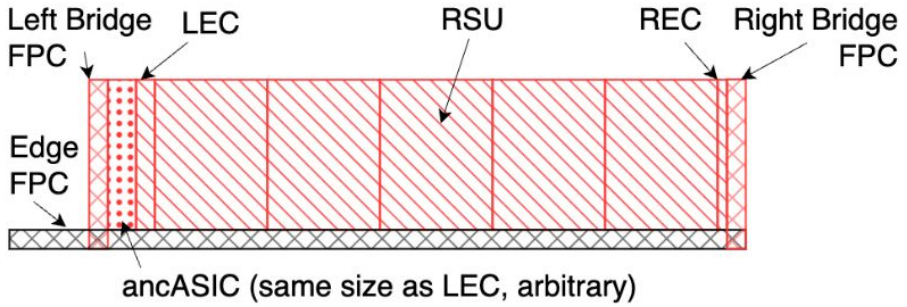
1. Not to scale.
2. Color-coding consistency not guaranteed.

References

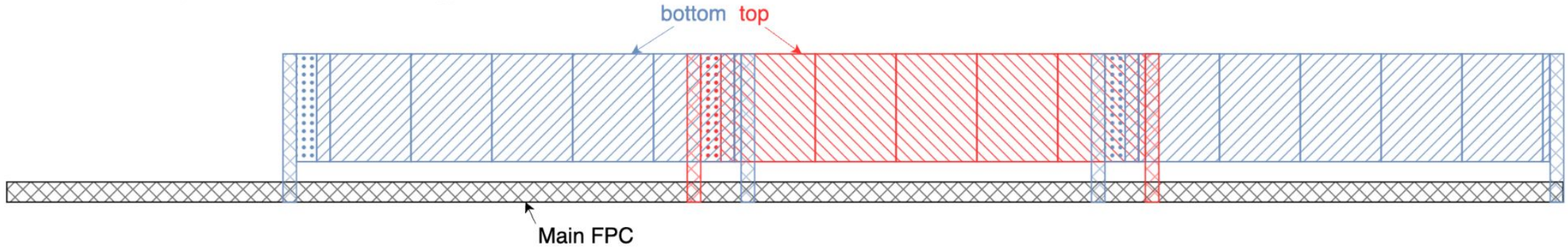
1. module drawing from Nikki 2025-08-22

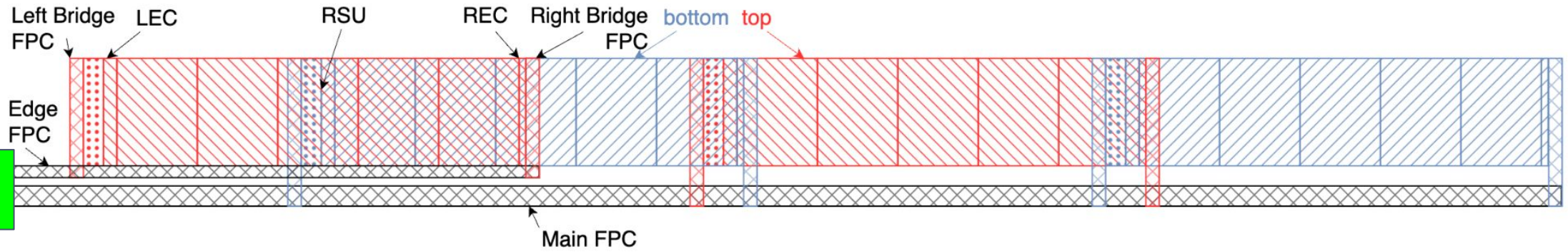


EIC-LAS Assembly for SVT Disks



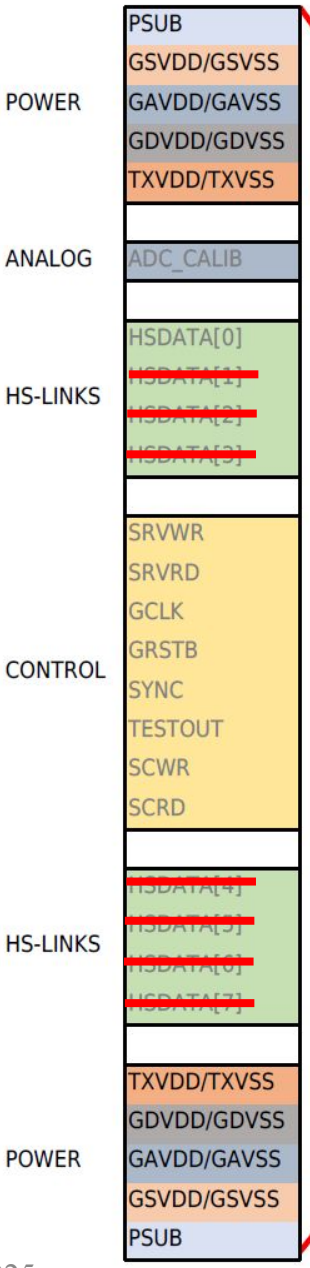
Left bridge FPC will connect to ancASIC and EIC-LAS LEC, while Right bridge FPC will connect to EIC-LAS REC. Both left/right bridge FPCs (could be one piece) will connect to a main or edge FPC, which will connect to FIB to make an assembly with upto four EIC-LAS + AncASIC.





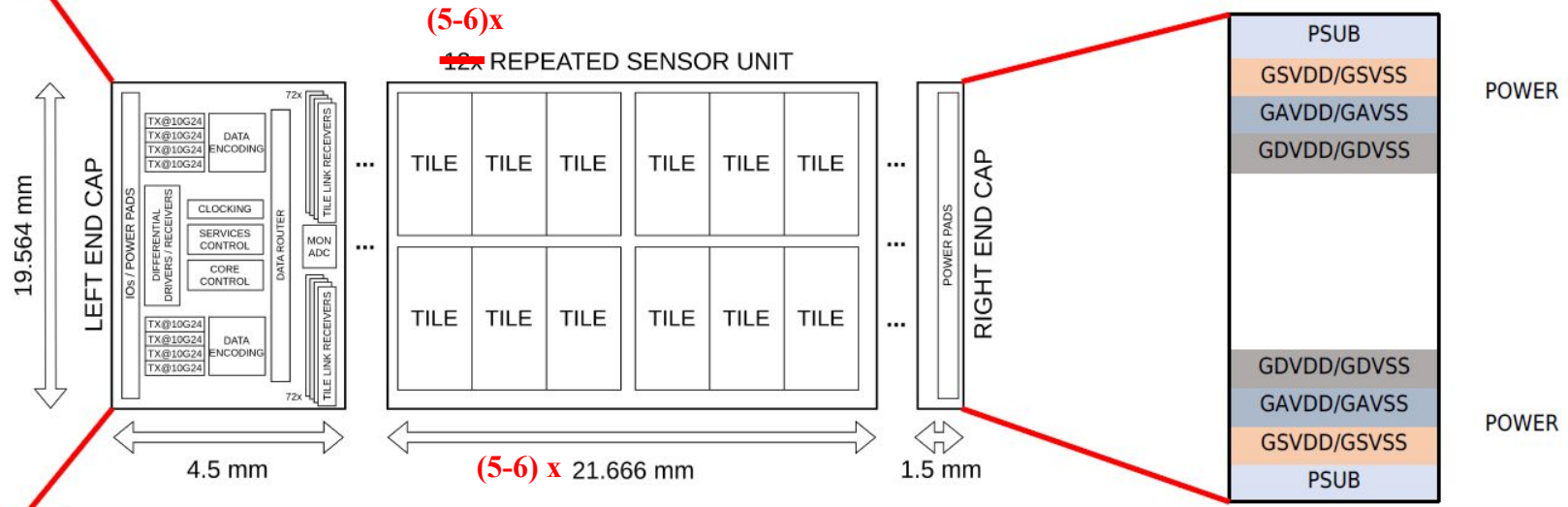
FIB

EIC-LAS



Supply	Typical (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	40	60
GAVDD/GSVSS (1.2V/0V)	170	270
GDVDD/GDVSS (1.2V/0V)	526	816
TXVDD/TXSVSS (1.8V/0V)	200	300

Signal	Frequency
GCLK	40/160/320 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5-10 Mbps
SCWR/RD	5-10 Mbps
HSDATA0	5.12/10.24 Gbps

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GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
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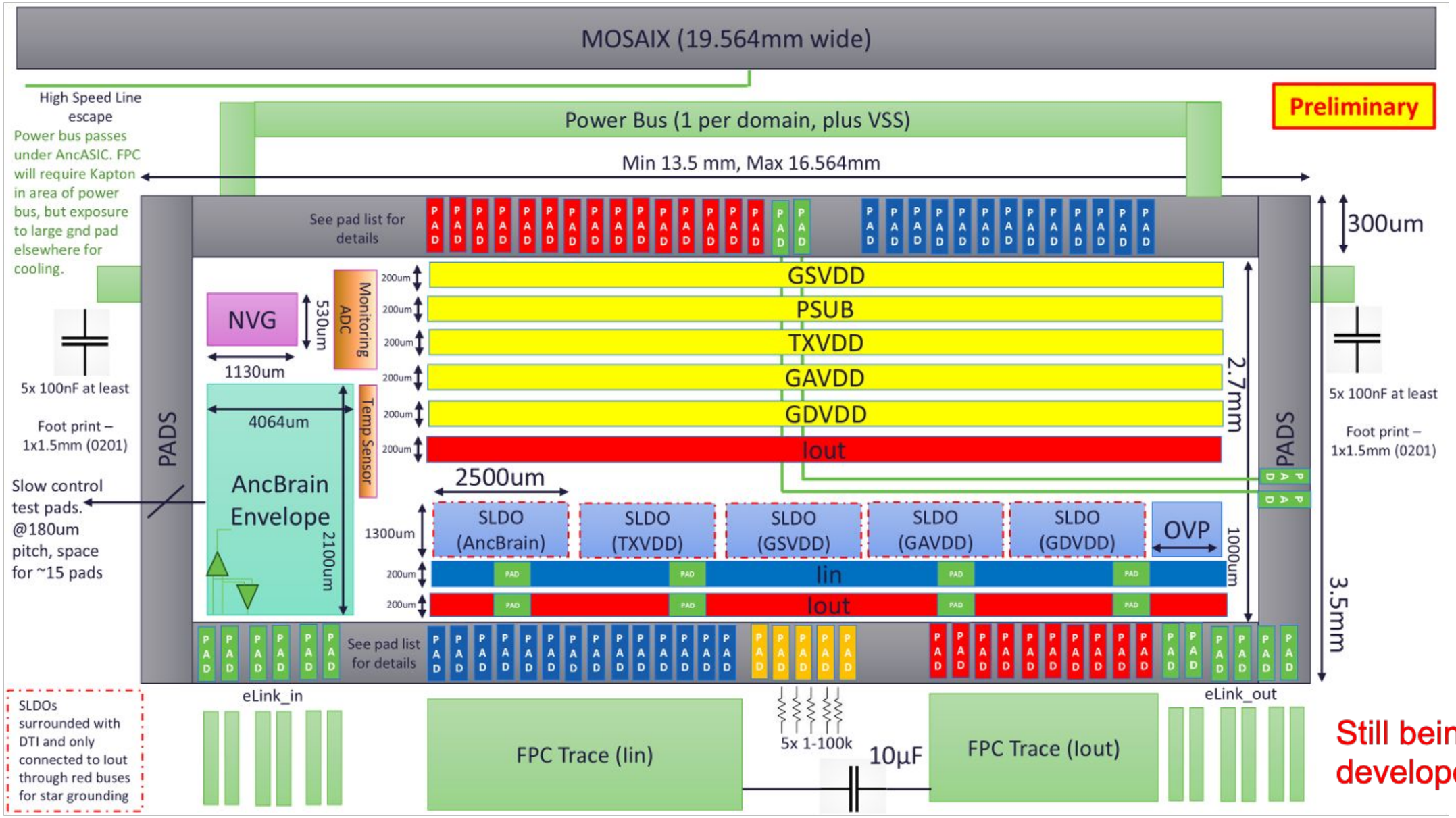
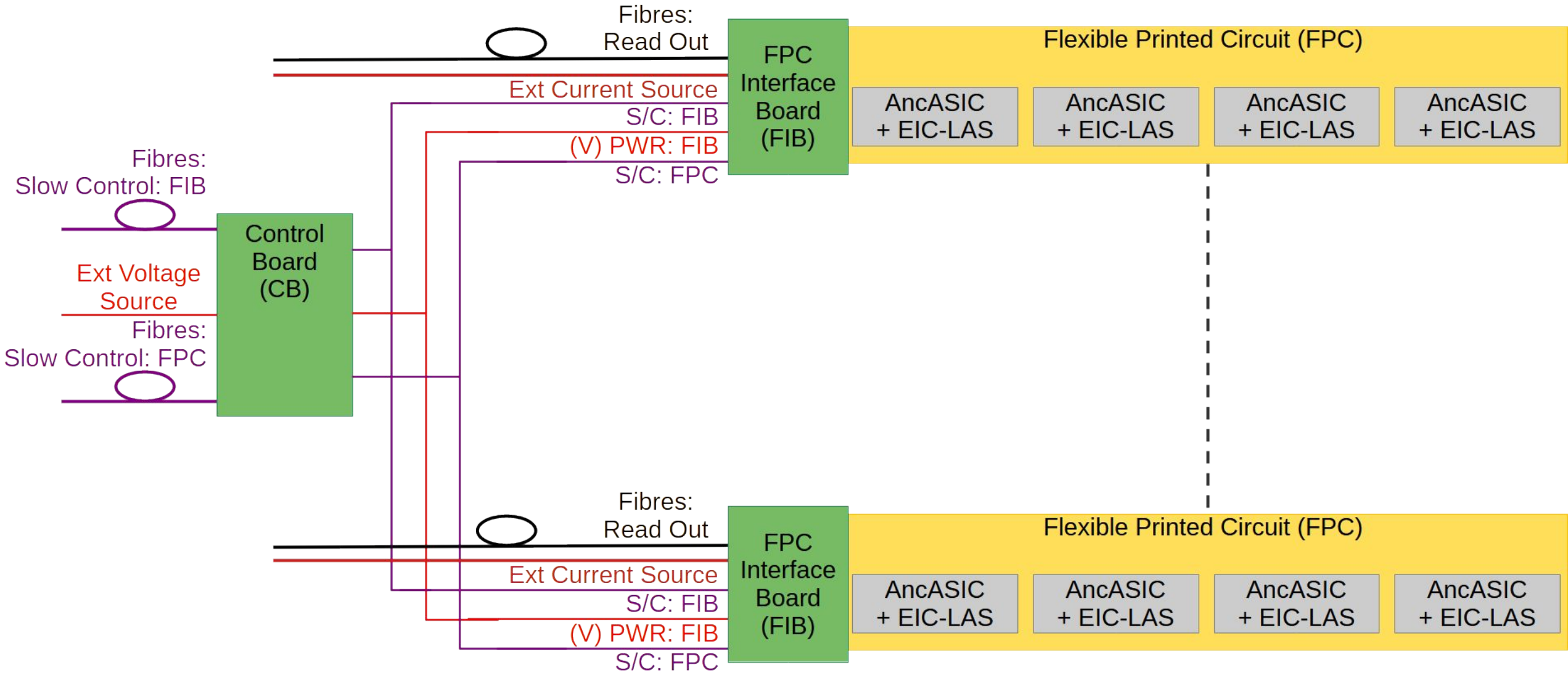
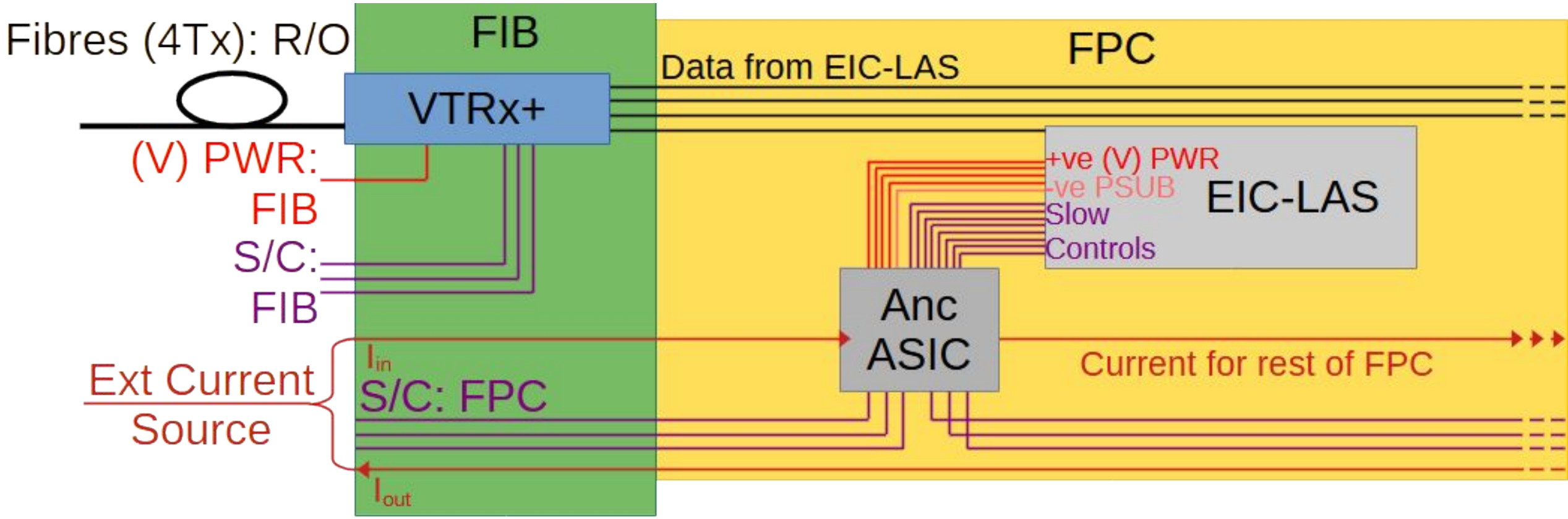
AncASIC


MOSAIX (19.564mm wide)
High Speed Line escape
Power bus passes under AncASIC. FPC will require Kapton in area of power bus, but exposure to large gnd pad elsewhere for cooling.
Power Bus (1 per domain, plus VSS)
Min 13.5 mm, Max 16.564mm
Preliminary
See pad list for details
300um
GSVDD
PSUB
TXVDD
GAVDD
GDVDD
Iout
NVG
530um
Monitoring ADC
1130um
200um
2.7mm
5x 100nF at least
Foot print – 1x1.5mm (0201)
PADS
4064um
Temp Sensor
AncBrain Envelope
2100um
Slow control test pads. @180um pitch, space for ~15 pads
2500um
SLDO (AncBrain)
SLDO (TXVDD)
SLDO (GSVDD)
SLDO (GAVDD)
SLDO (GDVDD)
OVP
1300um
1000um
Iin
Iout
3.5mm
SLDOs surrounded with DTI and only connected to Iout through red buses for star grounding
eLink_in
eLink_out
FPC Trace (Iin)
5x 1-100k
10µF
FPC Trace (Iout)
Still being developed…

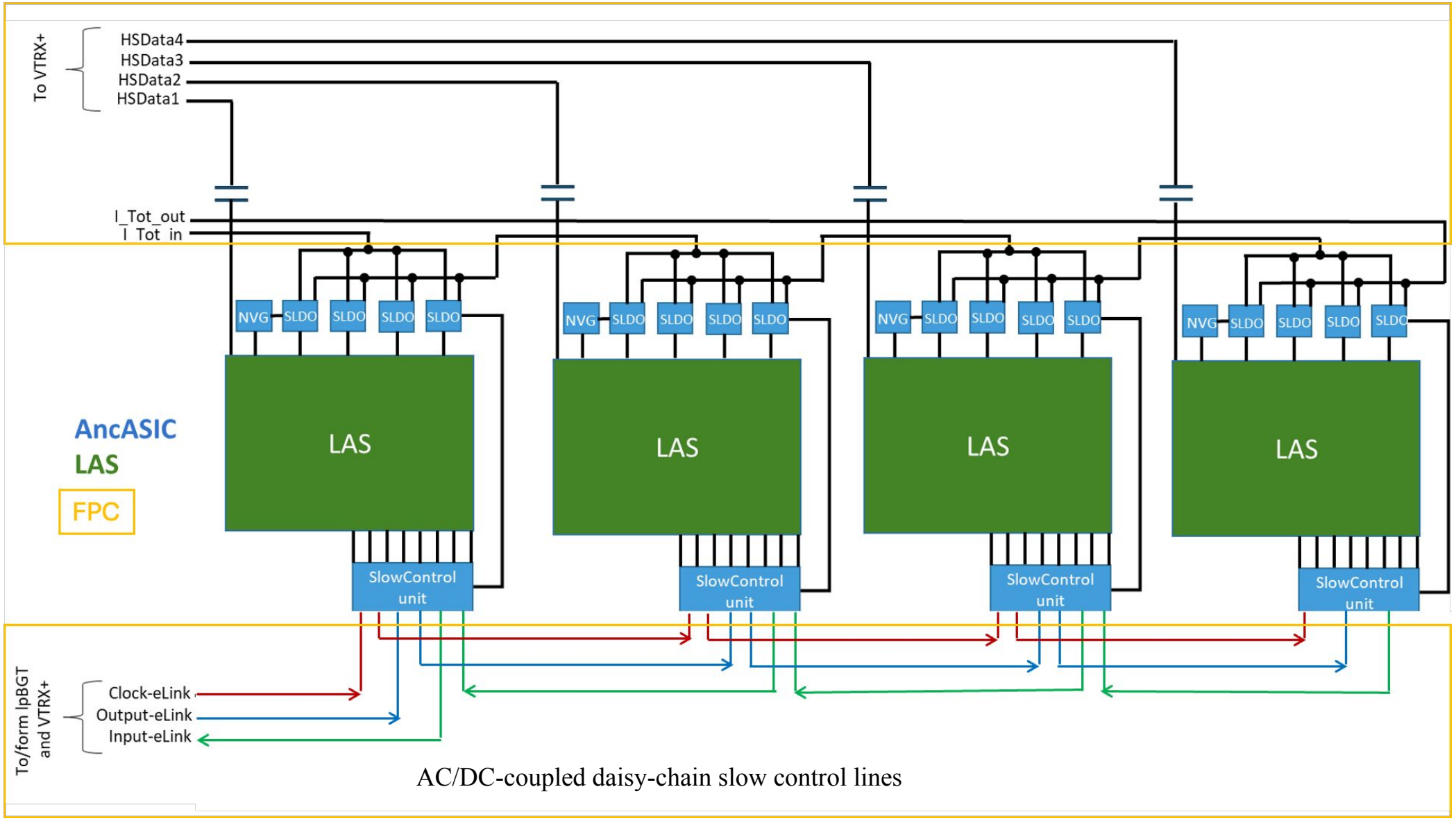
SVT Disks with EIC-LAS+AncASIC



SVT Disks with EIC-LAS+AncASIC



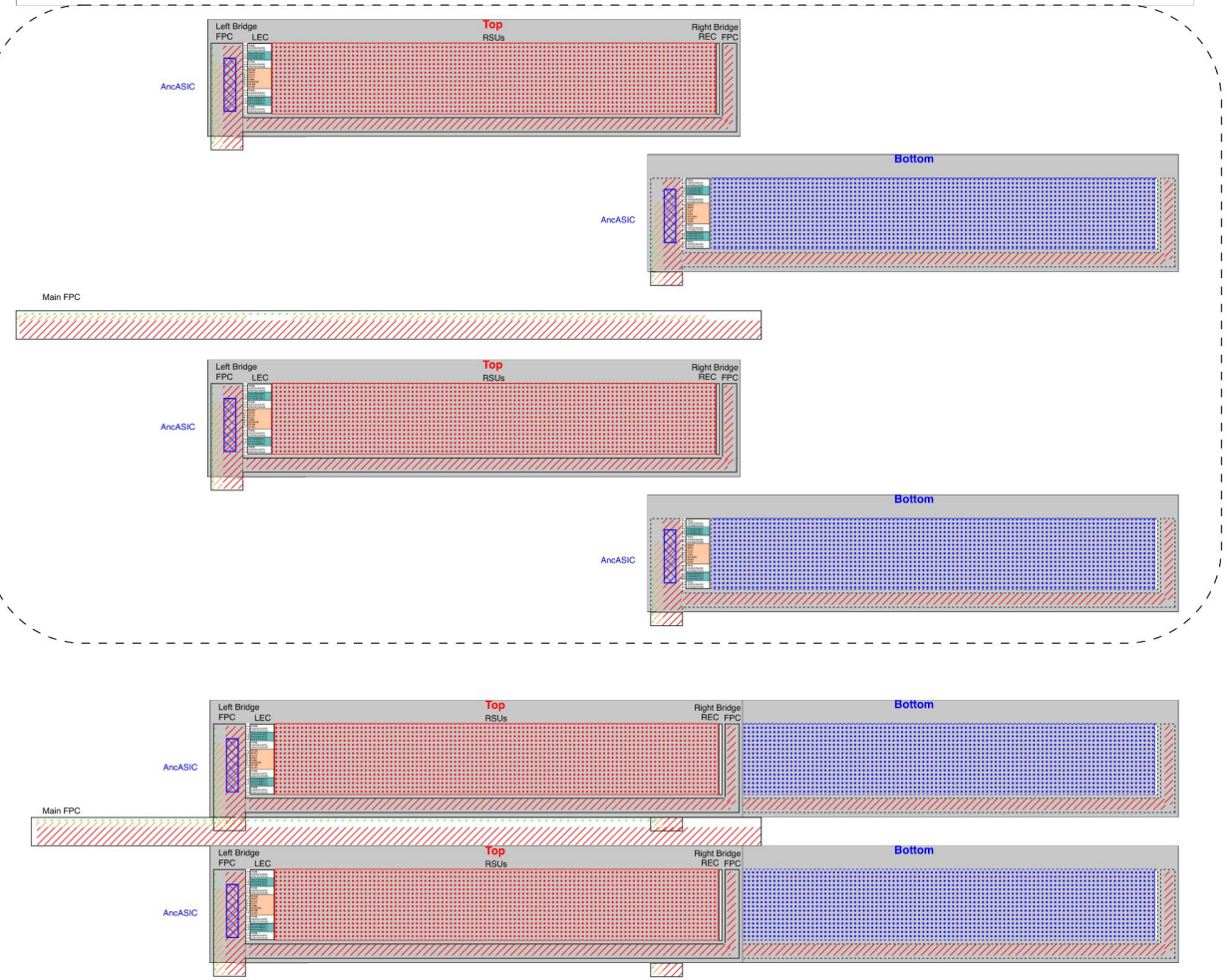
SVT Disks with EIC-LAS+AncASIC



AC/DC-coupled daisy-chain slow control lines

AncASIC on bridge or main FPC

8mm wide 40cm long Main FPC: signal (90+70+130+70+90)*(3+3)=2700 um; l_in/out/return: 5mm width, correspond to 0.075 Ohms per 10cm*2 Al, correspond to 0.08 W power loss
9mm wide 3cm long Left Bridge: signal (90+70+130+70+90)*(6+1)=3150 um; l_in/out/return: 1mm width, correspond to 0.0375 Ohms per 1cm*2 Al, correspond to 0.04 W power loss
4mm wide 12cm long Right Bridge: power: 0.1+1.8+0.1+0.5+0.1+0.3+0.1+0.3+0.1+0.3+0.1=3.8 mm, correspond to 0.066 W power loss



8mm wide 40cm long Main FPC: signal (90+70+130+70+90)*(3+3)=2700 um; l_in/out/return: 5mm width, correspond to 0.075 Ohms per 10cm*2 Al, correspond to 0.08 W power loss
8mm wide 3cm long Left Bridge: signal (90+70+130+70+90)*(8+1)=4050 um; power: 0.1+1.8+0.1+0.5+0.1+0.3+0.1+0.3+0.1+0.3+0.1=3.8mm, correspond to 0.013 W power loss
4mm wide 12cm long Right Bridge: power: 0.1+1.8+0.1+0.5+0.1+0.3+0.1+0.3+0.1+0.3+0.1=3.8 mm, correspond to 0.066 W power loss

Pros:
Cons:

AncASIC on bridge FPC

Signal	Rate	Comment	Type	Main FPC	Edge FPC	Bridge FPC
Serial Power Current	N/A	DC power current from FIB to AncASIC	DC	Y	Y	Y
SC_clk	40/160/320 MHz	Clock from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_in	40/160/320 Mbps	SC signals from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_out	40/160/320 Mbps	SC signals from AncASIC to lpGBT on FIB	AC/DC	Y	Y	Y
HS data	5.12/10.24 Gbps	HS data from EIC-LAS to VTRX+ on FIB	AC	Y	Y	Y
GCLK	160/320 MHz	Global clock from AncASIC to EIC-LAS	AC/DC	N	N	Y
SYNC GRSTB	N/A	SYNC/RESET from AncASIC to EIC-LAS	AC/DC	N	N	Y
SRVWR/RD SCWR/RD	5-10 Mbps	SC signals from AncASIC to EIC-LAS	AC/DC	N	N	Y
LV for EIC-LAS	N/A	LV from AncASIC to EIC-LAS	DC	N	N	Y

AncASIC on main/edge FPC

Signal	Rate	Comment	Type	Main FPC	Edge FPC	Bridge FPC
Serial Power Current	N/A	DC power current from FIB to AncASIC	DC	Y	Y	Y
SC_clk	40/160/320 MHz	Clock from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_in	40/160/320 Mbps	SC signals from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_out	40/160/320 Mbps	SC signals from AncASIC to lpGBT on FIB	AC/DC	Y	Y	Y
HS data	5.12/10.24 Gbps	HS data from EIC-LAS to VTRX+ on FIB	AC	Y	Y	Y
GCLK	160/320 MHz	Global clock from AncASIC to EIC-LAS	AC/DC	Y	Y	Y
SYNC GRSTB	N/A	SYNC/RESET from AncASIC to EIC-LAS	AC/DC	Y	Y	Y
SRVWR/RD SCWR/RD	5-10 Mbps	SC signals from AncASIC to EIC-LAS	AC/DC	Y	Y	Y
LV for EIC-LAS	N/A	LV from AncASIC to EIC-LAS	DC	Y	Y	Y

Interconnects with AncASIC on bridge FPC

	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB					
Main/Edge FPC	**Connector**, Soldering				
Bridge FPC	N/A	**soldering**, wire/TAB-bonding			
AncASIC	N/A	N/A	**wire-bonding**, TAB-bonding		
EIC-LAS	N/A	N/A	**wire-bonding,** TAB-bonding	N/A	

bold: preferred option

Interconnects with AncASIC on main/edge FPC

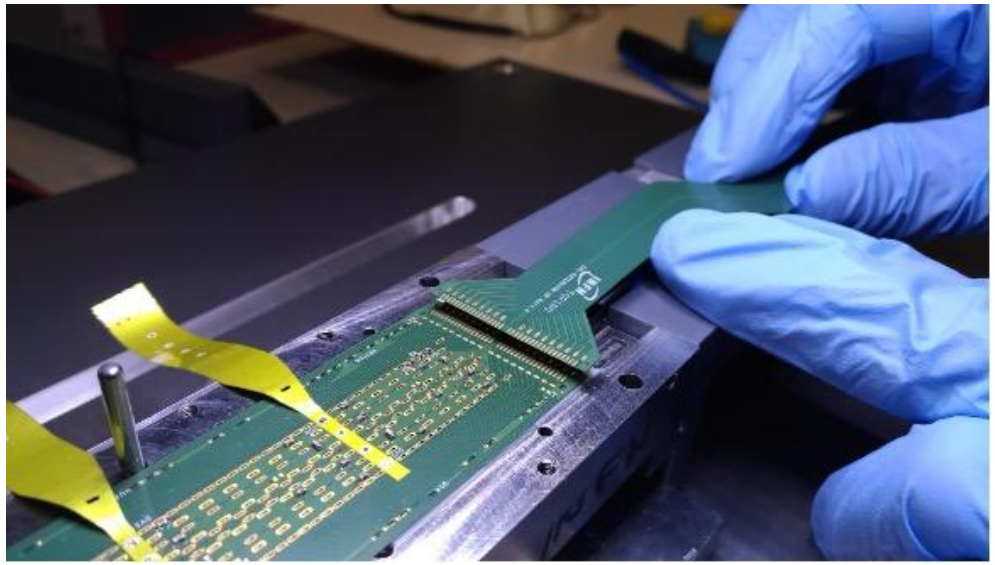
	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB					
Main/Edge FPC	**Connector**, Soldering				
Bridge FPC	N/A	**soldering**, wire/TAB-bonding			
AncASIC	N/A	**wire-bonding**, TAB-bonding	N/A		
EIC-LAS	N/A	N/A	**wire-bonding,** TAB-bonding	N/A	

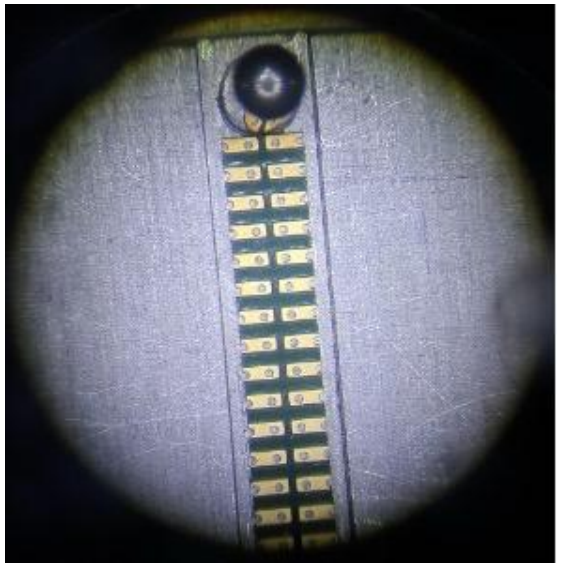
bold: preferred option

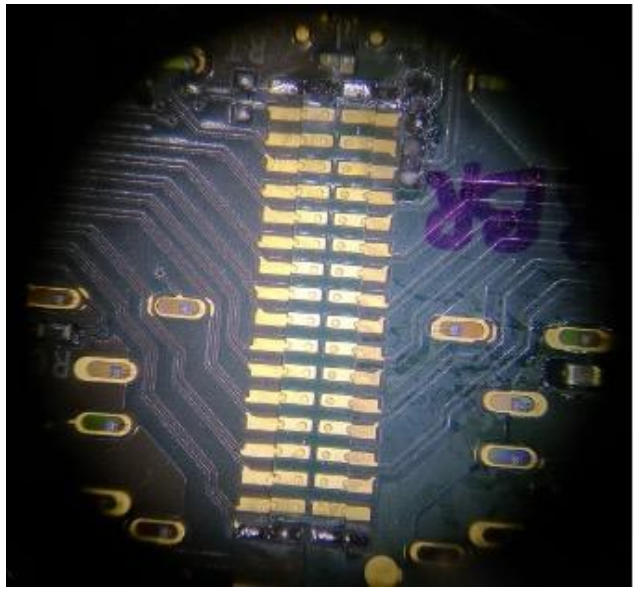
Summary

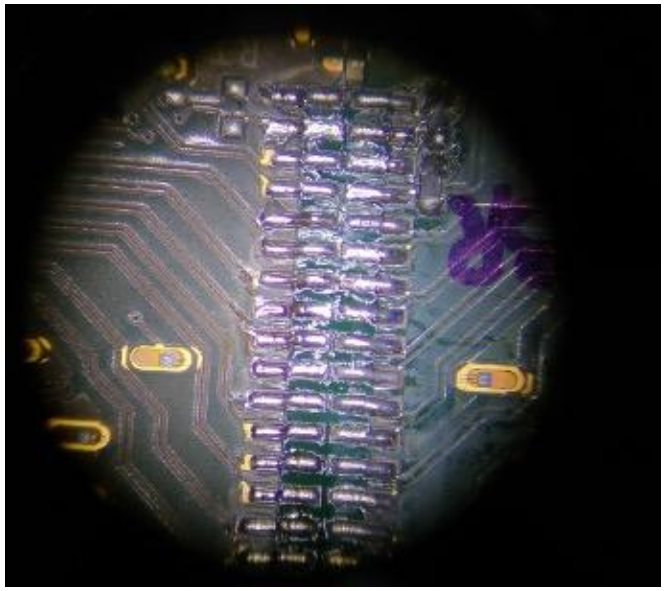
- Basic components and electrical connections are the same between disks and OBs, but there are a few differences
  - The number of modules on the disk varies per row
    - maintain a constant distance among neighboring modules in the center of the disk with a minimum overlap, and connect them to the main FPC; connect the module at the outer radius to the edge FPC
    - connect the main and edge FPCs in the same row to one FIB to form one serial power chain with upto four modules
  - Modules will need to be assembled on both sides of relatively large size half disks as one piece
    - prefer soldering over wire/TAB bonding to connect bridge FPC with main/edge FPC
  - Corrugated disk structure with air-cooling
    - AncASIC on bridge or main/edge FPC TBD - may impact AncASIC pad and FPC layouts

ALICE ITS2 FPC-to-FPC Soldering





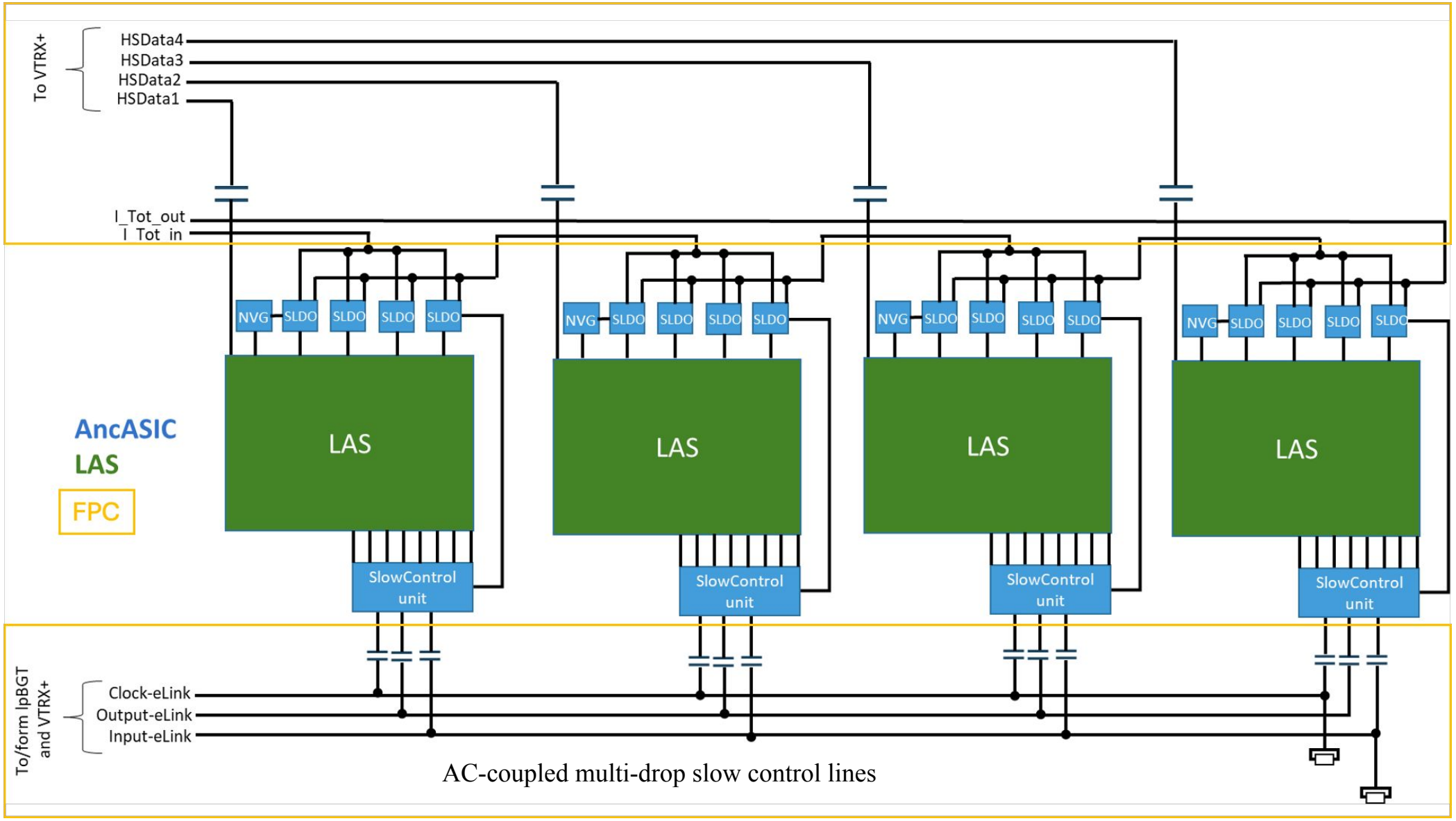




Summary and Plan

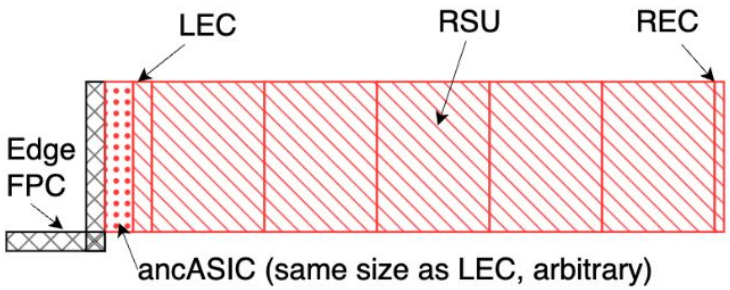
- UK colleagues have been working with LTU to produce Al-based FPC prototypes for OB
  - LTU: provided main and bridge FPC with SMD soldering through flex-mounts.
  - UK: investigate how to do TAB-bonding and wire-bonding; will check HS data transmission
- Goals at LBL for SVT disks:
  - investigate how to connect different components - can learn from OB experience !
  - validate power/signal integrity - can largely rely on OB conclusions
  - investigate connecting main and bridge FPCs by soldering
  - investigate connecting main and edge FPCs to FIB by connectors
  - investigate thermal and mechanical properties of the FPCs
  - develop relevant tooling and procedure for SVT disk assembly

SVT Disks with EIC-LAS+AncASIC

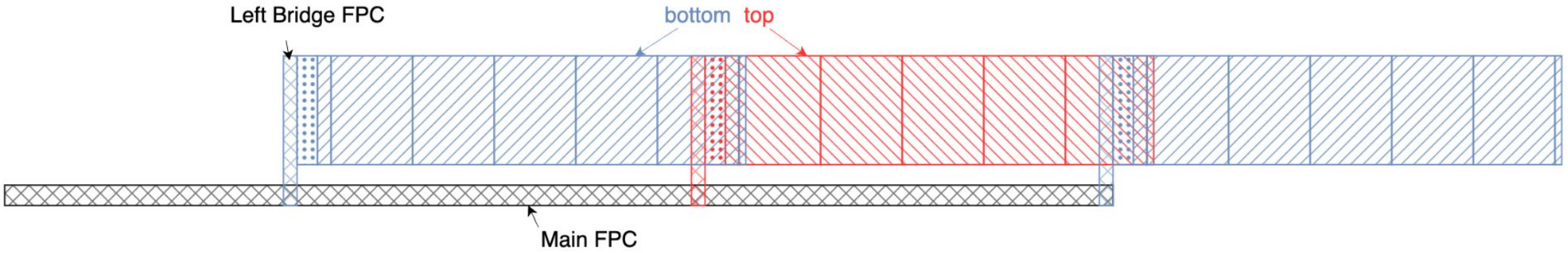


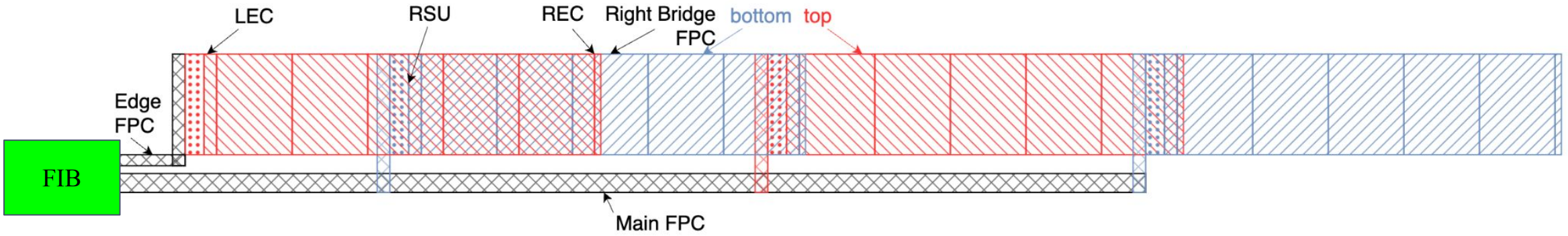
AC-coupled multi-drop slow control lines

EIC-LAS Assembly for SVT Disks

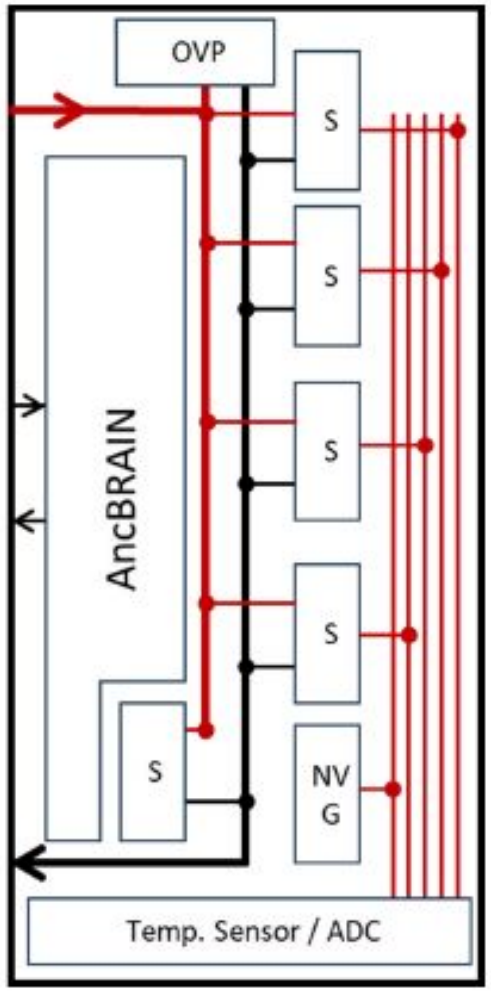


If there is no need to connect REC with decoupling capacitors, Left Bridge FPC will connect to ancASIC and EIC-LAS LEC, and to the Main FPC. Edge FPC will connect to ancASIC and EIC-LAS LEC. Edge and Main FPCs will connect to FIB to make an assembly with upto four EIC-LASs.





Sanity check on the “LAS side” of B-FPC



LEC

GSVDD/GSVSS

GAVDD/GAVSS

GDVDD/GDVSS

TXVDD/TXVSS

PSUB

HS DATA

CTRL,CLK, ETC

LEC: 152 pads, size: 144*91 um2;

~ symmetric pad distribution:
1 to 76; 77 to 152;

Q: GSVSS, GAVSS, GDSS, TXVSS, PSUB have common ground?

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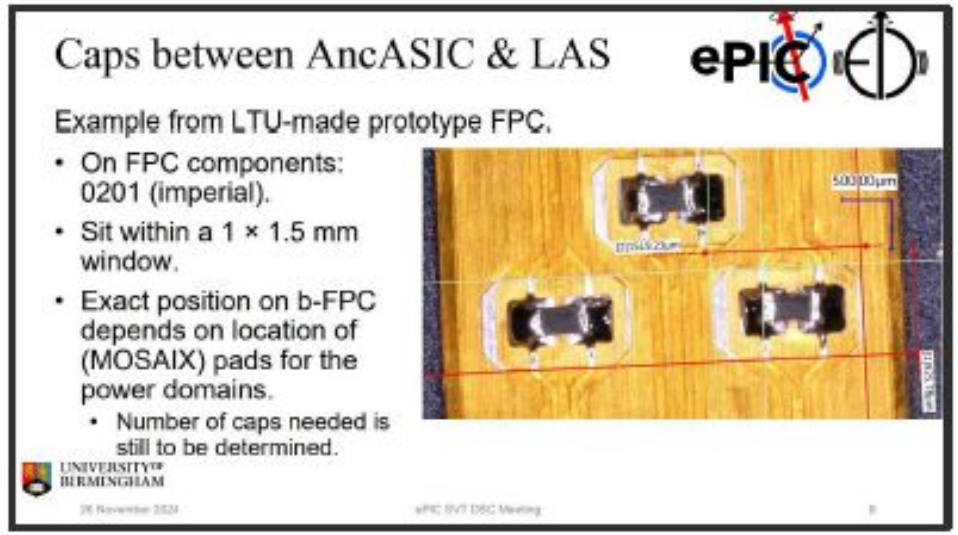
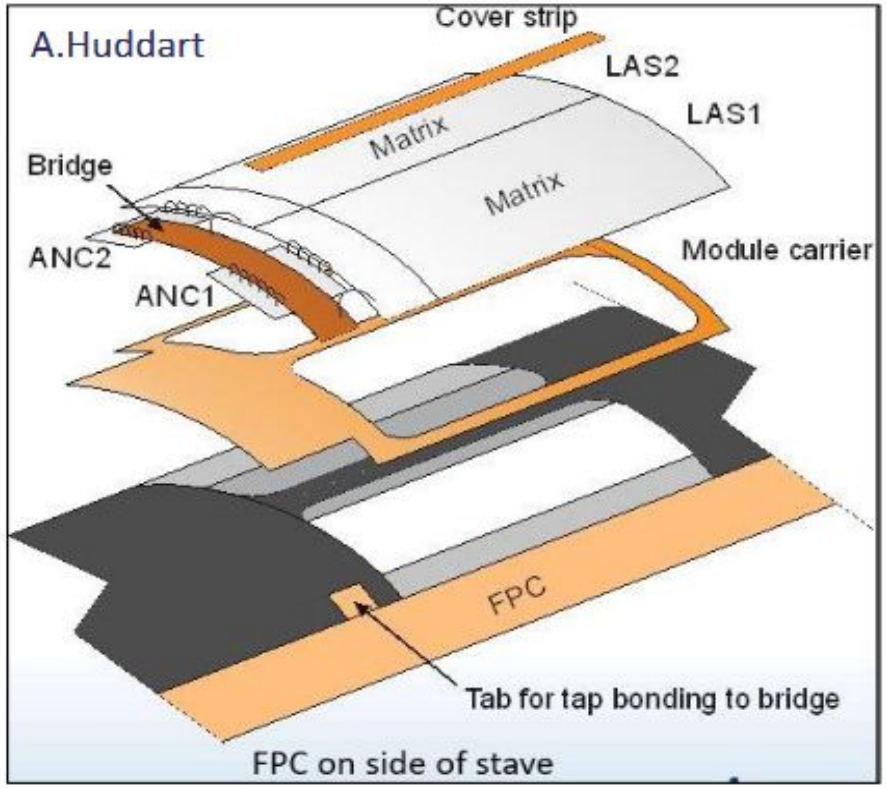
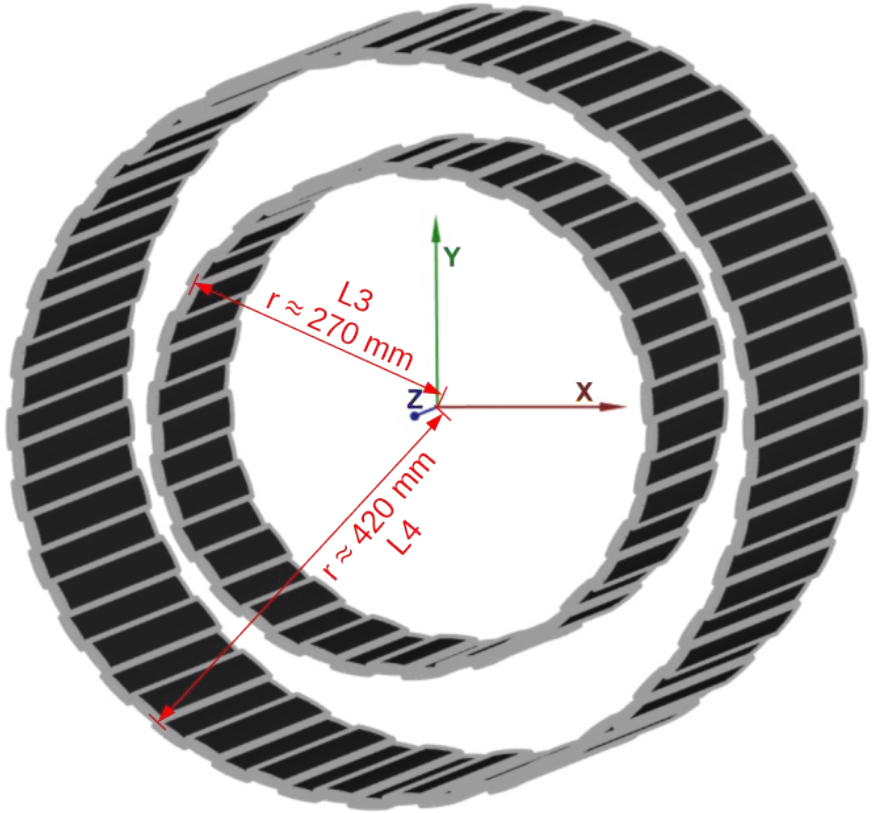


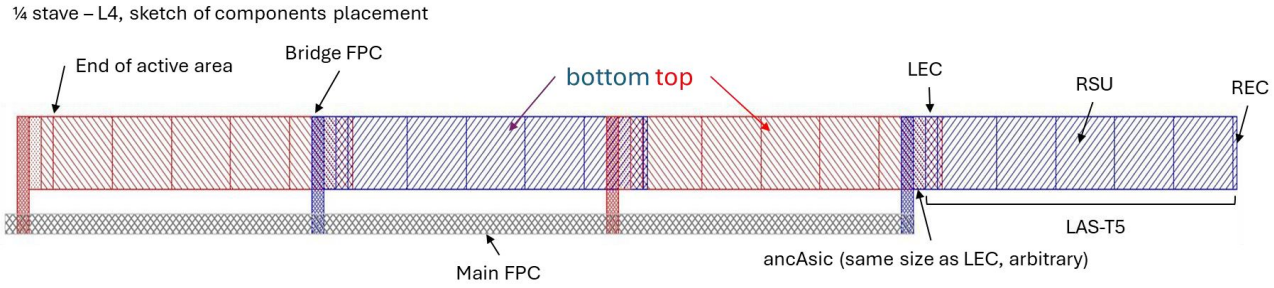
SVT Outer Barrel (L3/L4)

Outer barrels (L3, L4)

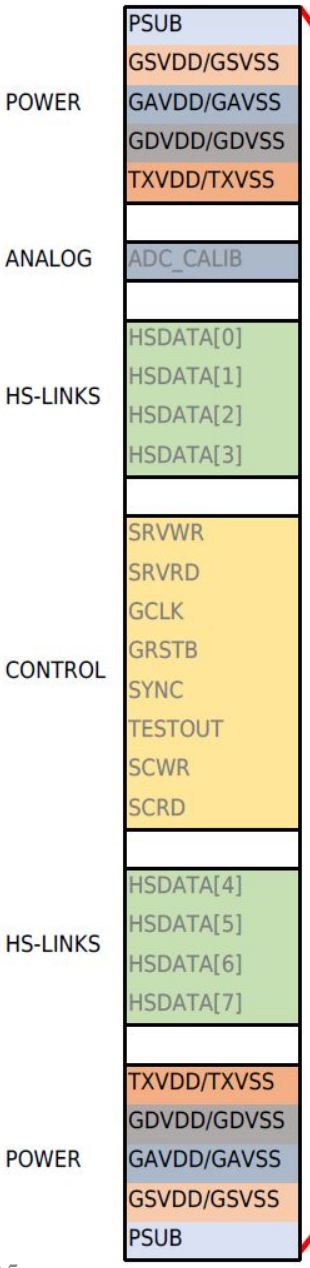
- **EIC large area sensors (EIC-LAS)** with design modified based on ITS3, mounted on more conventional staved structure with CF support and integrated air/water cooling
- **AncASIC** for sensor bias, serial power and slow control
- Radii of 27 and 42 cm; lengths of 42 and 84 cm
- X/X_0 ~0.25% and 0.55%





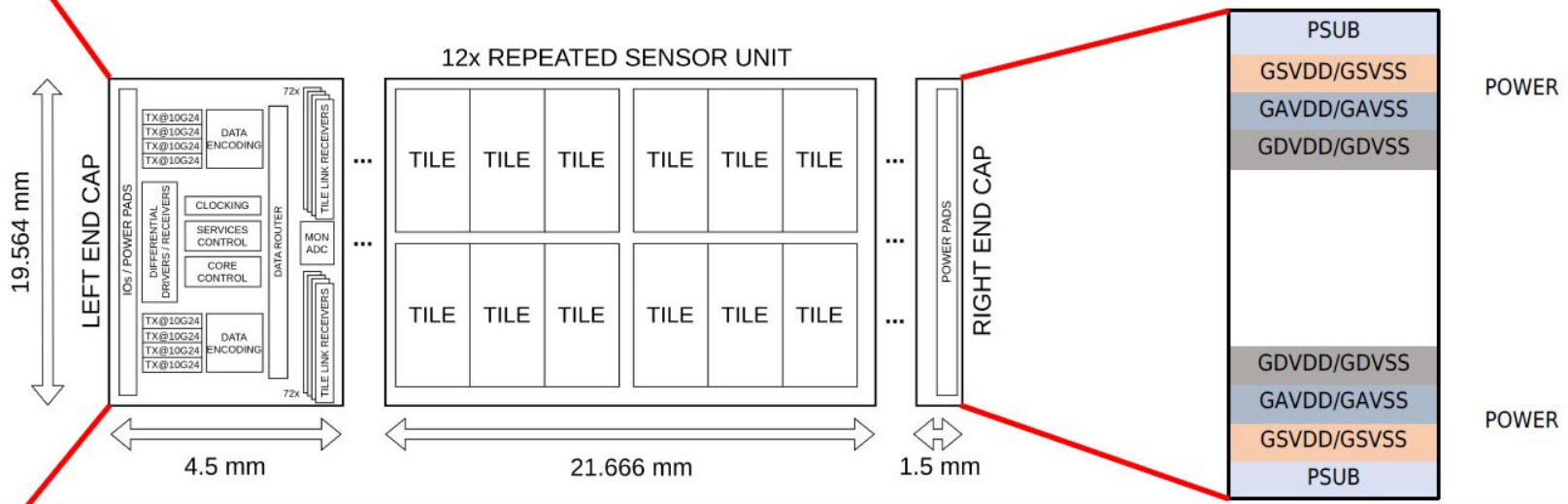


MOSAIX



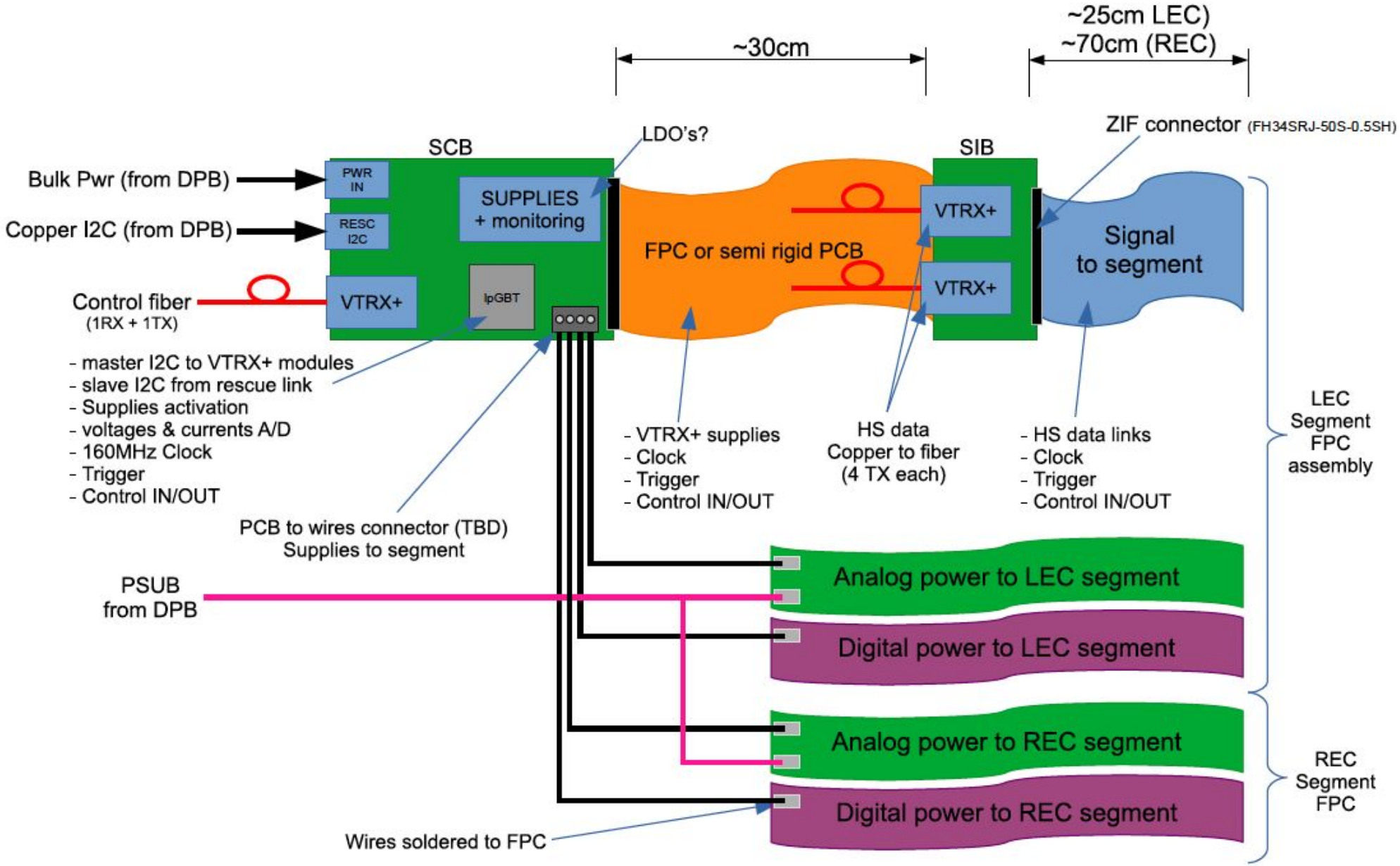
Power	Typ (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	50	
GAVDD/GSVSS (1.2V/0V)	340	540
GDVDD/GDVSS (1.2V/0V)	950	1430
TXVDD/TXSVSS (1.8V/0V)	200	

Signal	Frequency
GCLK	160 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5 Mbps
SCWR/RD	5 Mbps
HSDATA[0…7]	5.12/10.24 Gbps

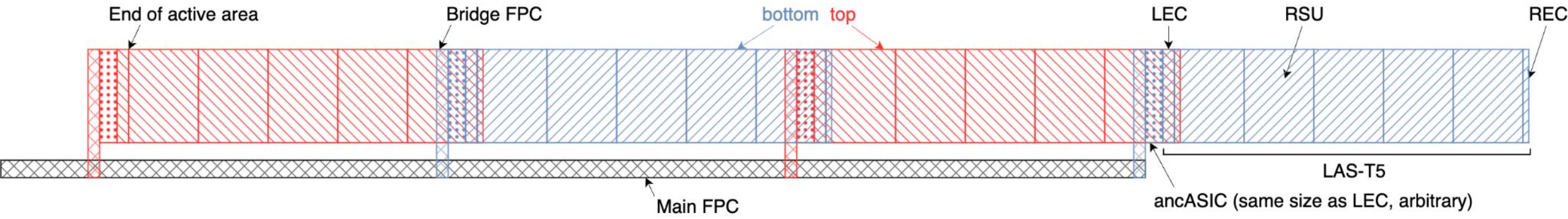



```
GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
```

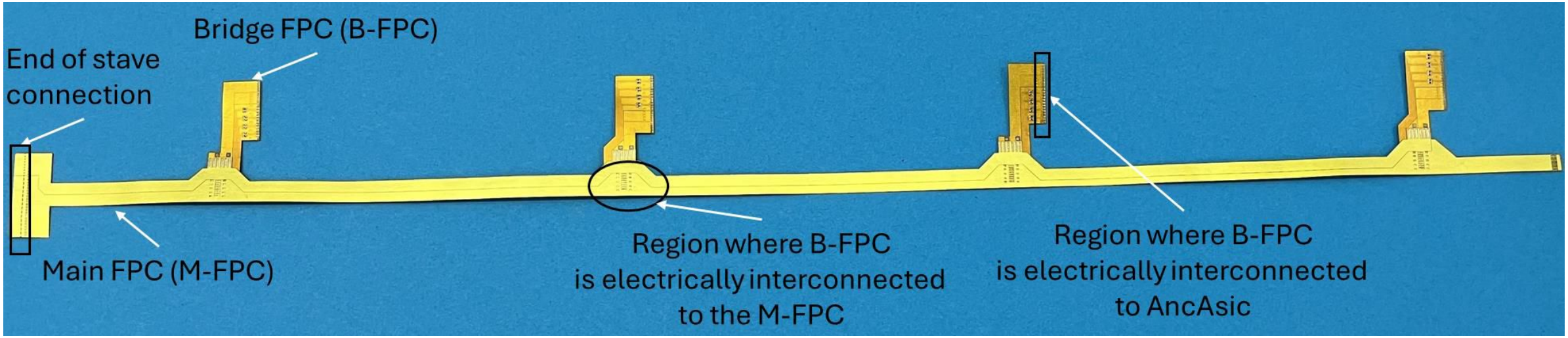
SVT IB with MOSAIX



SVT OB FPCs


End of active area
Bridge FPC
bottom
top
LEC
RSU
REC
LAS-T5
Main FPC
ancASIC (same size as LEC, arbitrary)

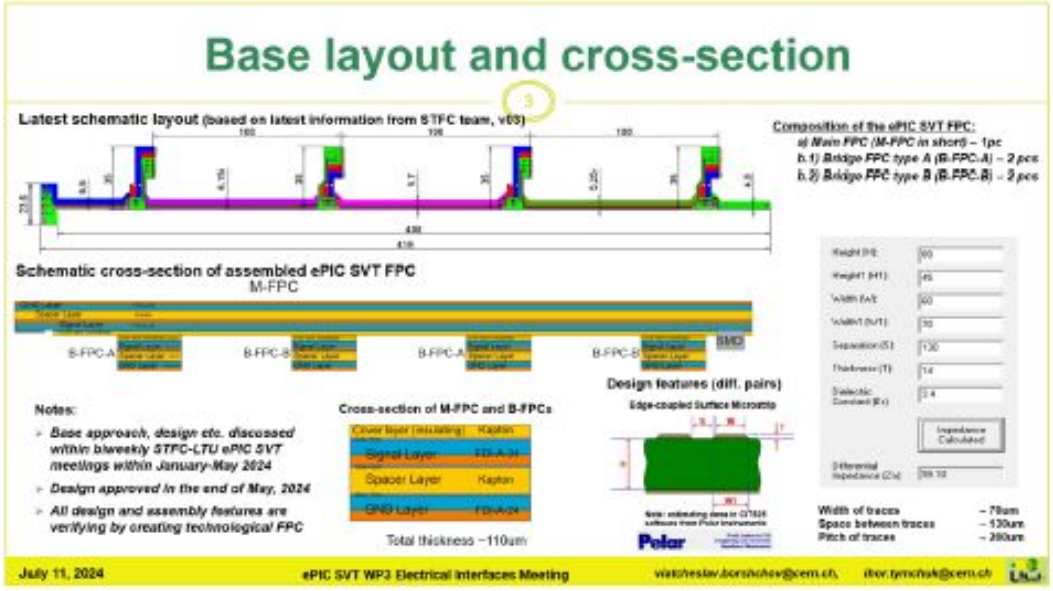
RPE LTU



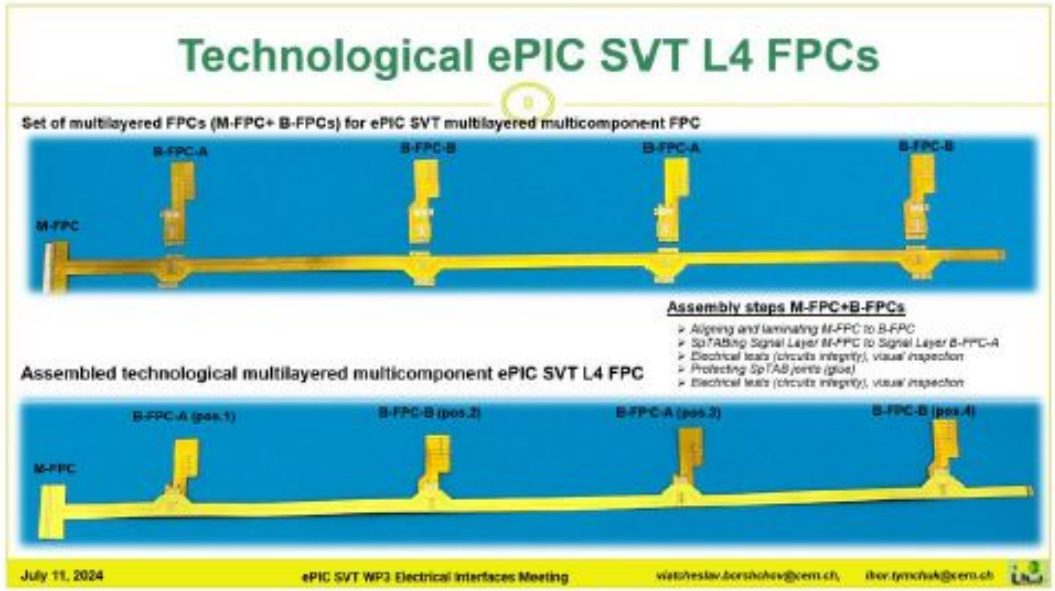
	Components	Thickness	Material	X0 (cm)	X0 (%)	Comment
HIC	FPC metal layers	28	Al	8.897	0.031	14um/layer x 2 layers = 28um (FDI-A-24)
	FPC insulating layers 1	20	polyimide	28.57	0.007	10um/layer x 2 layers = 20um (FDI-A-24)
	FPC insulating layers 2	25	polyimide	28.57	0.009	
	FPC binding glue	5	TBC	39.07	0.001	real glue unknown, assuming Araldite 2011
	Pixel Chip	50	Si	9.37	0.053	To change to 66um thickness, to read ITS3 TDR
Total (FPC + Pixel chip)					0.102	
Total FPC only					0.049	Note FPC material budget closer to Pixel chip (0.053%X))

Base approach and features (reminder)

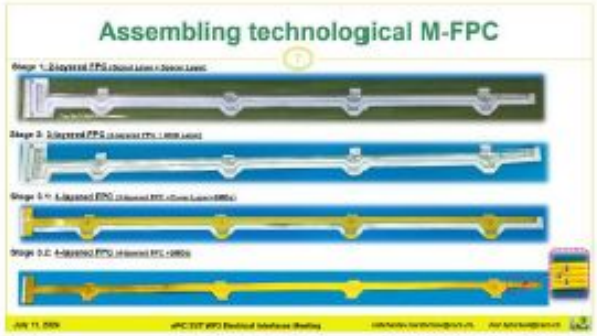
Base layout and cross-section



Technological ePIC SVT L4 FPCs



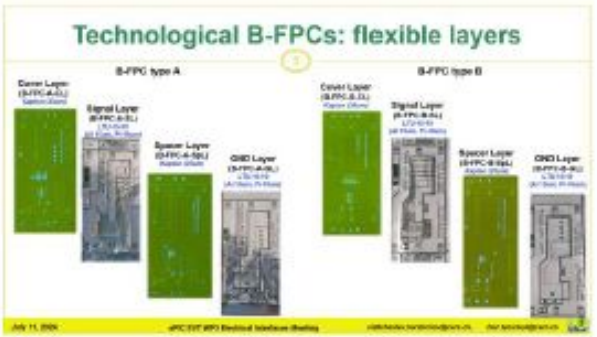
Assembling technological M-FPC



Assembling technological B-FPCs

Technological M-FPC: flexible layers

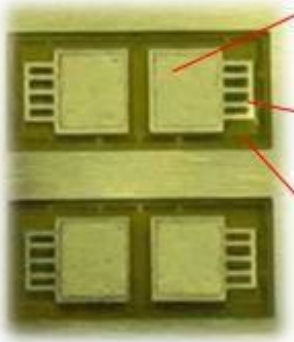
Technological B-FPCs: flexible layers



Features of mounting SMD components and connectors

For manufacturability increasing SMD components and connectors are mounting on small flexible carriers (flex-mounts) by soldering and after that connecting to board or cable by SpTAB

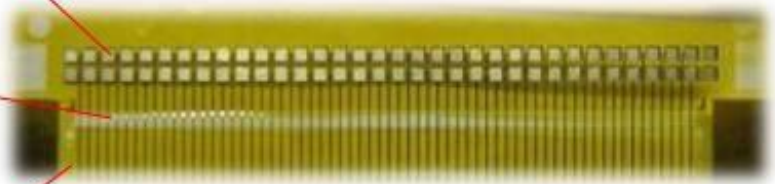
Flex-mounts for SMD component



Ni + SnBi layer (pads for soldering) ~ 2+8 um

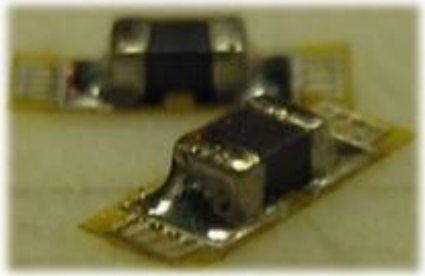
Aluminum layer (traces for bonding) ~ 15-30 um

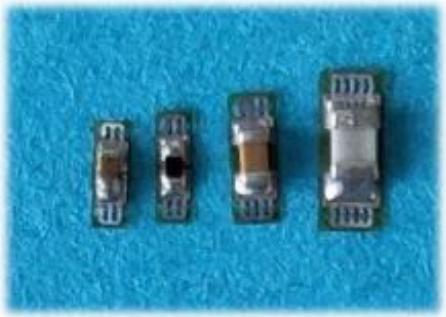
Polyimide layer ~ 10-20um



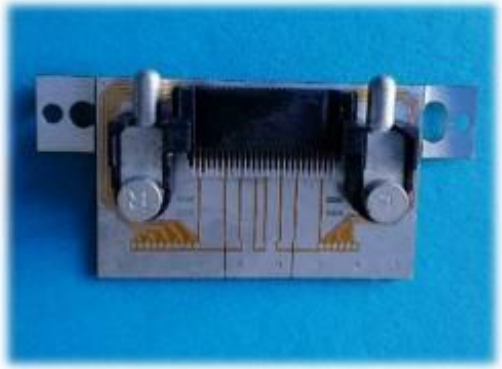
Flex-mounts for connectors

SMD components on flex-mounts





Connectors on flex mounts

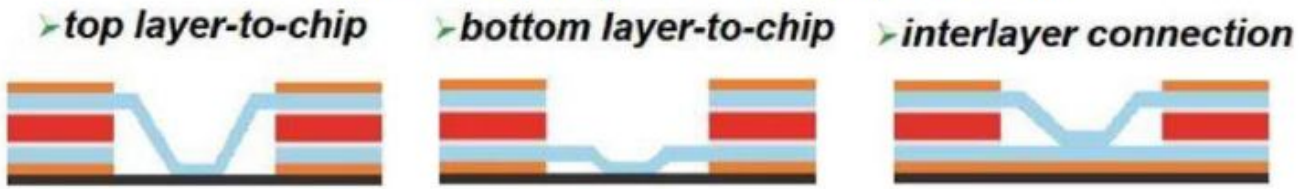


viatcheslav.borshchov@cern.ch, ihor.tymchuk@cern.ch

spTAB vs wire bonding

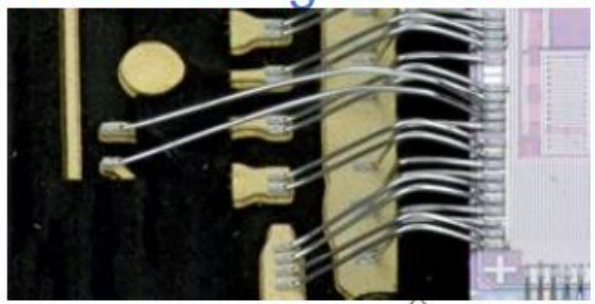
spTAB

- FPC traces have opening in support at bond locations.
- Aluminium trace (of FPC) is directly welded to a pad on the chip*.
- Foil width: ~70 µm.
- Best when FPC is above the chip*.
- Recommended by LTU.
  - Wire bonding to FPC is possible.



Wire bonding

- Wire connection between pads on 2 separate substrates (chip* or FPC).
- Wire width: ~25 µm (15-50 µm)
- Best when FPC is below the chip*.
- The current base-line for the ITS3 MOSAIX chip.
  - spTAB is being considered.



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* (EIC-LAS or AncASIC).

Main FPC only, slow control

Inject Data or Clock and data into SCTL1…3 from KCU105 via SMA cables

Remove termination from Main FPC

View SCTL1..3 with Scope

- Connect via SMA cable
  - 50 Ω terminated to GND at scope
  - Remove termination on test card
- Or connect via Hi (active) scope probe
  - With termination on test card.
- Also consider test in reverse direction.
- Additionally test these lines at > 1 Gbits/s using iBert bitstreams and MGT.

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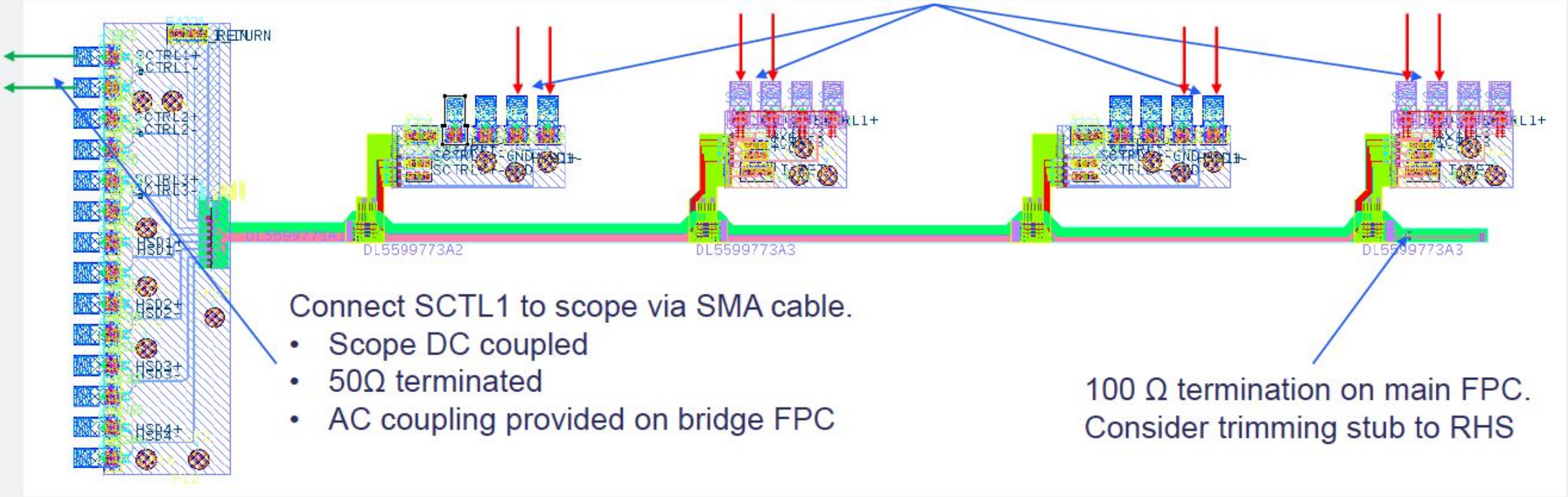
Technology

Slow Control RX data SCTL1

Inject Data into SCTL1 from KCU105 via SMA cable.



Connect SCTL1 to scope via SMA cable.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC

100 Ω termination on main FPC.
Consider trimming stub to RHS

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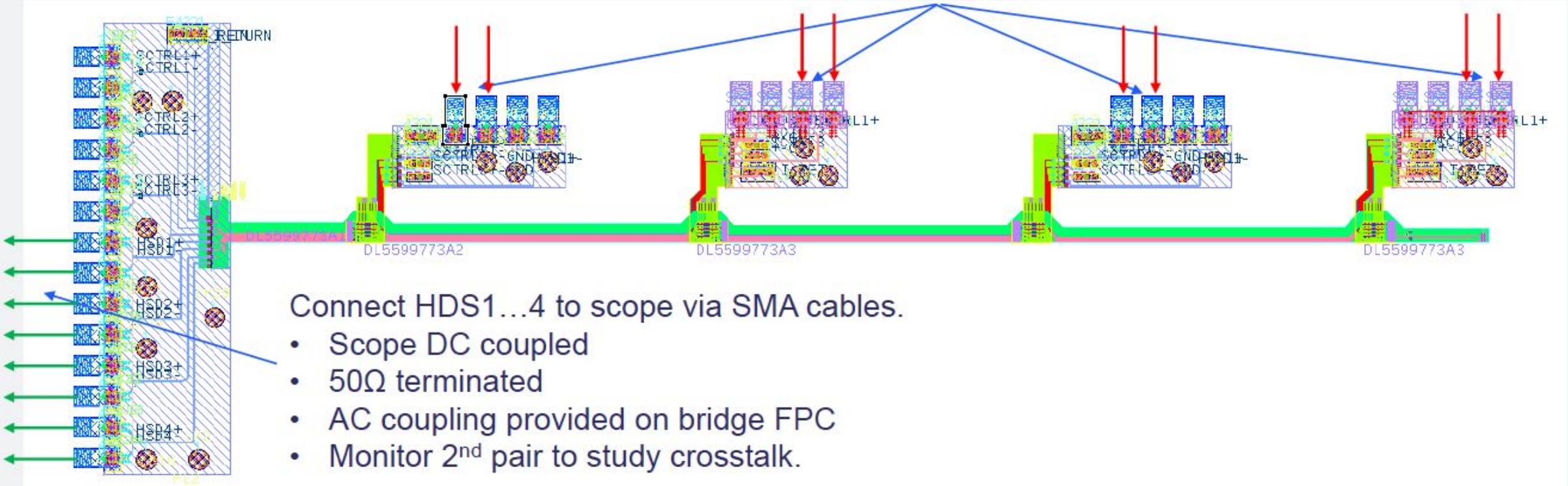
Technology

High speed signals

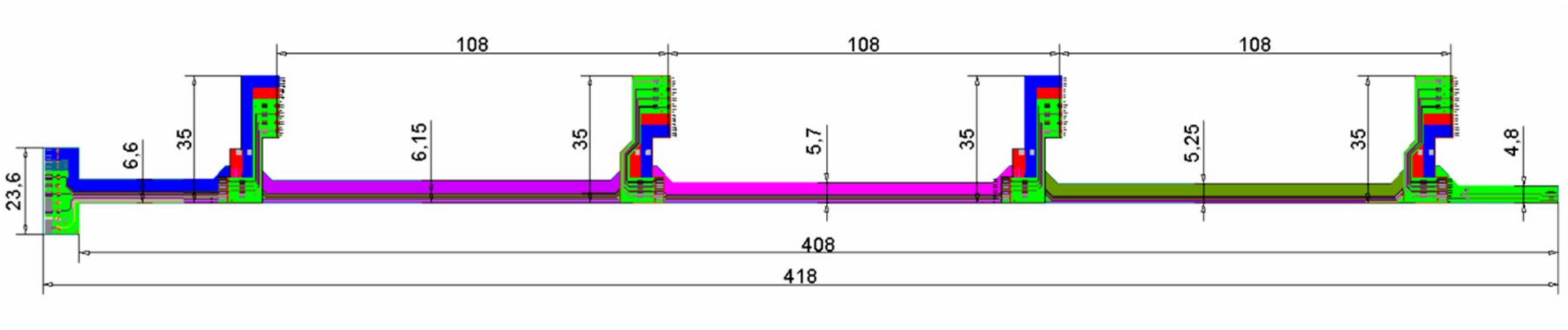
Inject Data into HSD1..4 from KCU105 via SMA cables.



Connect HDS1…4 to scope via SMA cables.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC
- Monitor 2nd pair to study crosstalk.

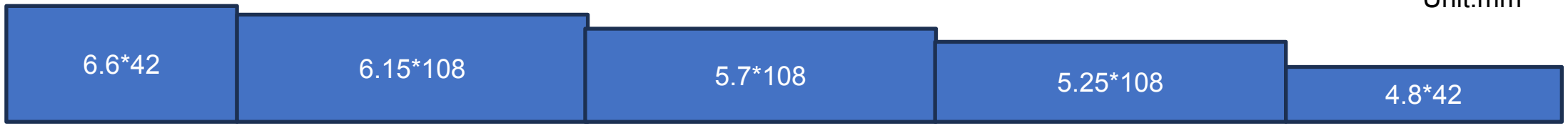
LTU FPC layout



LTU Dimensions

I_in & I_out width: 3.07mm
differential traces (width/space 6 mil) Total length: 408 mm

Unit:mm



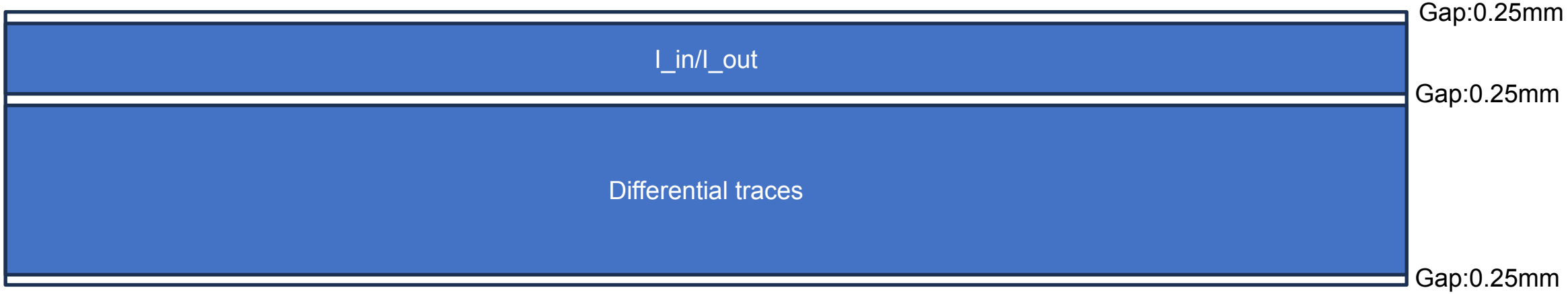
I_in +
7 differential traces

I_in +
6 differential traces

I_in +
5 differential traces

I_in +
4 differential traces

I_in +
3 differential traces



Total area: 2325.6 mm^2
Al area on Top layer (power & signal) : 1538.16
Fraction(Top): 1458.192/2136.42 = 66%
Fraction(Bottom): 1-(0.75*408/2325.6)=84%