AncBrain Hardware Mockup Status and Plan

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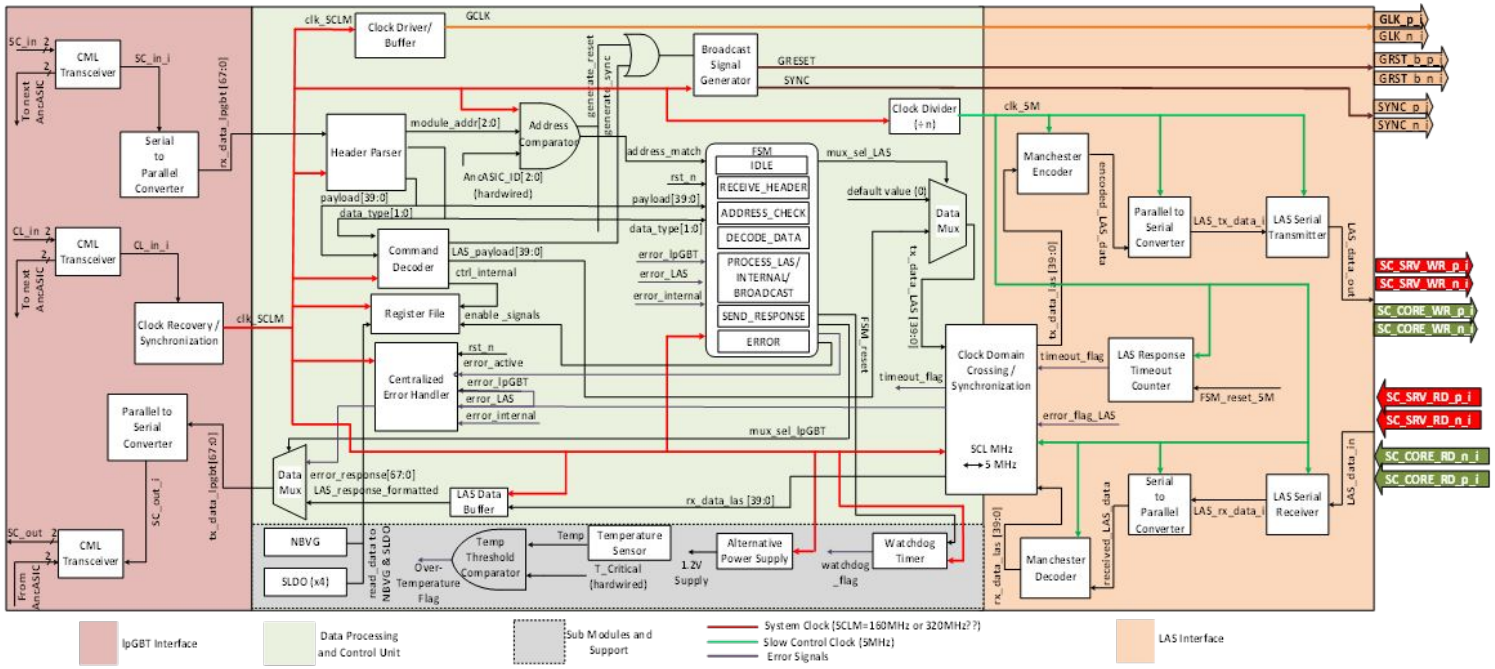
AncBrain and Hardware Mockup

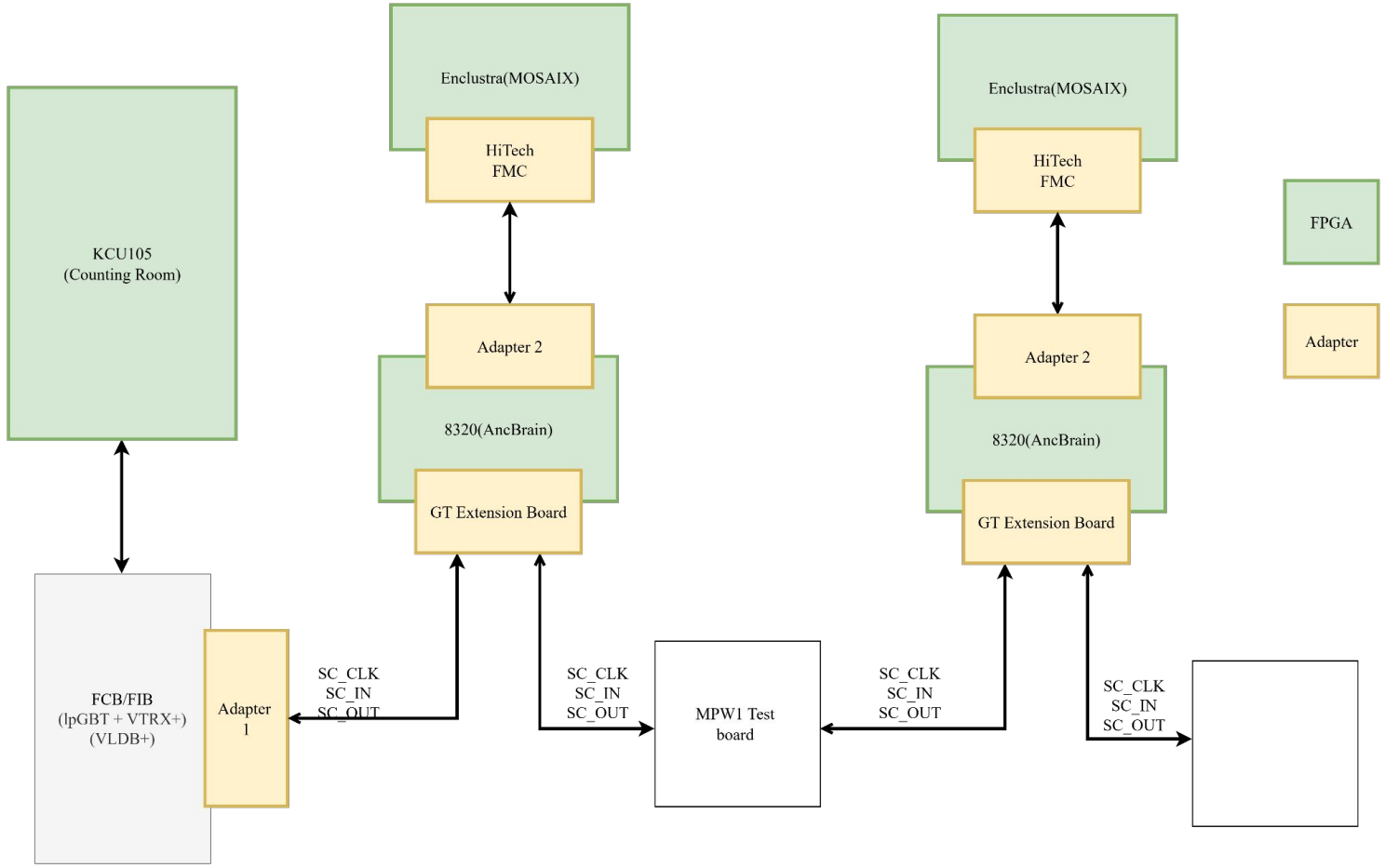


The main function of AncBrain including:

- Sub-module Control: Manages the operation of internal blocks such as the NVBG and SLDO
- Serves as a gateway, translating and forwarding communication between the lpGBT and LAS interfaces.
- Monitors critical parameters and performs necessary actions to ensure the overall stability and health of the system.

Motivation for hardware mockup:
Real-world interoperability cannot be tested in a simulated environment. Our design must reliably communicate with physical ASICs like the lpGBT and EIC-LAS, a requirement that software simulation cannot fulfill.
Furthermore. A hardware mockup reveals the true, post-implementation timing of all internal logic paths.

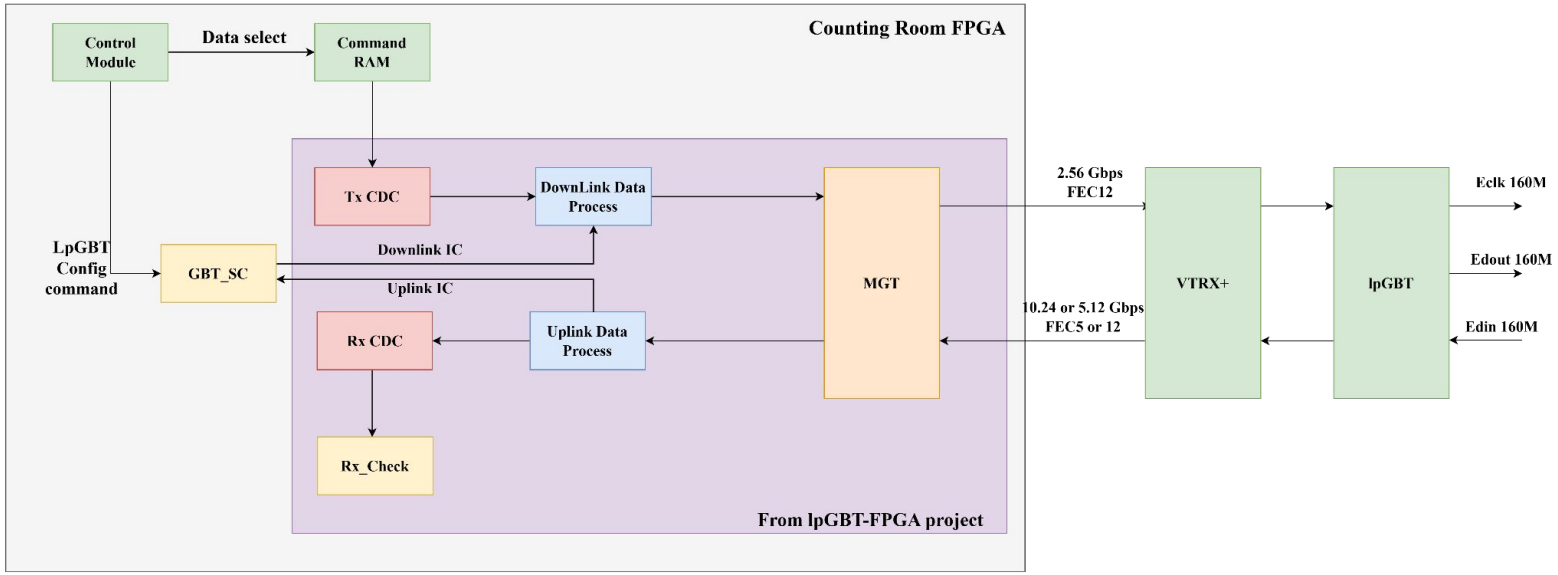
Hardware Mockup Platform



Components in system	Implementation platform
Counting Room	KCU105
FCB/FIB	VLDB+ (lpGBT, VTRX+)
AncBrain	XEM8320
EIC-LAS/MOSAIX	Enclustra AA1 SOM

- The system uses a daisy chain topology for slow control.
- The platform could potentially serve as a testbed to integrate and test
  - CML Transceiver on the MPW1
  - SLDO in MPW2
  - ER2 sensor (babyMOSAIX)
  - FPCs

Counting room FPGA + lpGBT+VTRX+



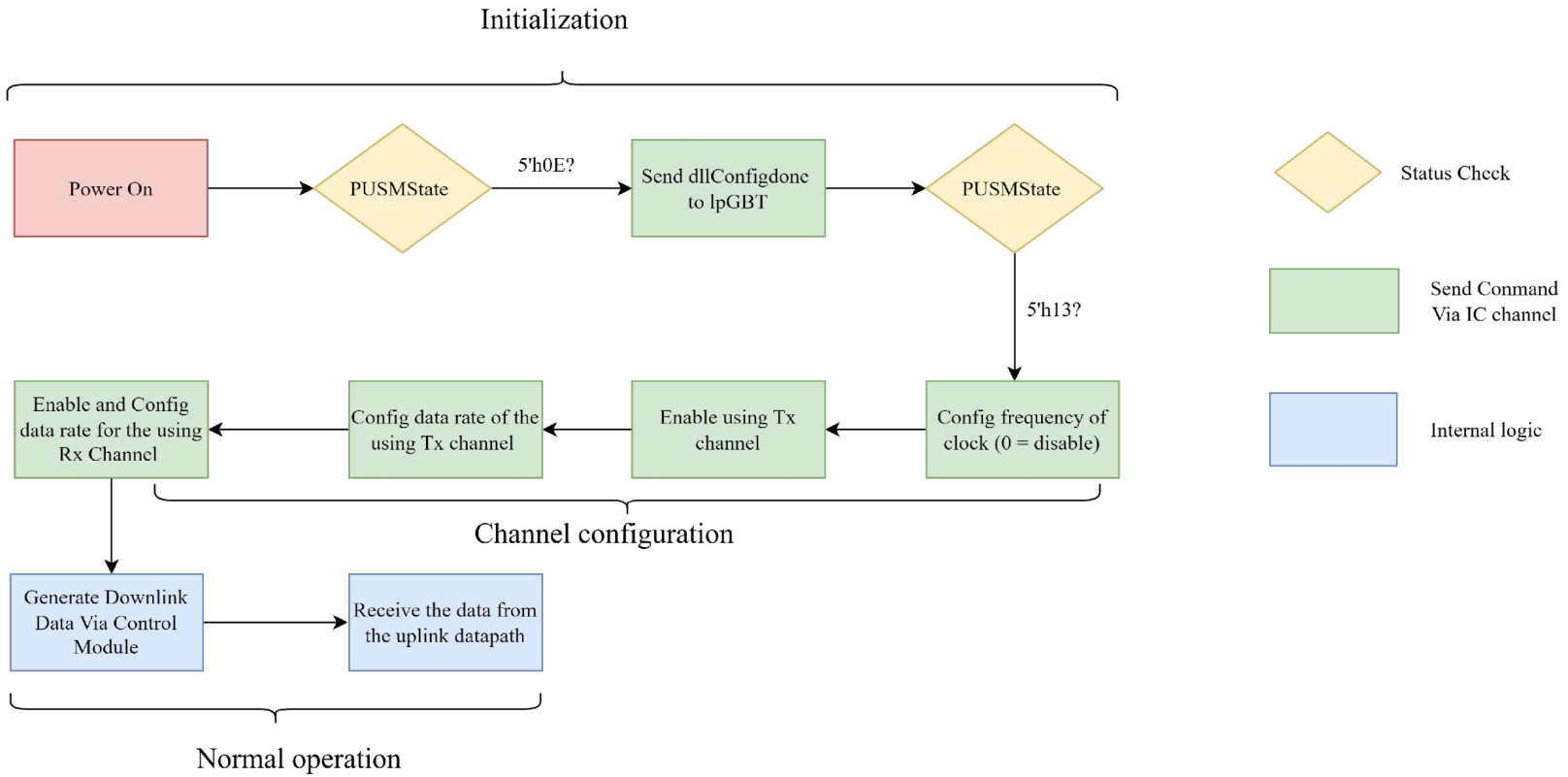
This project integrates key functionalities from lpGBT-FPGA and GBT-SC.

A Control Module and a Command RAM were added to improve overall functionality:

- **Control Module:** Uses the VIO to generate commands/data and enables for the lpGBT, routing them to their designated destinations: configuration commands to the GBT-SC and data to the Command RAM.
- **Command RAM:** The Command RAM is pre-loaded with AncBrain test commands, which are read out and sent to the Downlink Data Process module

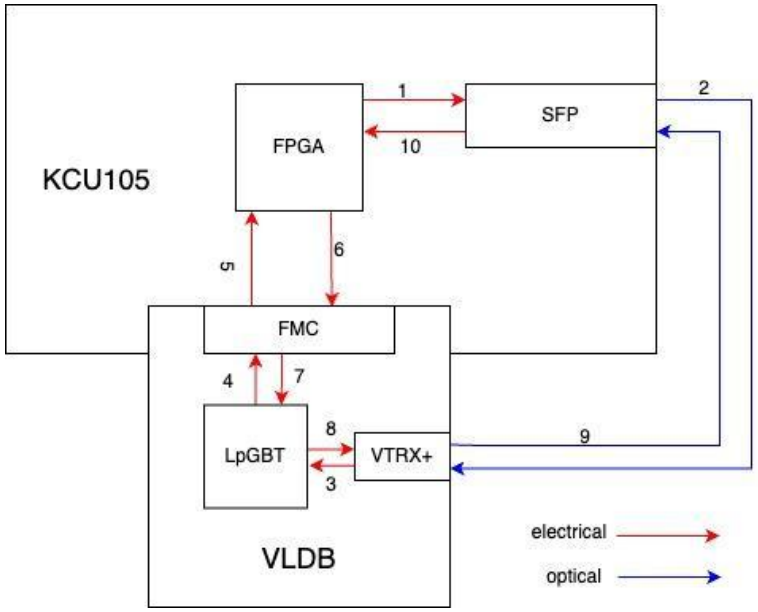
Counting room FPGA + lpGBT+VTRX+

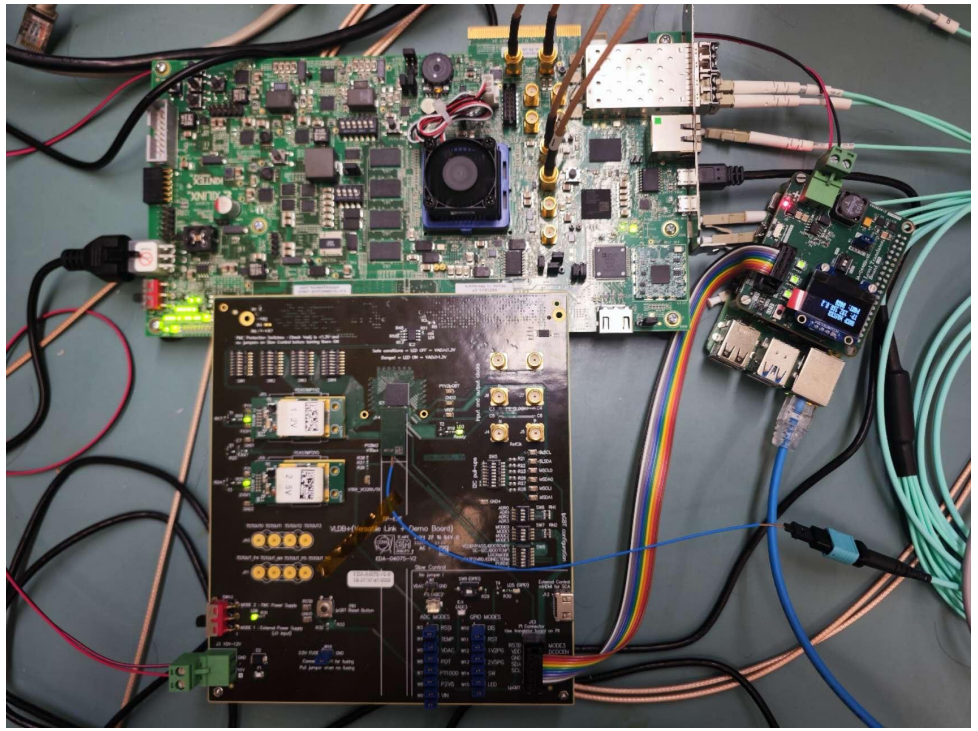
The lpGBT can be configured (initialization, I2C transaction, channel enables, and data rates settings) via the IC channel. This diagram shows an example for data transition between control room FPGA and FCB/FIB:



PUSM: Power Up State Machine
PUSMState == 5'h0E: Waiting for DLL config finish;
PUSMState == 5'13: Ready.

Counting Room FPGA



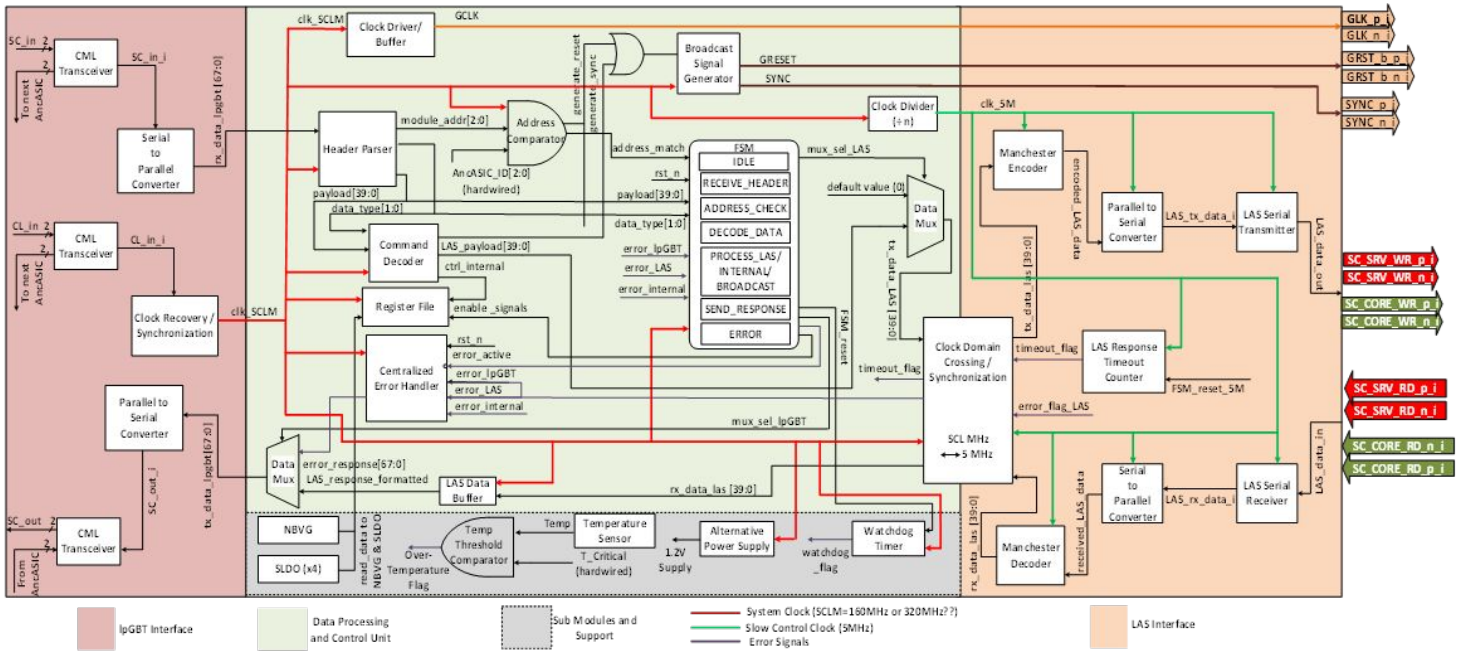


A full data path loopback test has been successfully implemented, as illustrated in the diagram. This result confirms that the initial phase (Counting Room FPGA+FCB/FIB) of our hardware test platform is operational.

Ongoing Development:

- An enhanced communication module for more flexible data and command handling.
- Implementation of high-level host interfaces, such as Ethernet in a DAQ PC.

AncBrain Mockup



This project is developed on the XEM8320 FPGA Evaluation Board.

The RTL design is adapted from the BNL AncBrain project. To adapt the design to a real physical hardware environment:

- made several fixes (e.g. adjust the FSM transition logic to take into account the latency due to non-blocking assignments);
- Developed the CDC and Manchester Encode/Decode module for LAS interface;
- Constrained the I/O and clock to generate a bitstream file.

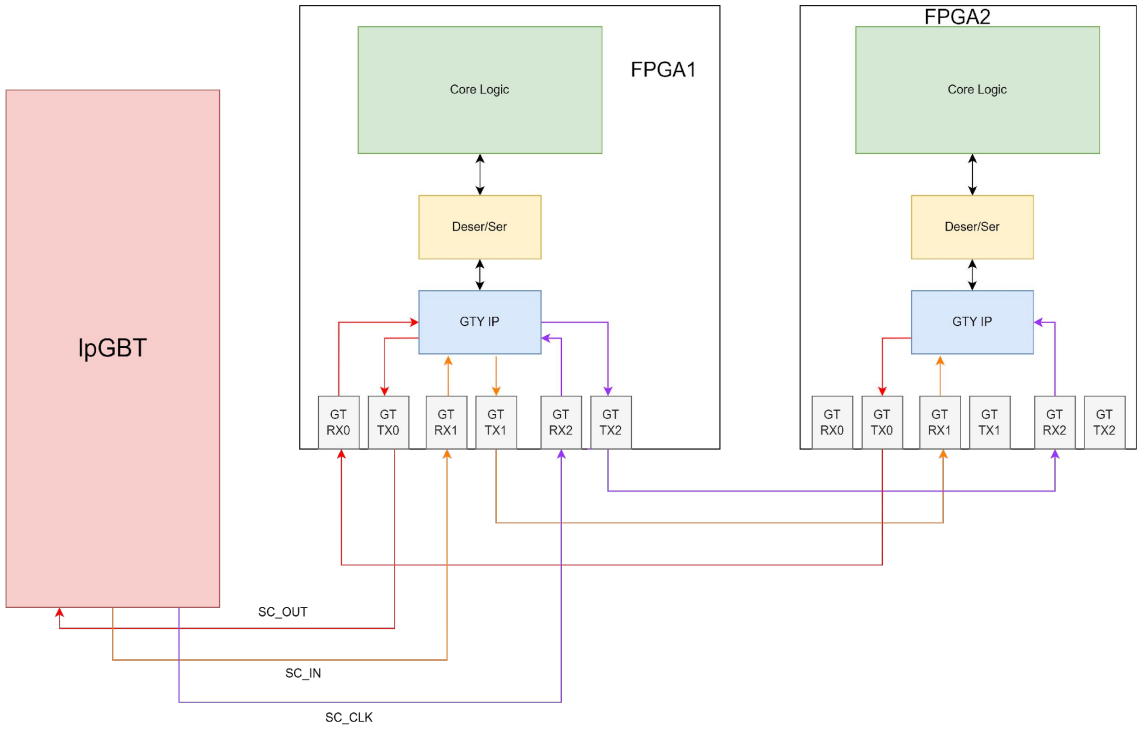
Verified Simulation Test Cases

The simulation testbench was set up to specifically validate the interaction between the **AncBrain module and a loopback module**, with the lpGBT interface inputs being driven by a shift register to generate controlled command patterns.

- **Internal Register Read/Write Test:**
  - Ensures configuration and check registers are accessible.
- **Broadcast Signal Generation Test:**
  - Verifies the correct generation and timing of broadcast signals.
- **Error Injection and Handling Tests:**
  - Validated the design's robustness against various induced errors, including:
    - CRC Errors
    - Parity Errors
    - Missing EOF or SOF
    - Address Errors
- **Interface Verification with the LAS Emulator:**
  - Verified the firmware's response processing logic by utilizing a loopback module that intentionally delays the returned data.

To-do:
Perform simulations with the integrated MOSAIX emulator module.
Complete and expand the Error Injection test suite.

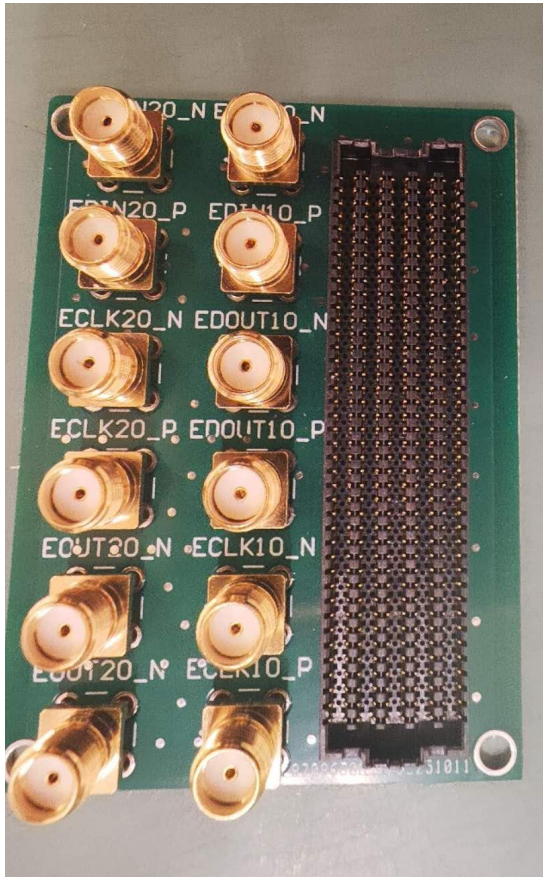
Daisy-chain for Slow Control



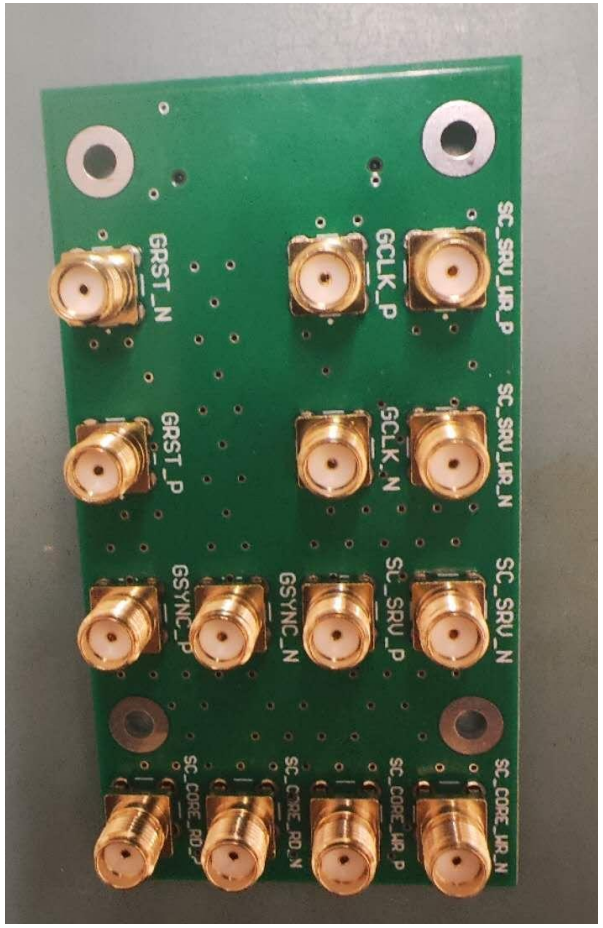
This diagram illustrates a two-AncBrain daisy-chain configuration for which the data communication link has been successfully tested and confirmed.

Similar to the CML (Current-Mode Logic) Transceiver in the AncBrain, the FPGA's on-chip GTY transceivers also operate based on the CML standard, which could provide a hardware-level approximation for testing key aspects of the signal standard, such as DC vs. AC coupling.

Customized Adapter Boards



Adapter1:
Female FMC to SMA,
This adapter serves as a breakout board for the lpGBT, exposing the EDIN, EDOUT, and ECLK signals from e-link channel 10 and 20.



Adapter2:
SYZYGY to SMA,
This board serves as a dedicated breakout for the AncBrian Mockup (XEM8320)'s LAS interface, exposing its core signals: CORE, SRV, GRST, GCLK, and GSYNC.

Summary and Outlook

Component	Hardware Platform	Current Status	Completed Milestones	Next Steps
Counting Room FPGA	KCU105	In Progress	Verified operational build on KCU105; Dataloop test between lpGBT and FPGA has passed.	Developing more flexible data and command transmitted module Implementation of high-level host interfaces, such as Ethernet
FCB/FIB	VLDB+	Existing		
AncBrain	XEM8320	In Progress	Verified core functionality in RTL simulation; Bitstream generated for target device.	Complete the simulation; On Board test; Aligning the FPGA Design with the BNL Roadmap
EIC-LAS/ MOSAIX	Enclustra AA1 SOM	Not started	Obtained FPGA kits, access to MOSAIX emulator and test system FW/SW	Setup the MOSAIX emulator based on Enclustra SOM
Adapter board		Completed		

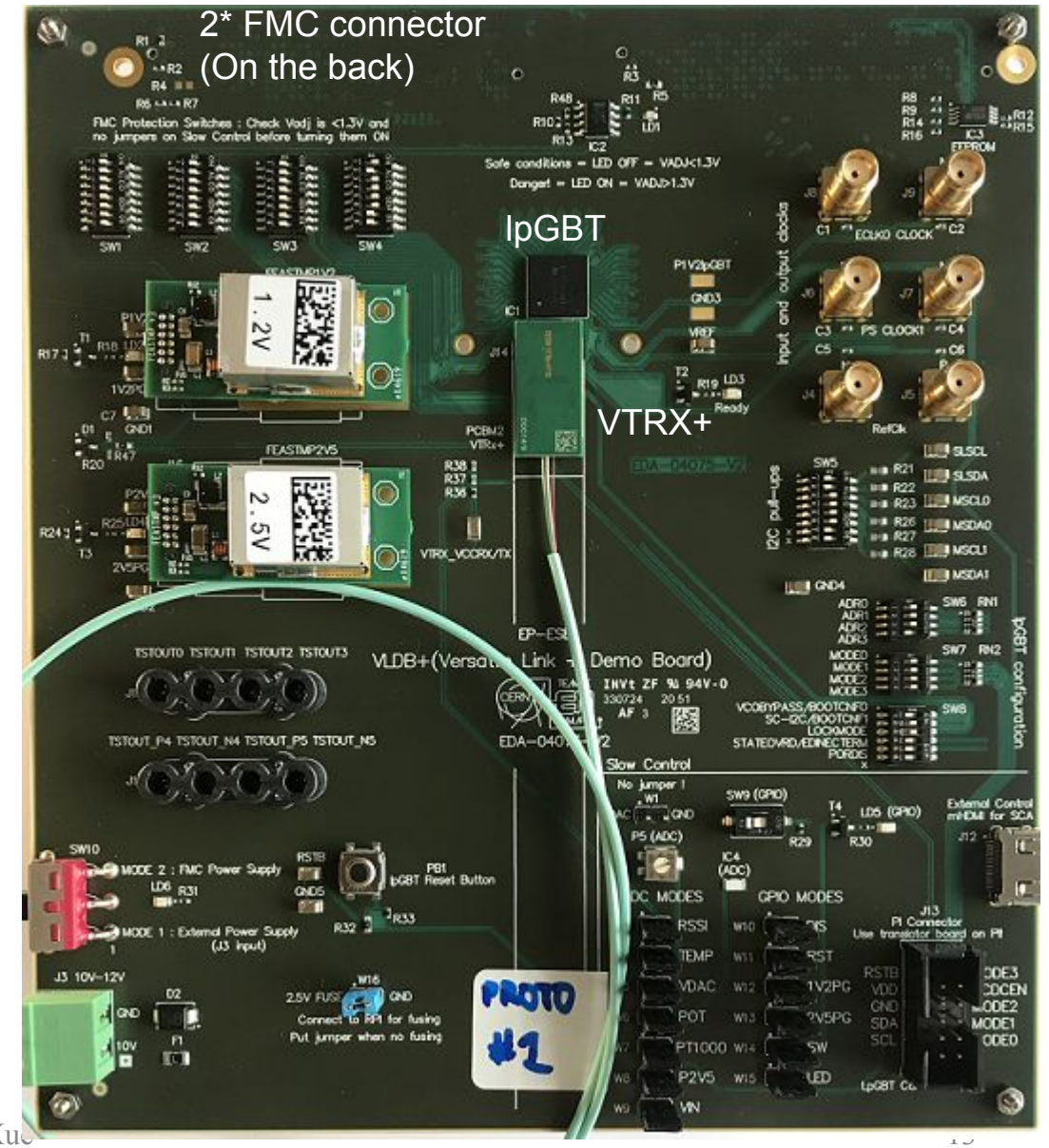
Thank you

Back up VLDB+

- The Low Power Giga Bit Transceiver (lpGBT) is a radiation tolerant ASIC used to implement high speed bidirectional optical links for high-energy physics experiment;
- Versatile Transceiver-plus (VTRx+) is an optical link module for data transmission;

- lpGBT and VTRx+ are planned to be used for AncASIC and AC-LGAD;
  - In outer barrel and Disk area of SVT, lpGBT will receive command from control room, and it will **initiate communication and send control commands** to AncASIC;
  - For AC-LGAD, lpGBT is planned to be used in **slow-control & data transmission**.

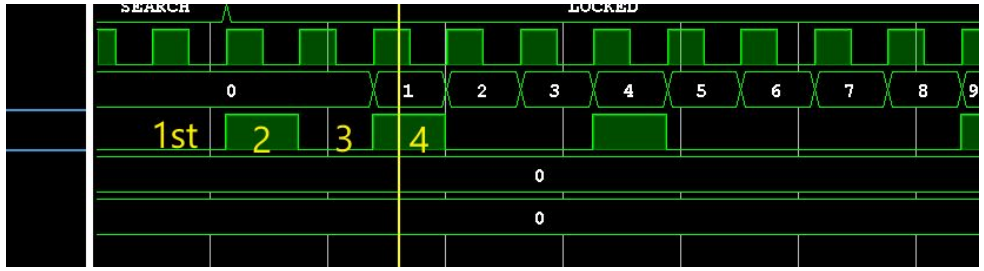
- The VLDB+ is a board designed to provide an evaluation kit for lpGBT, with the VLDB+, we can:
  - get familiar with the lpGBT
  - test our custom front-end system communication to the lpGBT



Back up non-blocking assignments

```
51  always_ff @(posedge clk or negedge rst_n) begin
52      if (!rst_n) begin
53          shift_reg    <= '0;
54          cmp_reg      <= '0;
55          word_reg     <= '0;
56          word_valid_q <= 1'b0;
57          sof_locked_q <= 1'b0;
58          state        <= SEARCH;
59          bit_cnt      <= 7'd0;
60          loss_cnt     <= 4'd0;
61          resync_pulse_q <= 1'b0;
62      end else begin
63          // slide compare window first for fastest path
64          cmp_reg   <= {cmp_reg[0], sc_in_bit_i};
65          shift_reg <= {shift_reg[63:0], sc_in_bit_i};
66
67          state     <= next;
68          loss_cnt  <= next_loss_cnt;
69          sof_locked_q <= (next == LOCKED);
70
71          // bit counter active only when locked
72          if (state == LOCKED) begin
73              bit_cnt <= (bit_cnt == 7'd62) ? 7'd0 : bit_cnt + 1'b1;
74          end else begin
75              bit_cnt <= 7'd0;
76          end
```

```
        word_valid_q <= 1'b0;                // default clear
        if (state == LOCKED && bit_cnt == 7'd62) begin
            // capture the complete 65-bit word (shift_reg already contains all 65 bits)
            word_reg     <= shift_reg; // shift_reg contains the complete 65-bit frame
            word_valid_q <= 1'b1;     // pulse for 1 clk
        end
    end
end
```



Bit_cnt started to count when state == LOCKED

⇒ When bit_cnt = 62, the package receiving finished. Word_valid should be high. bit_cnt =64 is too late.