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SVT DAQ & Slow Controls

J. Schambach

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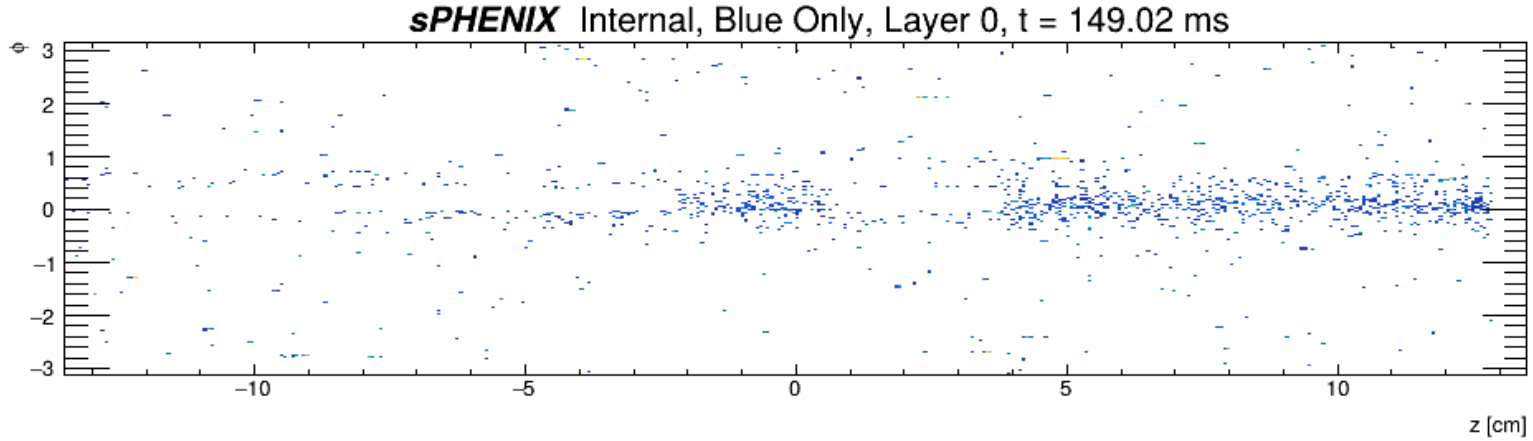
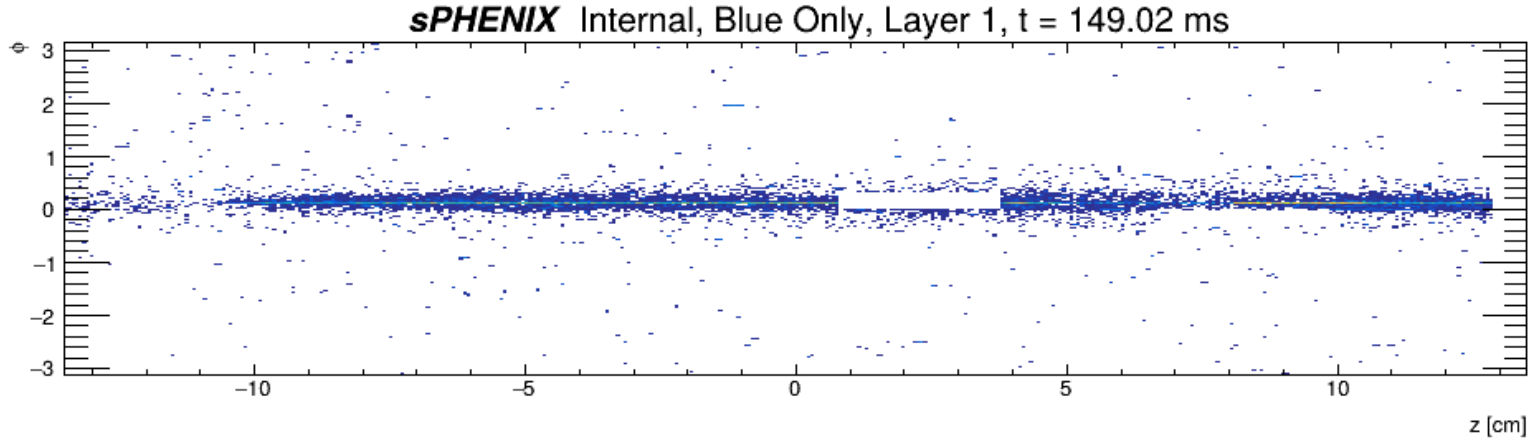
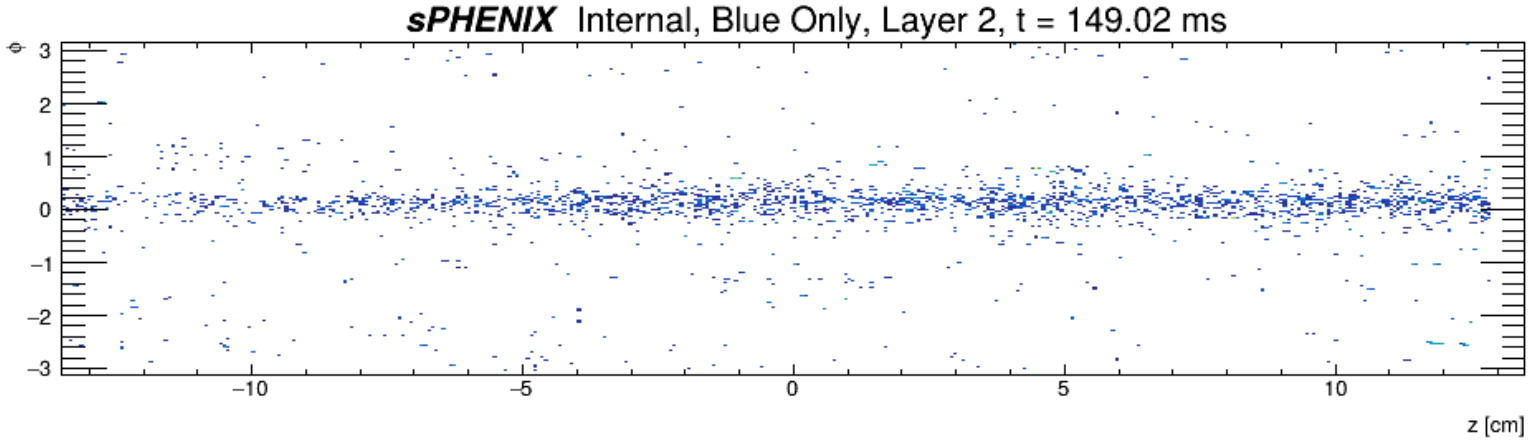
U.S. DEPARTMENT OF ENERGY

Select hit maps from sPHENIX MVTX

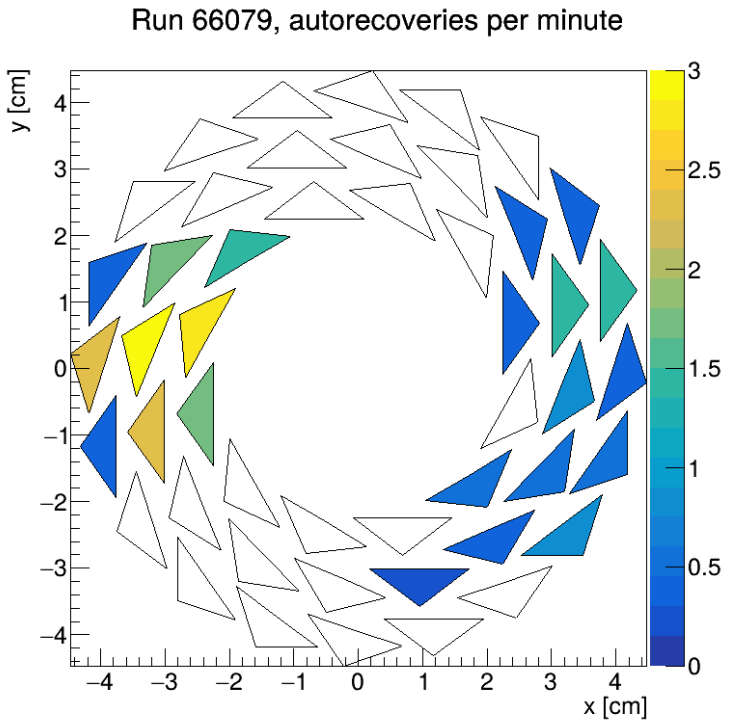
- Z is along beam axis (-z is south or incoming blue)
- Phi is around MVTX (phi = 0 is outside of the ring)



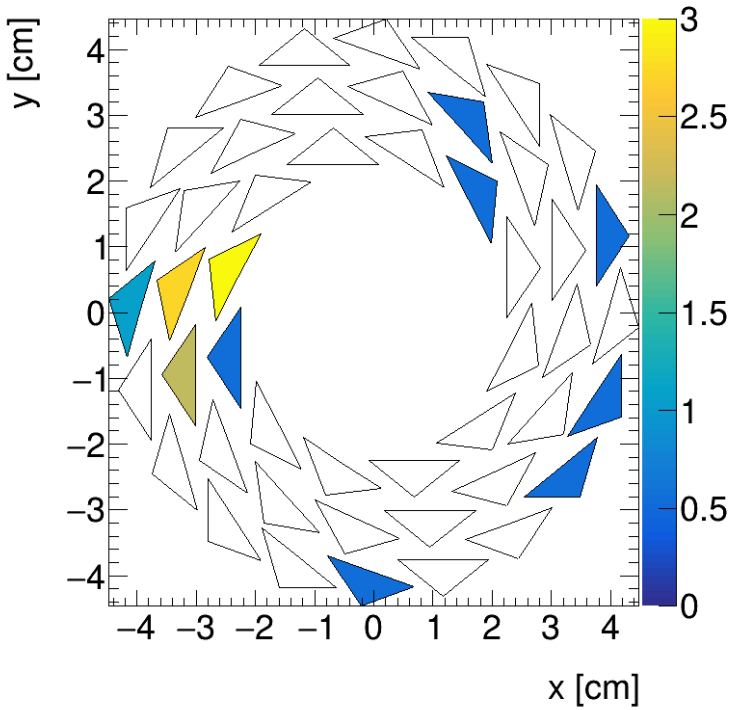




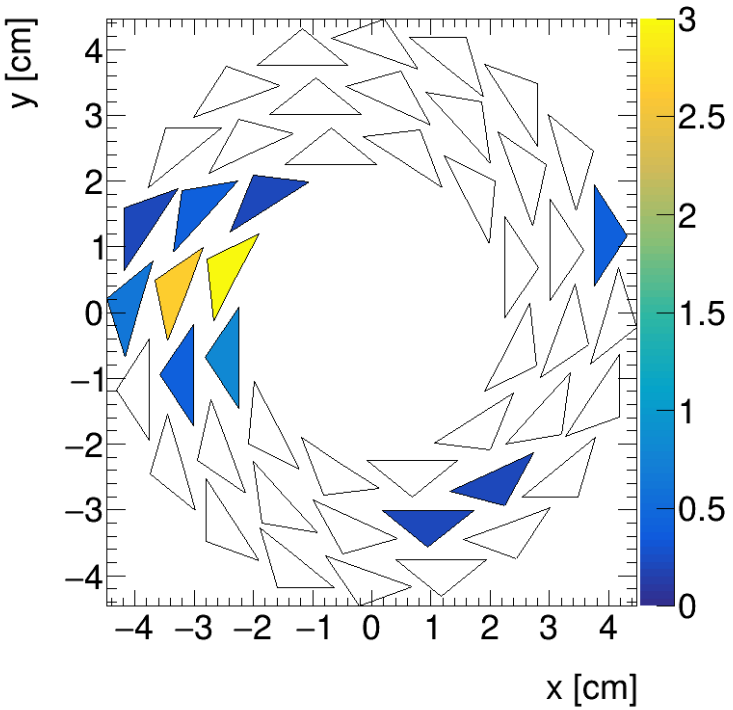
Auto-recovery rate per stave



Streamed



16 kHz trigger



11 kHz trigger

- Plots from Michael Peters
- Autorecovery takes ~ 20s. Max rate per stave is ~ 3

MOSAIX Documentation

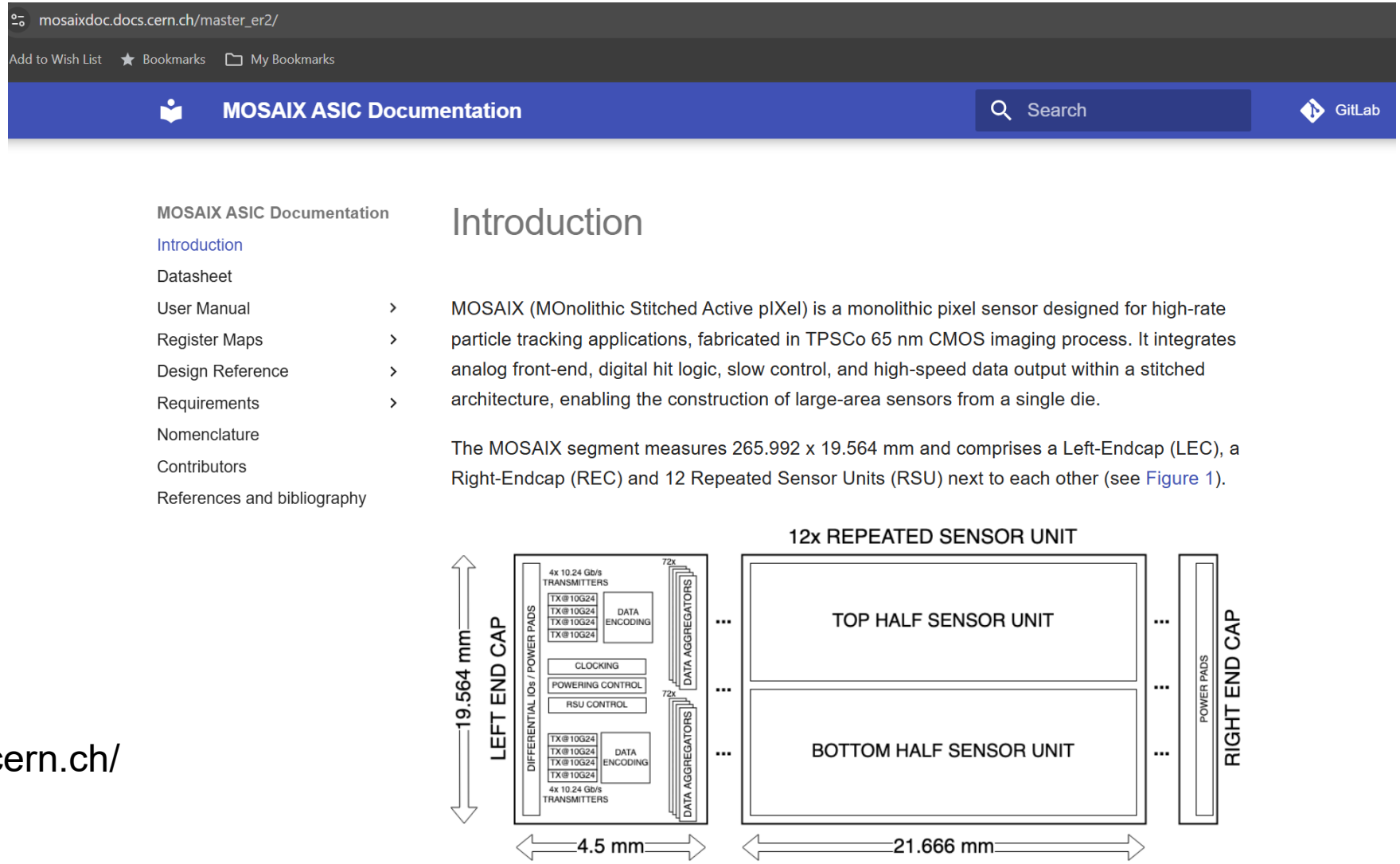


Figure 1: *Top level block diagram of the MOSAIX chip, one segment of larger sensors.*

https://mosaixdoc.docs.cern.ch/

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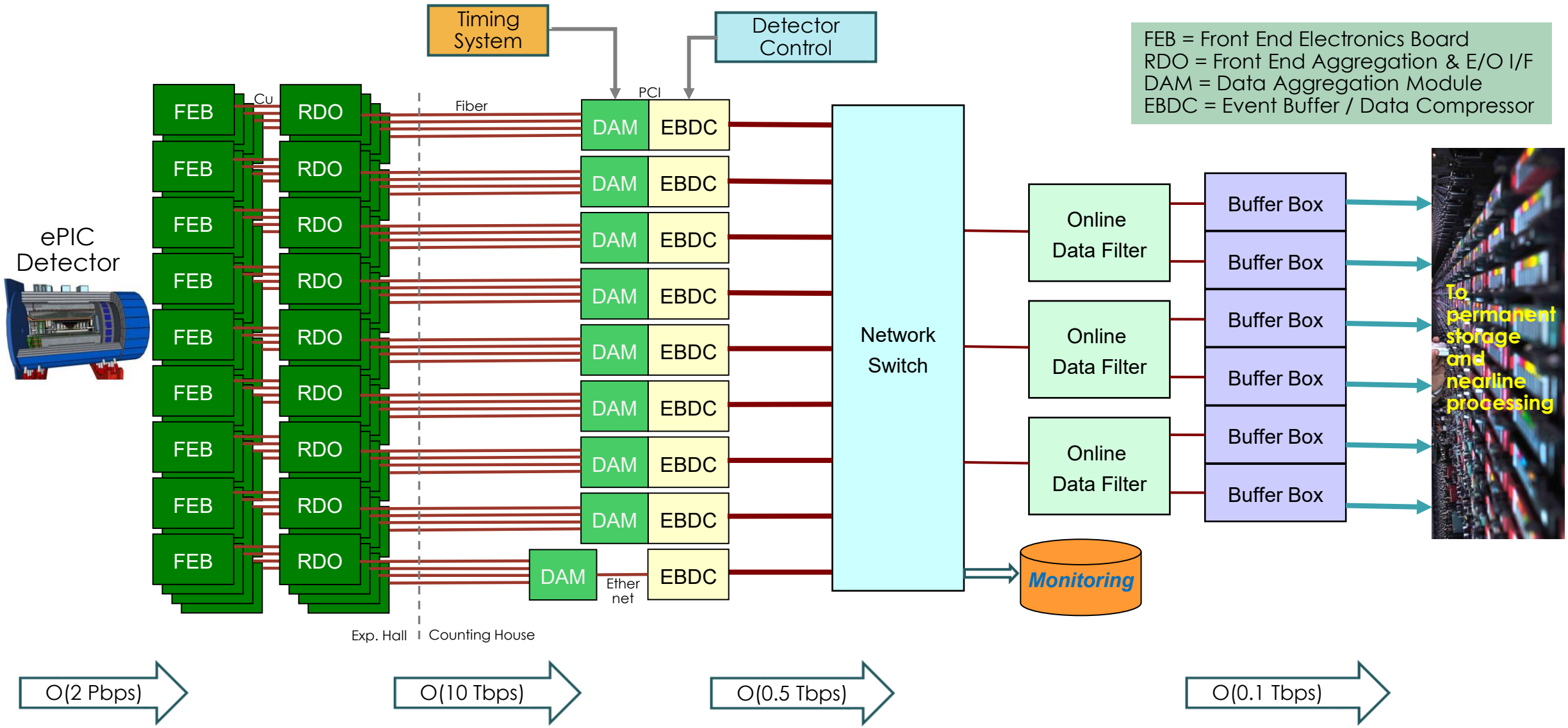
ePIC Streaming DAQ



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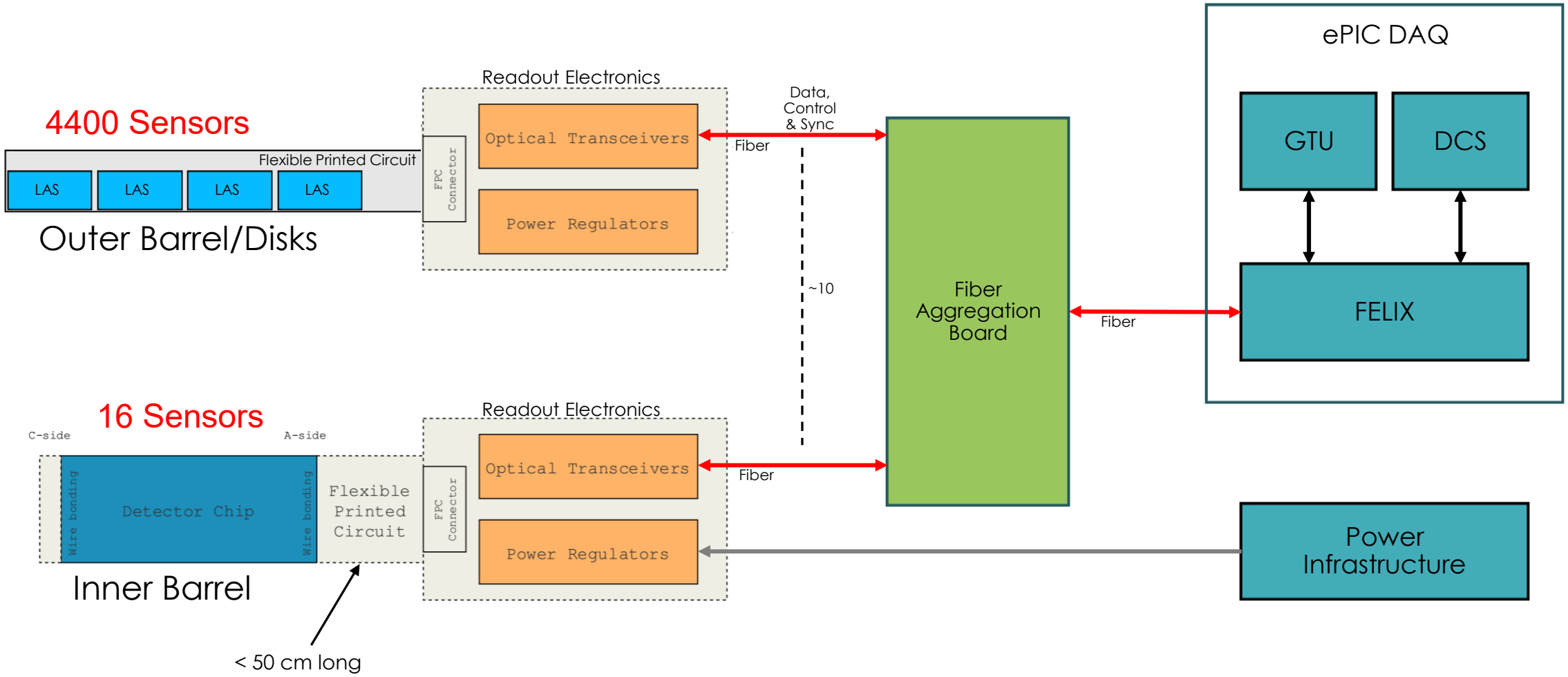
SVT Electronics – Simplified Overview



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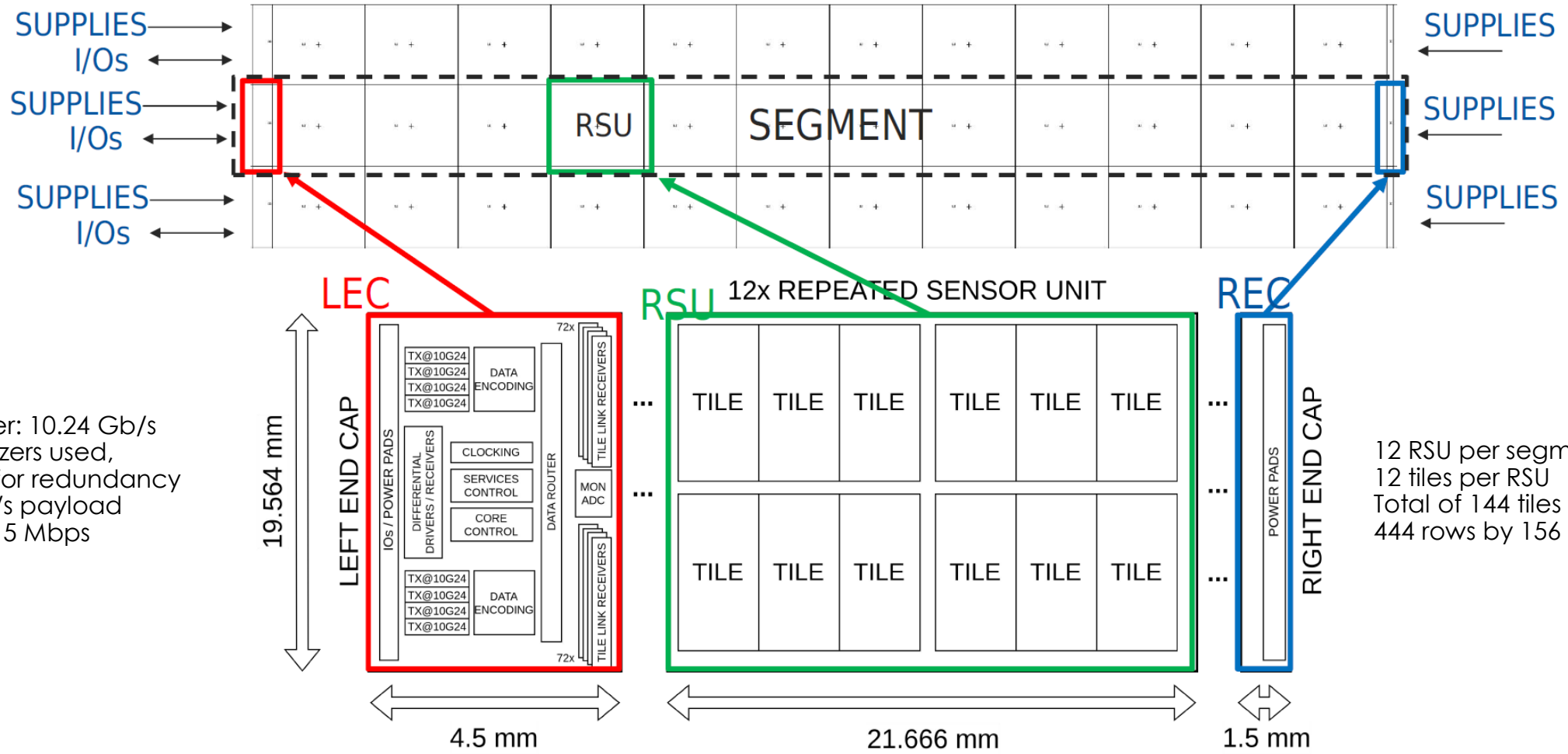
MOSAIX Architecture



Serializer: 10.24 Gb/s
3 serializers used,
others for redundancy
7.6 Gb/s payload
DCS at 5 Mbps

12 RSU per segment
12 tiles per RSU
Total of 144 tiles per segment
444 rows by 156 columns per tile

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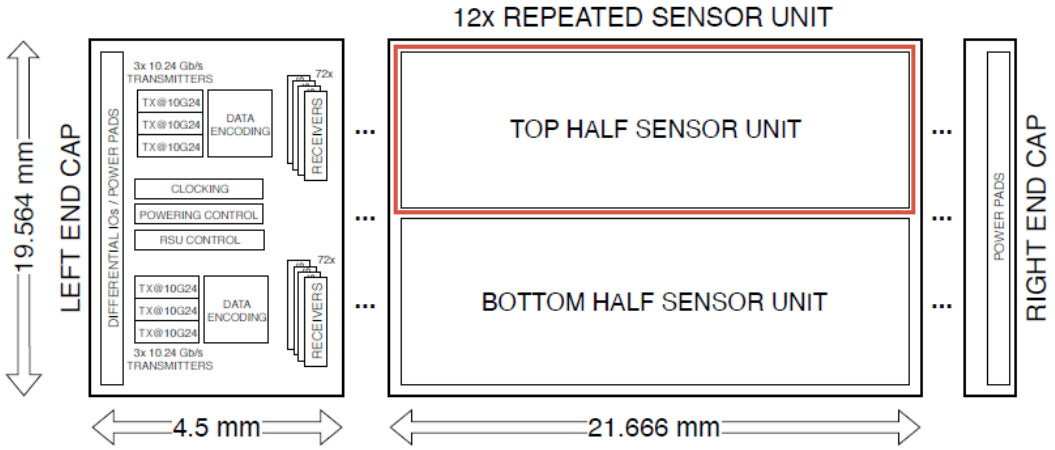
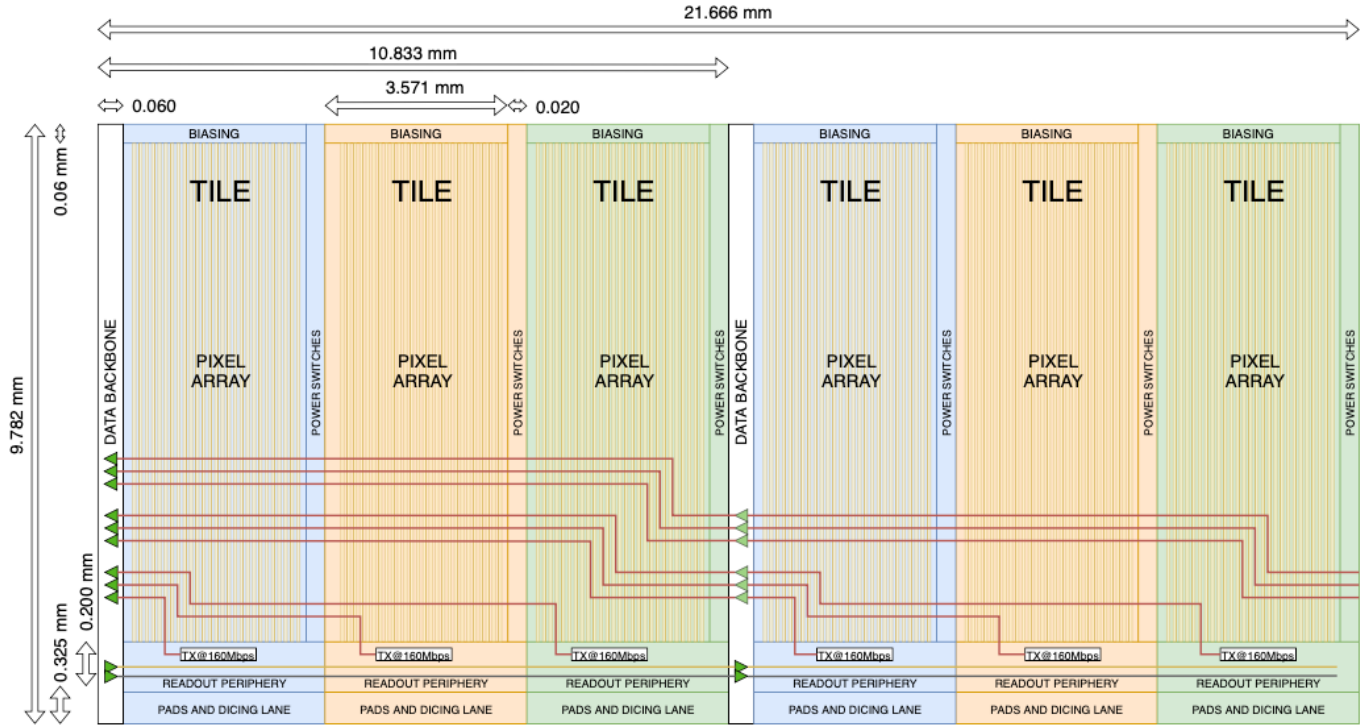
Half Repeated Sensor Unit



Each Half Unit is segmented in **Tiles** (Domains)

Each **tile** acts as an
independent sensor
Separate Local Power
Configuration
Readout Link (160 Mb/s)
Each **Tile** data output has
direct connection to the **left endcap**



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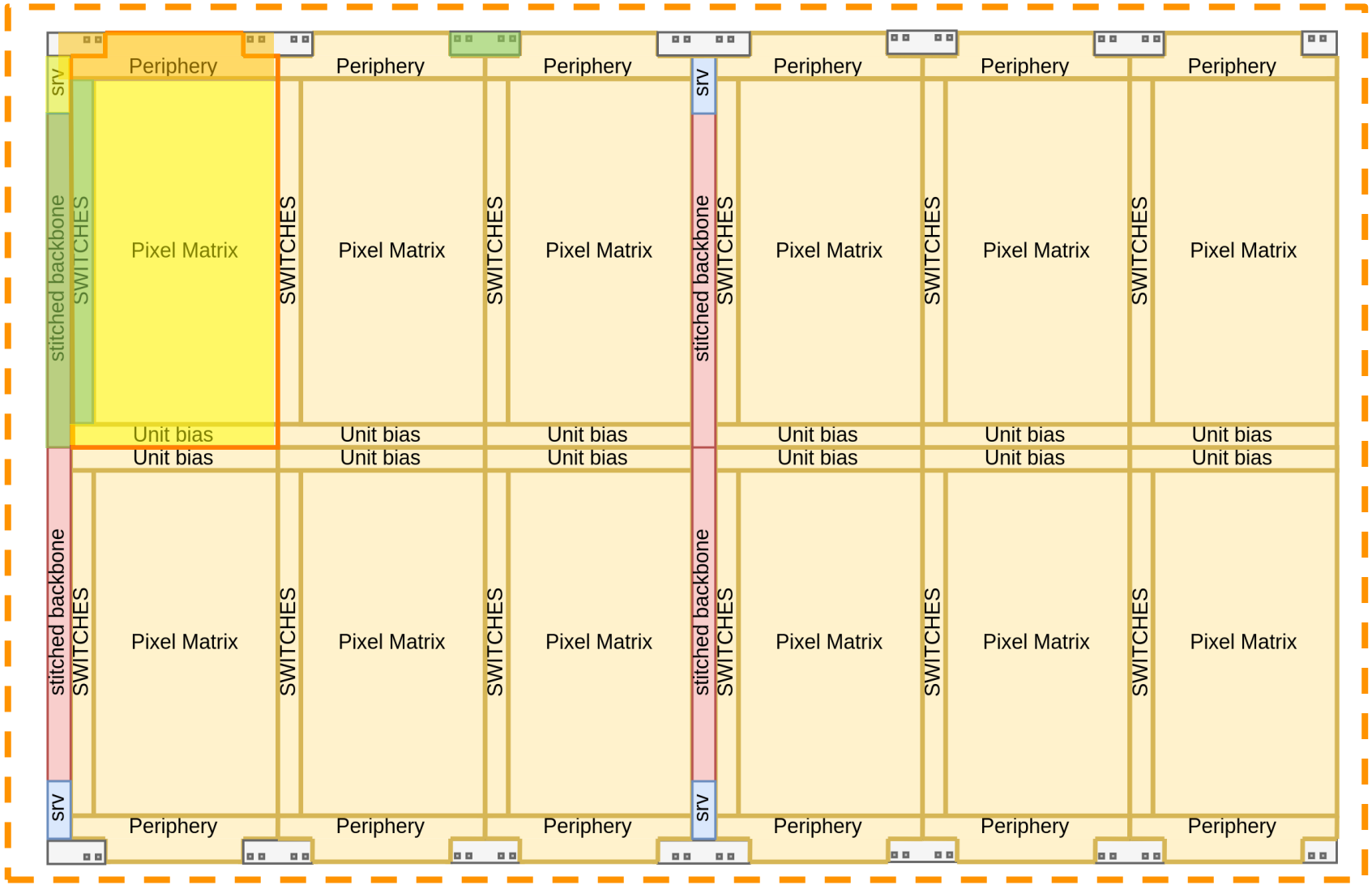
RSU

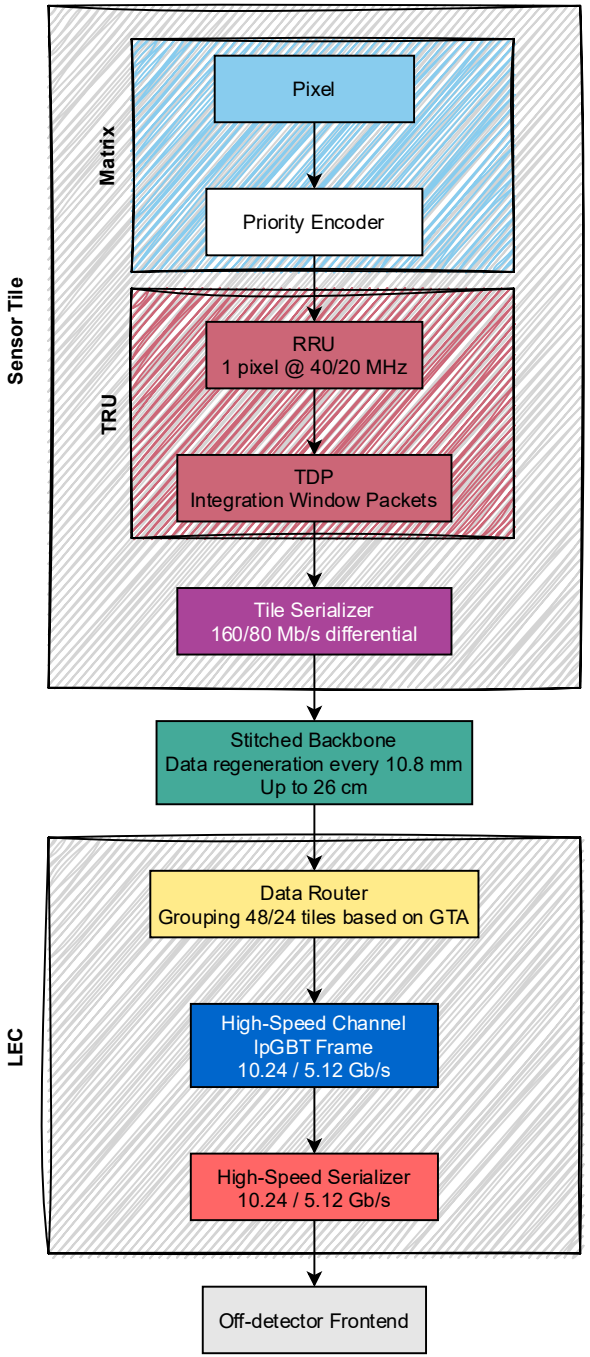
RSU INTEGRATION



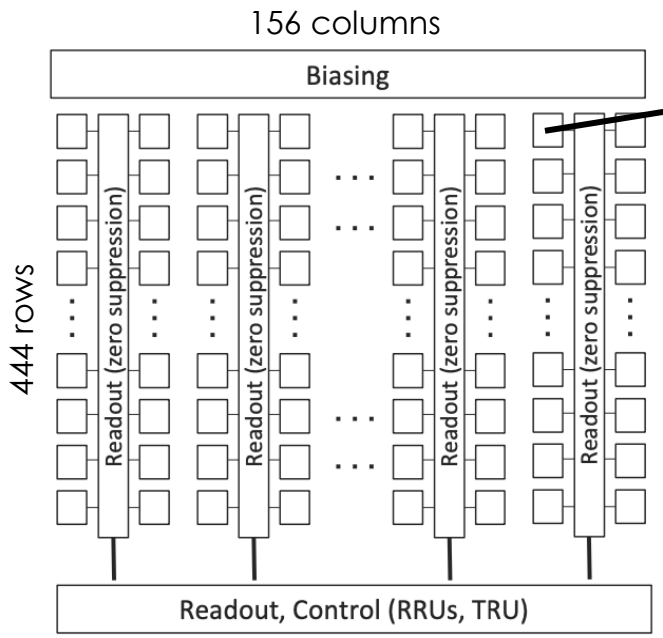
Interface Signals

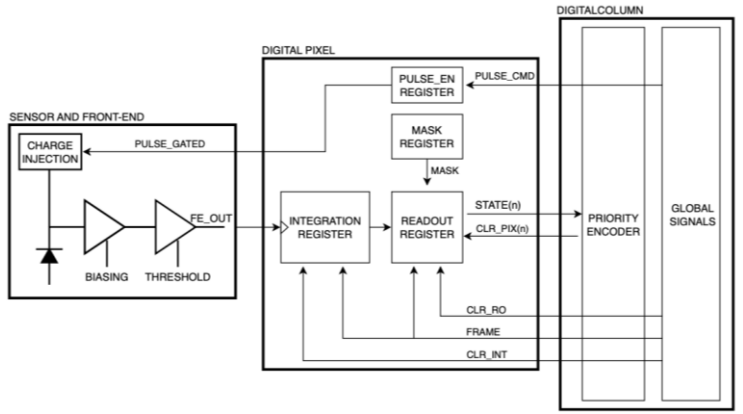
Name	Type	Coupling	Direction	Purpose
GCLK_(P/N)	Differential (CLPS)	AC or DC	Input	Global clock input
GRST_B_(P/N)	Differential (CLPS)	AC or DC	Input	Global reset input (active low)
SYNC_(P/N)	Differential (CLPS)	AC or DC	Input	Synchronization signal input
SC_SRV_WR_(P/N)	Differential (CLPS)	AC or DC	Input	Slow control service management write input
SC_SRV_RD_(P/N)	Differential (CLPS)	AC or DC	Output	Slow control service management read output
SC_CORE_WR_(P/N)	Differential (CLPS)	AC or DC	Input	Slow control core management write input
SC_CORE_RD_(P/N)	Differential (CLPS)	AC or DC	Output	Slow control core management read output
HSDATATOP_(P/N)[0]	Differential	AC	Output	High-speed data output
HSDATATOP_(P/N)[1]	Differential	AC	Output	High-speed data output
HSDATATOP_(P/N)[2]	Differential	AC	Output	High-speed data output
HSDATATOP_(P/N)[3]	Differential	AC	Output	High-speed data output
HSDATABOT_(P/N)[0]	Differential	AC	Output	High-speed data output
HSDATABOT_(P/N)[1]	Differential	AC	Output	High-speed data output
HSDATABOT_(P/N)[2]	Differential	AC	Output	High-speed data output
HSDATABOT_(P/N)[3]	Differential	AC	Output	High-speed data output
TEST_OUT_TOP_(P/N)	Differential (CLPS)	AC or DC	Output	Test signal output
TEST_OUT_BOT_(P/N)	Differential (CLPS)	AC or DC	Output	Test signal output
ADC_CALIB[0]	Analog	DC	In/Out	ADC reference
ADC_CALIB[1]	Analog	DC	In/Out	ADC calibration

Data Flow


Sensor Tile
Matrix
Pixel
Priority Encoder
TRU
RRU
1 pixel @ 40/20 MHz
TDP
Integration Window Packets
Tile Serializer
160/80 Mb/s differential
Stitched Backbone
Data regeneration every 10.8 mm
Up to 26 cm
LEC
Data Router
Grouping 48/24 tiles based on GTA
High-Speed Channel
lpGBT Frame
10.24 / 5.12 Gb/s
High-Speed Serializer
10.24 / 5.12 Gb/s
Off-detector Frontend

Tile Architecture



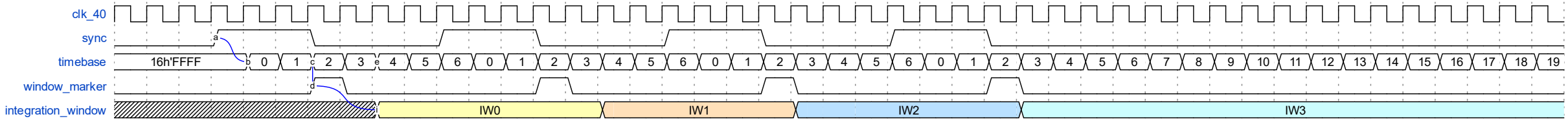


444 x 156 pixels / tile
831168 pixels per RSU
144 domains / segment
9.974 Mpixels / segment

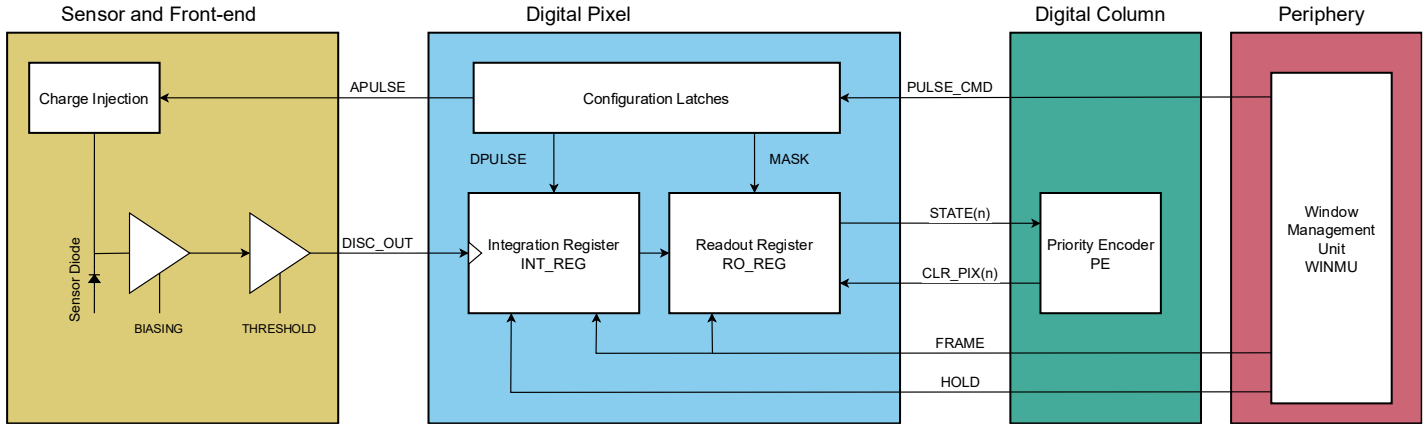
In pixel:

- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- Digital pulsing
- Masking

Pixel Integration Windows



Timing diagram showing how integration window are generated following a sync pulse and a window marker. In this particular case, the Window Marker Latency is set to two, and thus is asserted when the internal timebase equals 2. Notice, that with an absence of new sync pulses, the timebase continues to increment and the integration window remains active.



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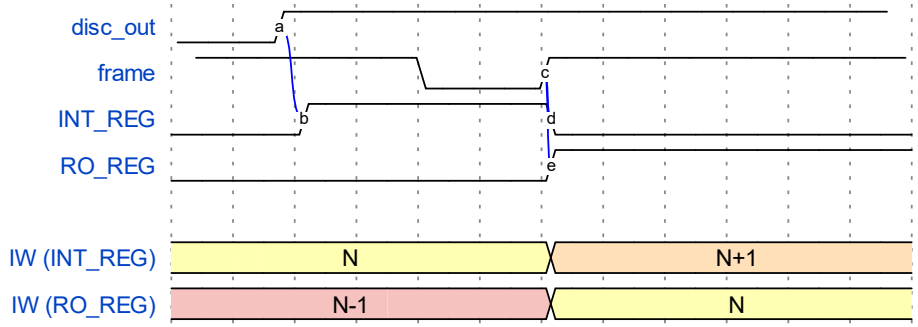
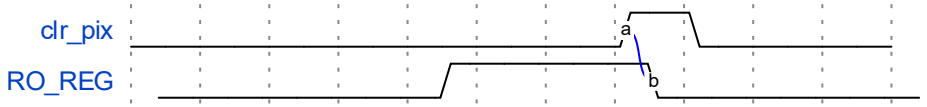
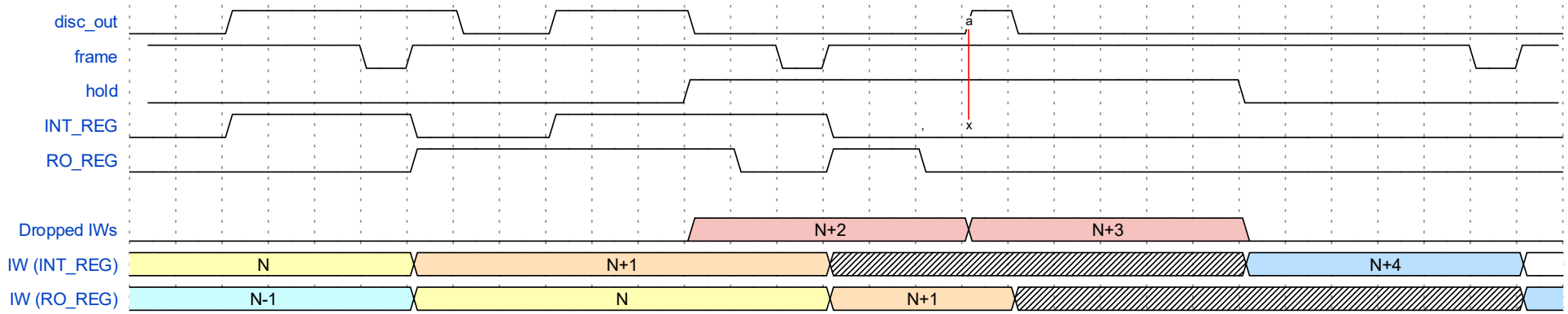
Timing for Pixel Readout





When RO_REG is finished being read out

When the RRU hasn't emptied all RO_REG entries by the end of an integration window, WINMU asserts hold until it has read out all the data.



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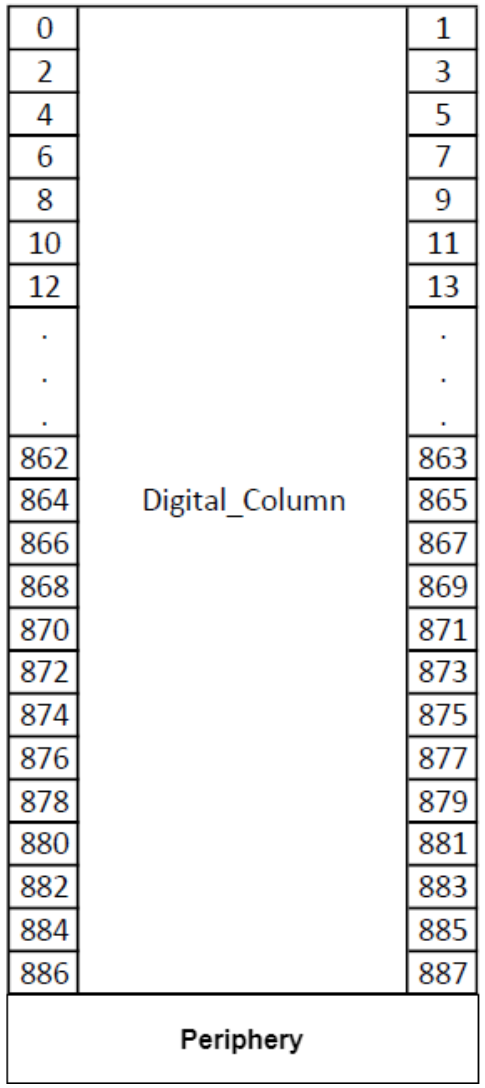
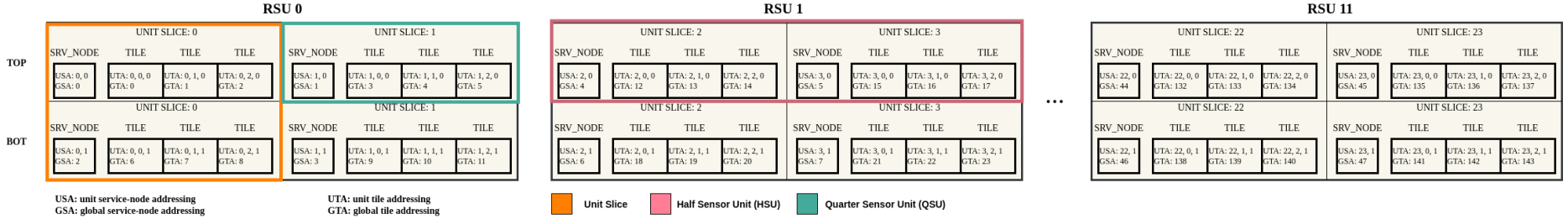
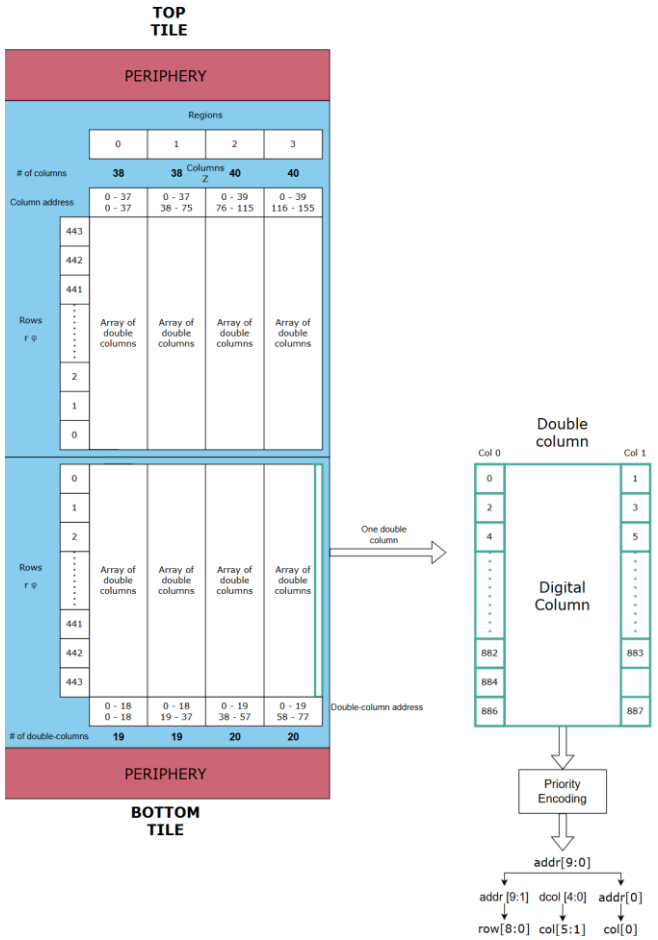
Tile and Pixel Address Encoding



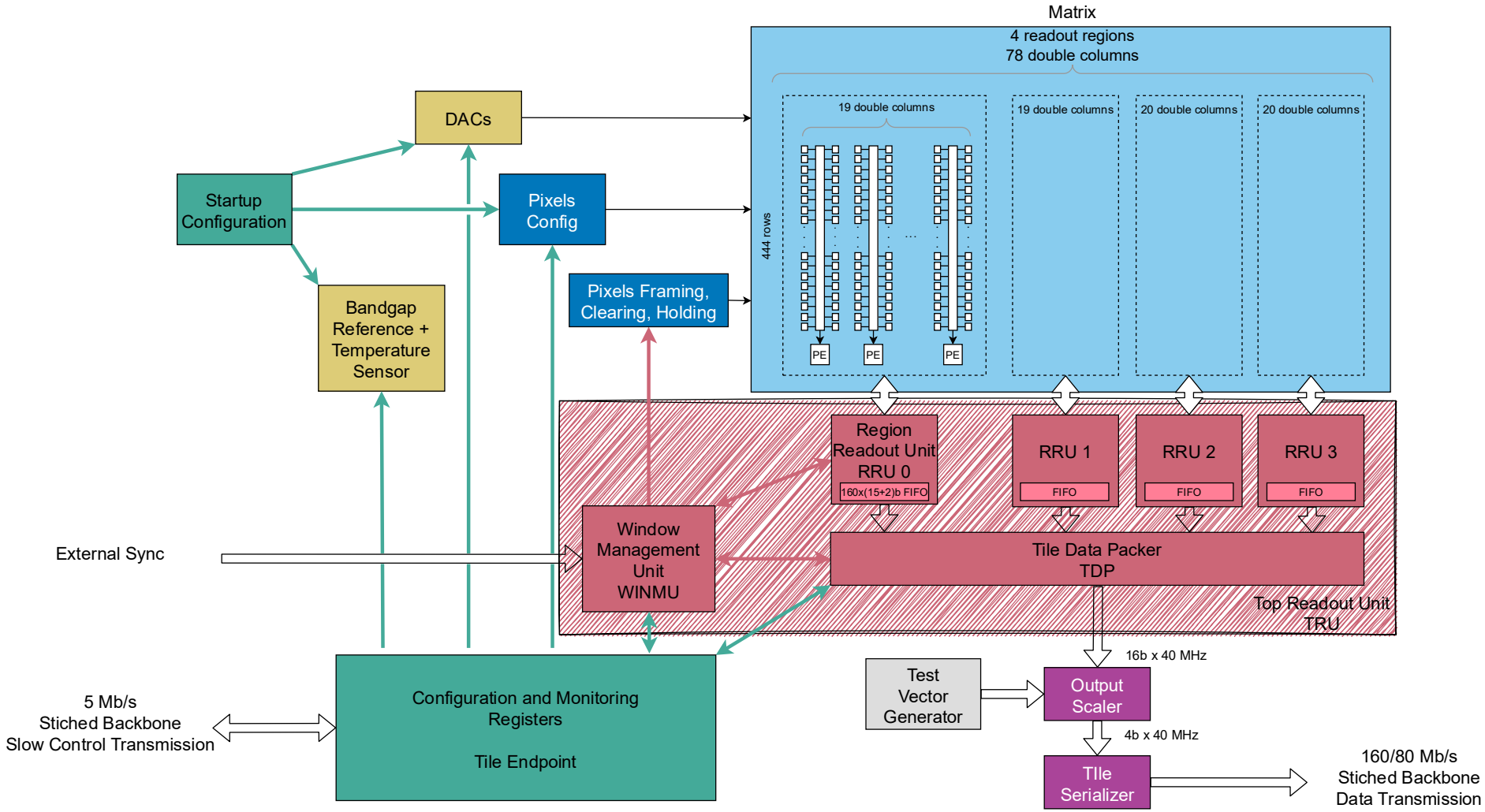




5 bits for unit slice (0 – 23)
2 bits for tile within unit_slice (0 – 2)
1 bit for t_b (top = 0, bottom = 1)

- Row (rϕ): 9 bits, provided in full by the Priority Encoder
- Column (Z): 8 bits total, split between:
  - Region Header: upper 2 bits (0–3)
  - Priority Encoder output: lower 6 bits (0–40)

Tile Readout Conceptual Block Diagram



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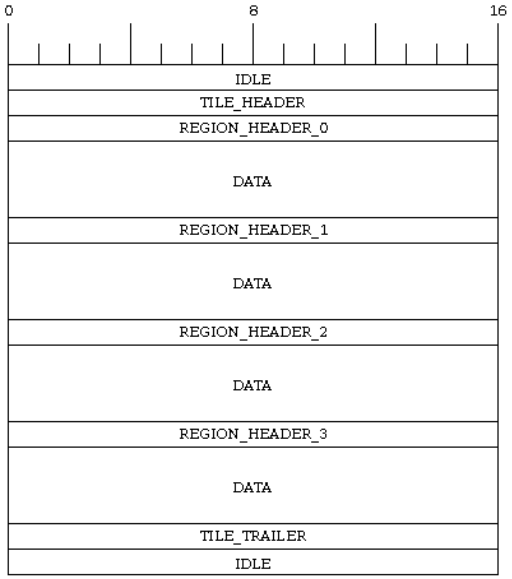
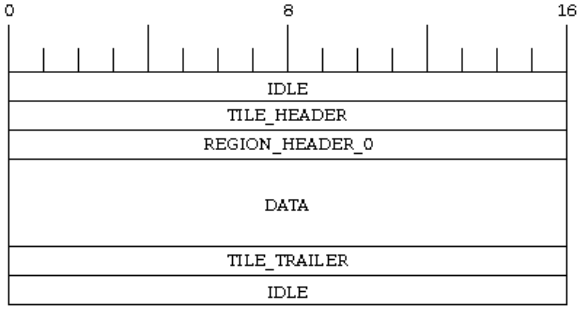
Readout Protocol

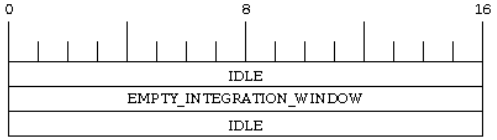
Hits in all 4 regions



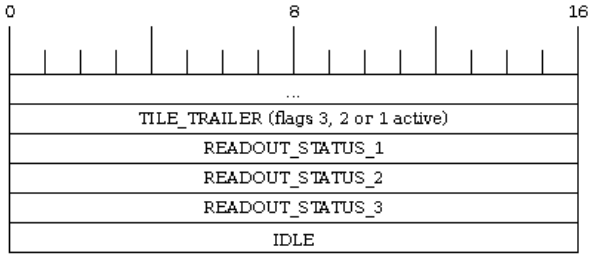
Hits in 1 region



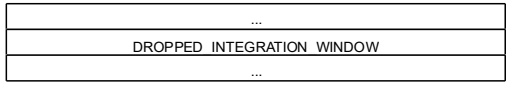
No hits



Status



Dropped IW Packet



READOUT PROTOCOL

Word type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]							
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]							
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]							
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]				Integration Window Counter [7:0]							
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]					Tile [1:0]		T/B
REGION_HEADER	1	0	1	0	1	1	Region Address.		Integration Window Counter [7:0]							
DATA	0	Pixel Address Row [8:0]									Pixel Address Column [5:0]					
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]				Packet Checksum [7:0]							
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
RECOVERY	1	0	0	1	0	0	1	1	'0							
RESERVED	1	0	0	0	RESERVED											

Text is not SVG - cannot display

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Bit Counts

1 tile noise pixel:
- 1 tile header
- 1 region header
- 1 data
- 1 tile trailer

4 words
-> 64 bits per pixel

1 tile hit (4 pixels):
- 1 tile header
- 1 region header
- 4 data
- 1 tile trailer

7 words
->112 bits
-> 28 bits per pixel

1 hit (4 pixels) per region:
- 1 tile header
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 tile trailer

22 words
-> 352 bits
-> 22 bits per pixel

2 hits (4 pixels) in 1 region:
- 1 tile header
- 1 region header
- 8 data
- 1 tile trailer

11 words
-> 176 bits
-> 22 bits per pixel

4 hits (4 pixels each) in 1 region:
- 1 tile header
- 1 region header
- 16 data
- 1 tile trailer

19 words
-> 304 bits
-> 19 bits per pixel

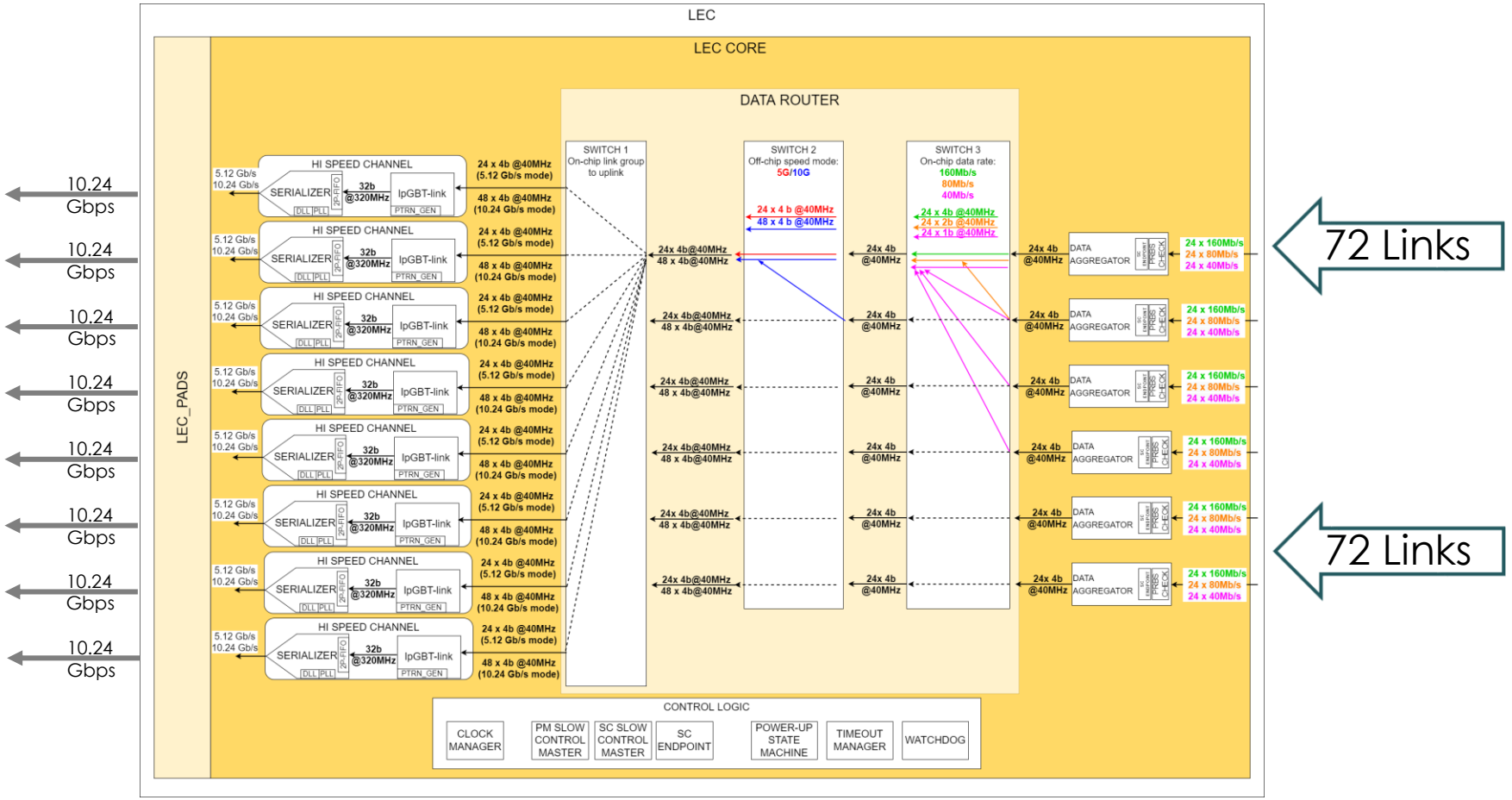
1 tile hit (2 pixels):
- 1 tile header
- 1 region header
- 2 data
- 1 tile trailer

5 words
-> 80 bits
-> 40 bits per pixel

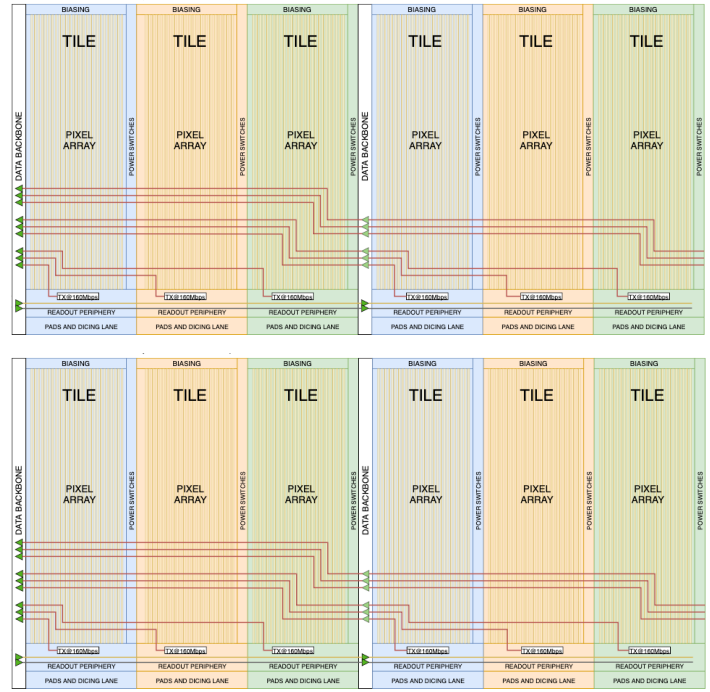
1 row threshold scan:
- 1 tile header
- 1 region header
- 38 data
- 1 region header
- 38 data
- 1 region header
- 40 data
- 1 region header
- 40 data
- 1 tile trailer

162 words
-> 2,592 bits

Data Flow – From Tiles to Left Endcap



x 12 RSU



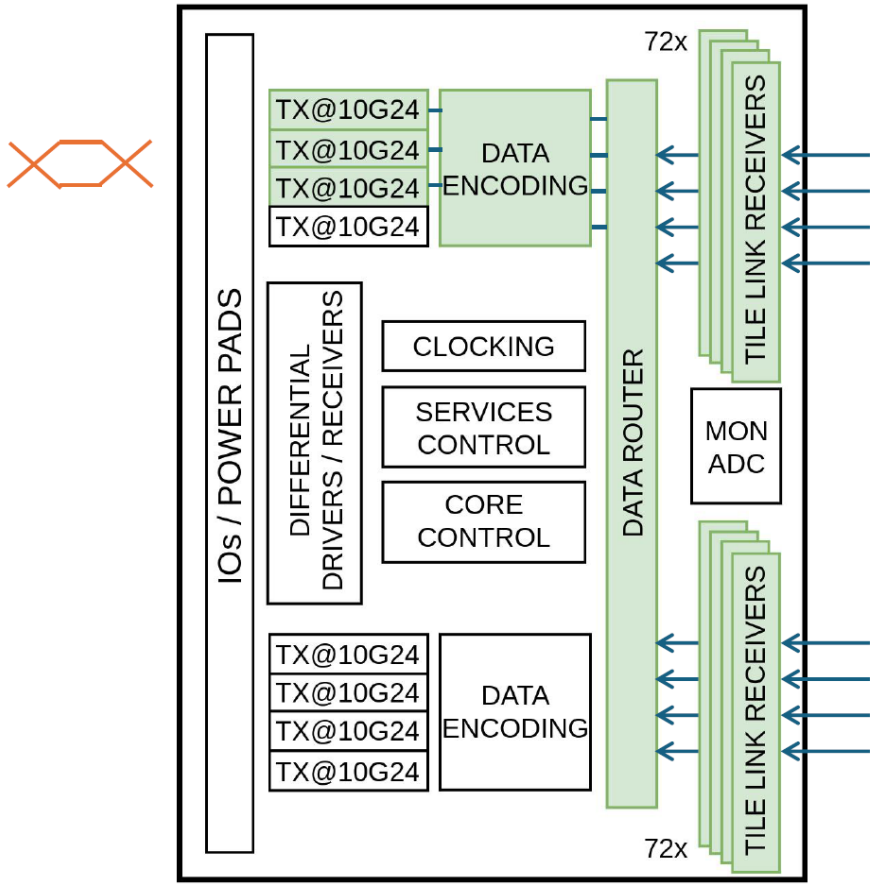
12-RSU MOSAIX
160 Mbps x 144 = 22.5 Gbps
Full capacity: 8 HS serializers = 80 Gbps (10 Gbps each)
Fallback: 40 Gbps, 5 Gbps each
4 outputs into one VTRx+

6-RSU LAS
72 Tiles
1 HS serializer = 10 Gbps

5-RSU LAS
60 Tiles
1 HS serializer = 10 Gbps

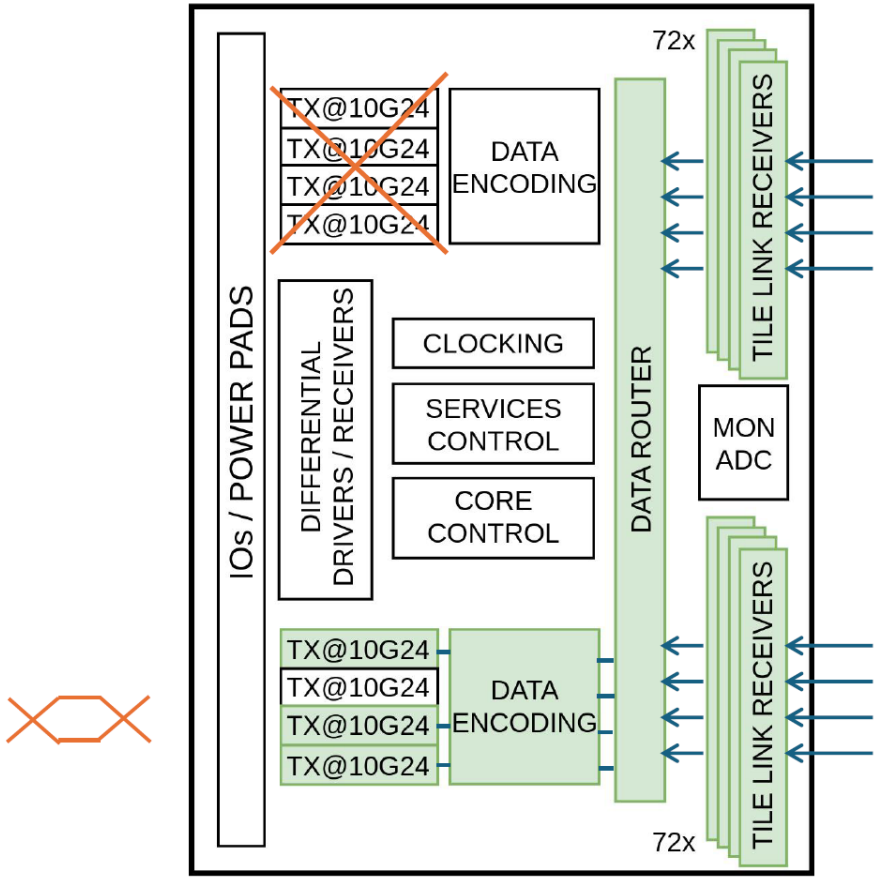
LEC Nominal Operation

[nominal operation]



10.24 Gb/s per serializer
3 serializers in use

[in case of fault]



10.24 Gb/s per serializer
3 serializers in use

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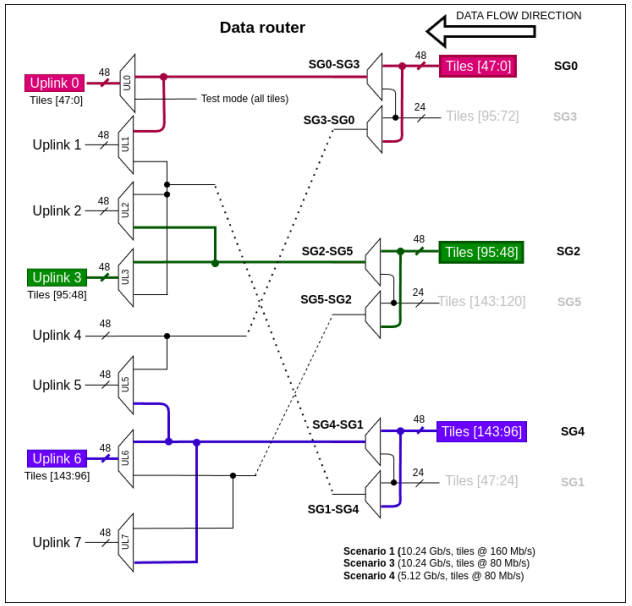
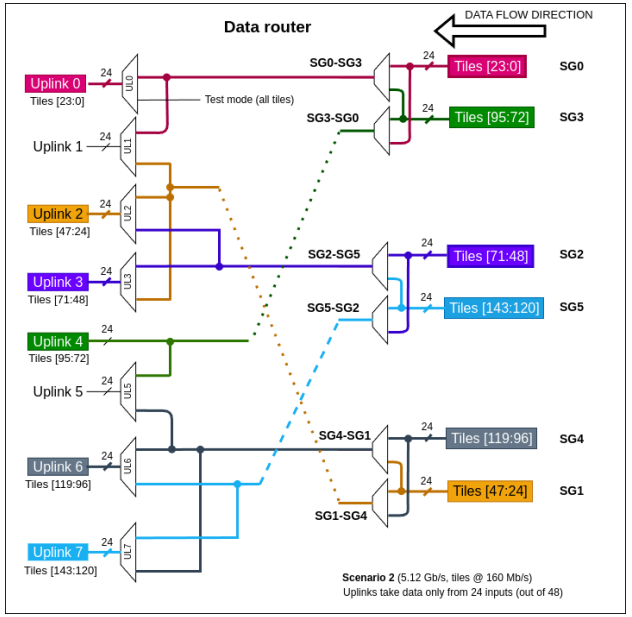
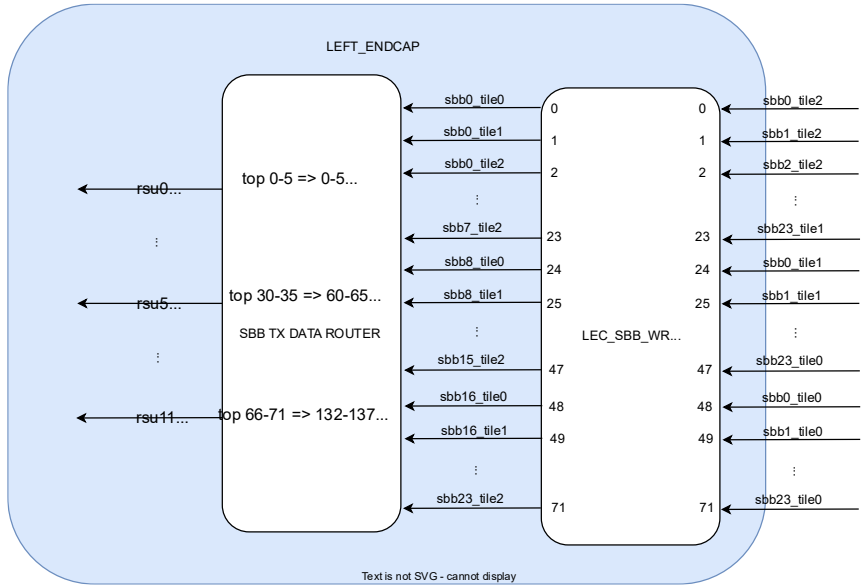
LEC Data Routing

Scenarios 1, 3, 4				
	Uplink 0	Uplink 1	Uplink 2	Uplink 3
Tiles[47:0]	x	x		
Tiles[95:48]			x	x
Tiles[143:96]		x	x	x
	Uplink 4	Uplink 5	Uplink 6	Uplink 7



Scenario 2				
	Uplink 0	Uplink 1	Uplink 2	Uplink 3
Tiles[23:0]	x	x		
Tiles[47:24]		x	x	x
Tiles[71:48]			x	x
Tiles[95:72]	x	x		
Tiles[119:96]		x	x	x
Tiles[143:120]			x	x
	Uplink 4	Uplink 5	Uplink 6	Uplink 7





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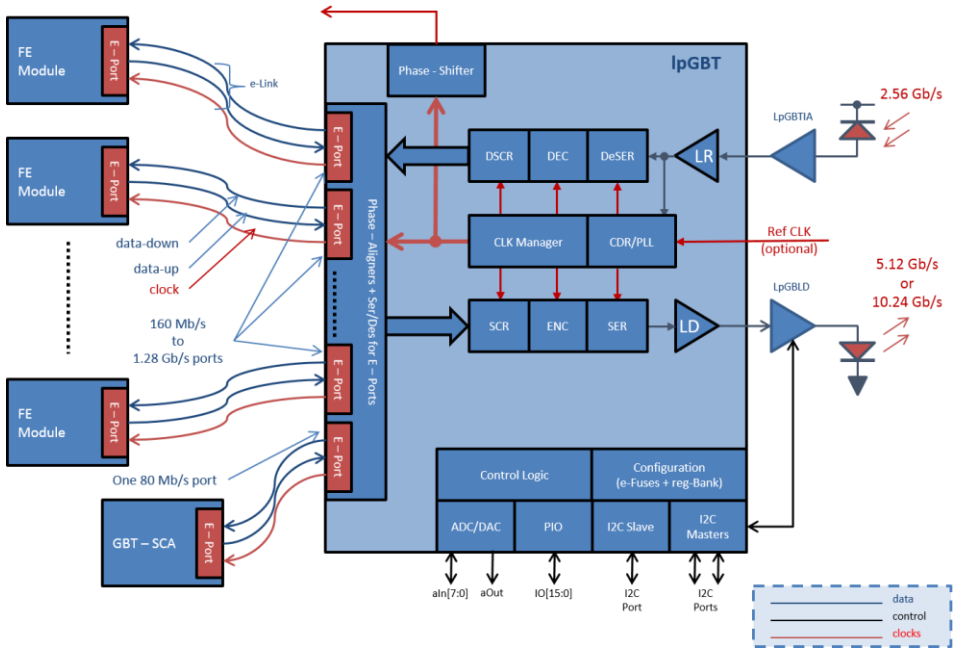
Left Endcap: Use **lpGBT** for Data Transmission

Communicates with

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

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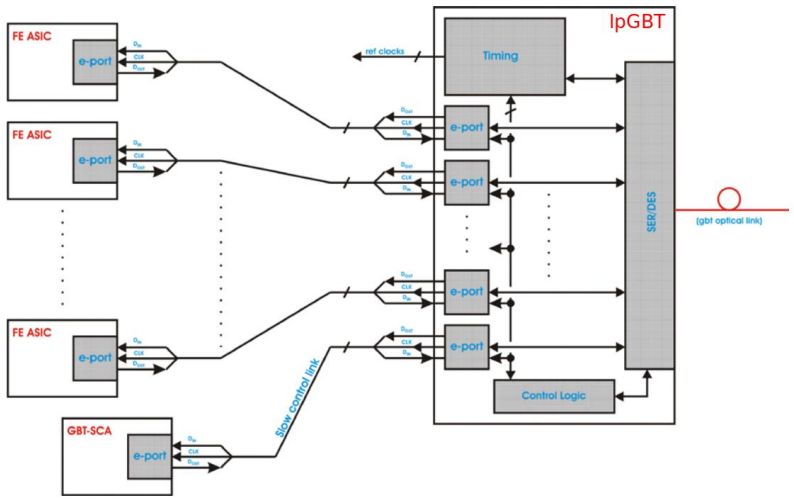
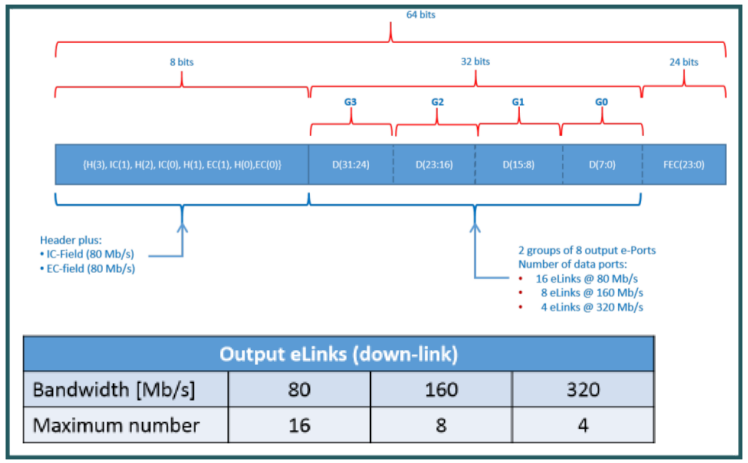
lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 128bit or 256bit
  - 256bit frame contains 192bits of payload (7.68 Gbps)
  - Up to 24 e-links at either 160 Mbps or 320 Gbps



Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = **1.280 Gbps**

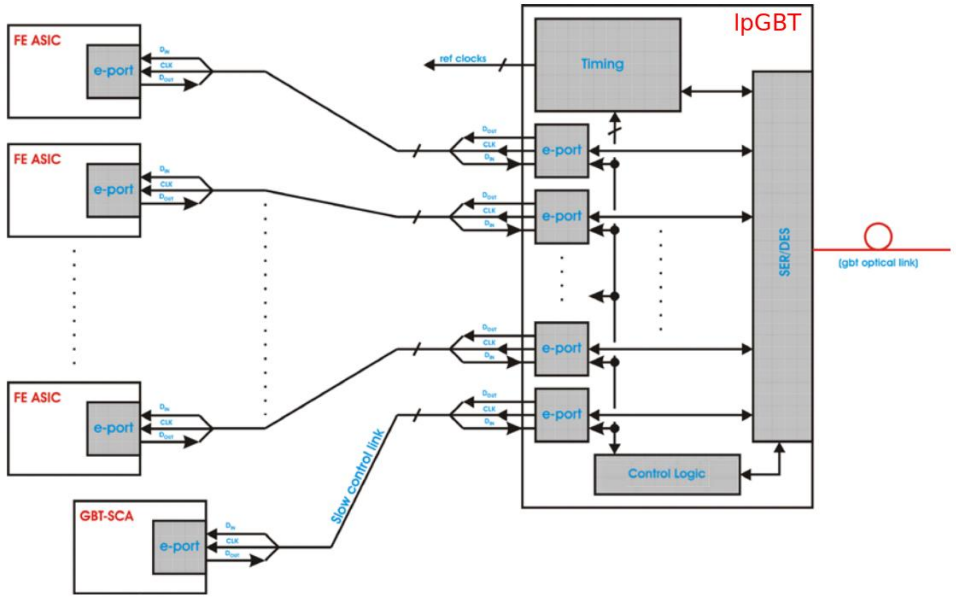
Data Uplink

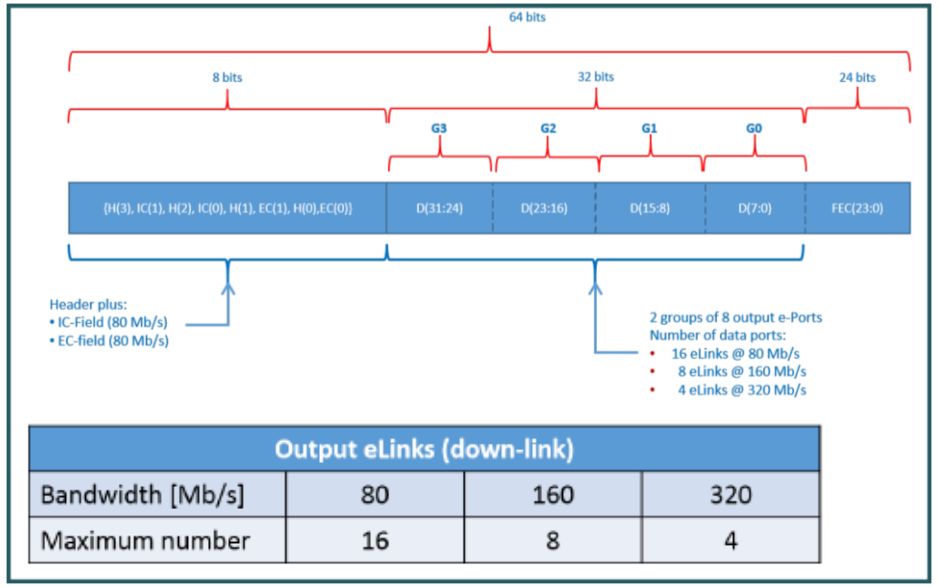
192 out of 256 bits are data:
Payload = **7.680 Gbps**

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

lpGBT Architecture





Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = 1280 Mbps

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Frame	Function	I/O Group
FRMUP[47:0]	FEC[47:0]	
FRMUP[79:48]	Data[31:0]	0
FRMUP[111:80]	Data[63:32]	1
FRMUP[143:112]	Data[95:64]	2
FRMUP[175:144]	Data[127:96]	3
FRMUP[207:176]	Data[159:128]	4
FRMUP[239:208]	Data[191:160]	5
FRMUP[249:240]	{8'b0, DownIC[1:0]}	See text
FRMUP[251:250]	EC[1:0]	
FRMUP[253:252]	IC[1:0]	
FRMUP[255:254]	H[1:0]	H[1:0] = 2'b 10

Each I/O group contains either 4, 2, or 1 elink(s)

Uplink

192 out of 256 bits are data:
Payload = 7680 Mbps

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

lpGBT Data Format

Uplink Format (5.12 or 10.24 Gbps)

- **5.12Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (112bit)**: From lpGBT e-links.
  - **FEC (10bit)**: Can correct up to 5 consecutives errors.

- **5.12Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (98bit)**: From lpGBT e-links (2bit unconnected).
  - **FEC (24bit)**: Can correct up to 12 consecutives errors.

- **10.24Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (230bit)**: From lpGBT e-links (6bit unconnected).
  - **FEC (20bit)**: Can correct up to 10 consecutives errors.

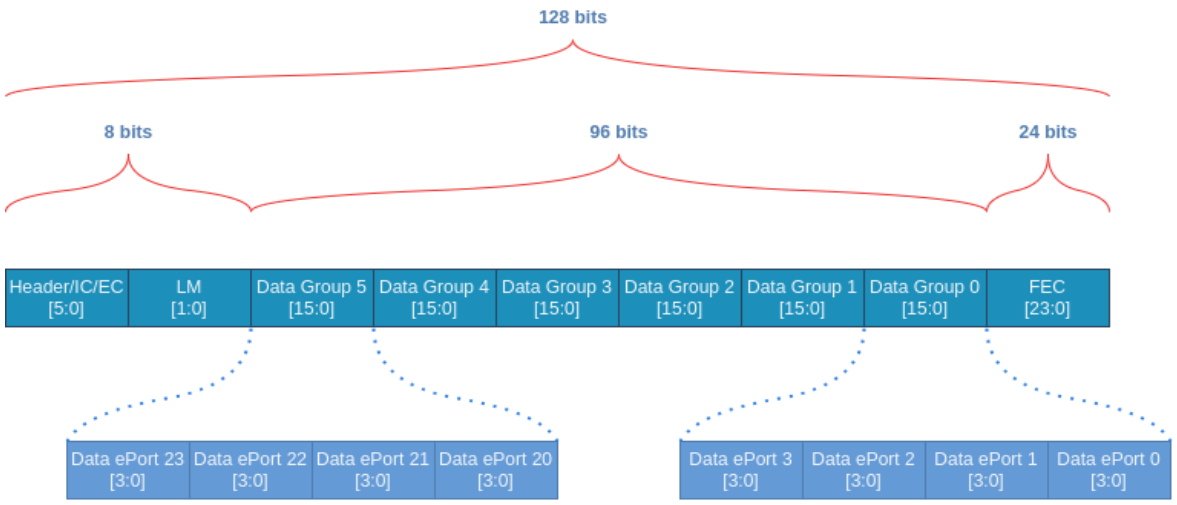
- **10.24Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (202bit)**: From lpGBT e-links (10bit unconnected).
  - **FEC (48bit)**: Can correct up to 24 consecutives errors.

Downlink Format (2.56 Gbps)

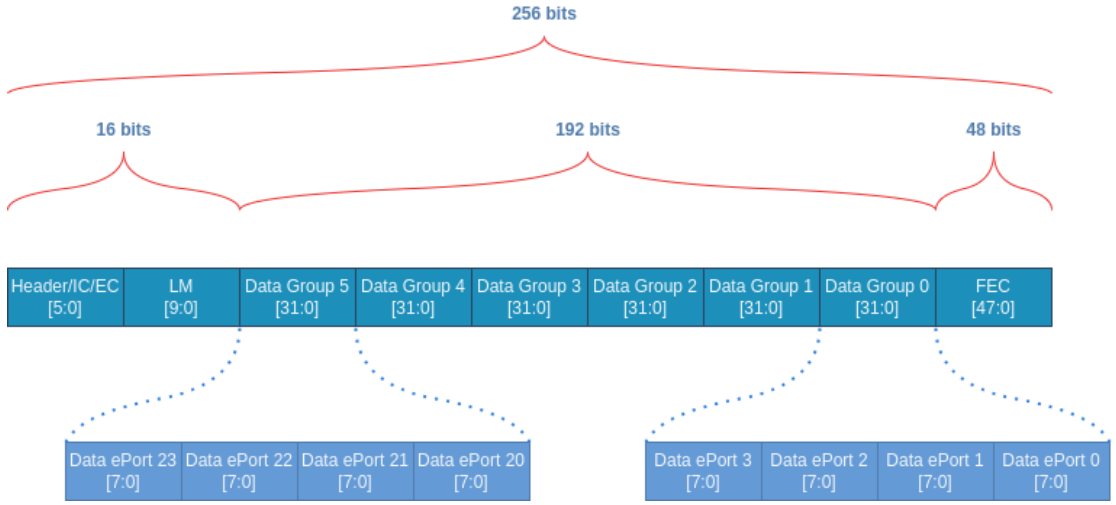
- **Header (4bit)**: Used by the lpGBT to align the frame.
- **User data (32bit)**: sent to lpGBT e-links.
- **EC (2bit)**: used for the external slow control (e.g.: GBT-SCA).
- **IC (2bit)**: used for the internal slow control of the lpGBT (register configuration).
- **FEC (24bit)**: used to recover from transmission error (can correct up to 12 consecutives errors).

lpGBT ePort Routing

5.12Gbps



10.24Gbps

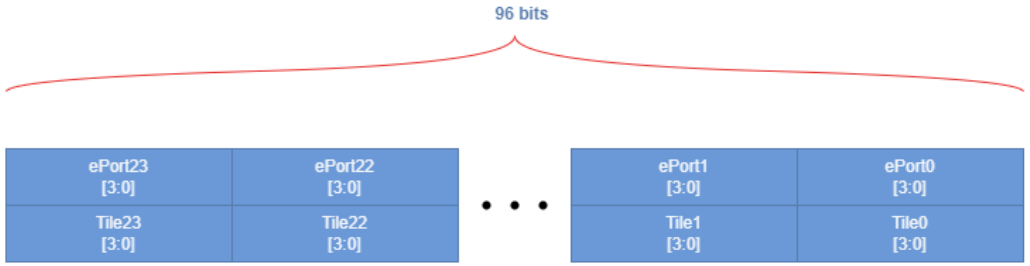


MOSAIX uplink						
Uplink bandwidth (Gbps)	5.12			10.24		
FEC Coding	FEC12			FEC12		
Tile bandwidth (Mbps)	40	80	160	40	80	160
Tiles per uplink [1]	48	48	24	48	48	48
Bits per tile	1	2	4	1	2	4
Tiles per ePort	2	2	1	2	2	2
Bits per ePort	4	4	4	8	8	8
Used bits per ePort	2	4	4	2	4	8
Bandwidth efficiency	50%	100%	100%	25%	50%	100%

1. To simplify routing scheme, 48 tiles are connected in instances where there are bandwidth enough to support a higher number of tiles.

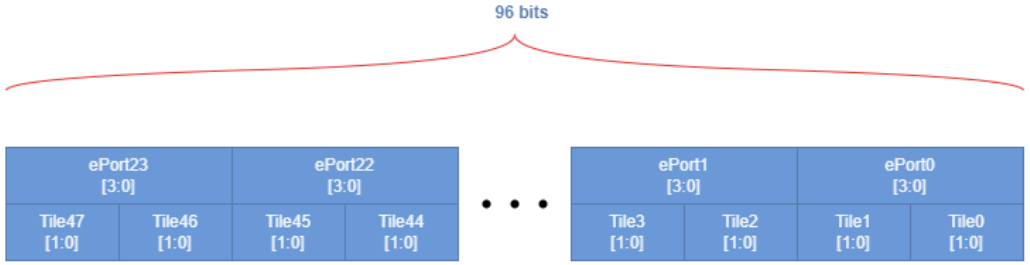
LEC Data Routing

5 Gbps / 160 MHz (6 links)



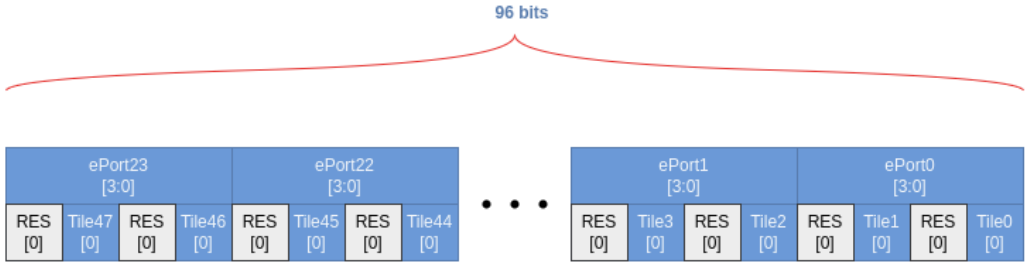
4 frames to reconstruct tile word

5 Gbps / 80 MHz



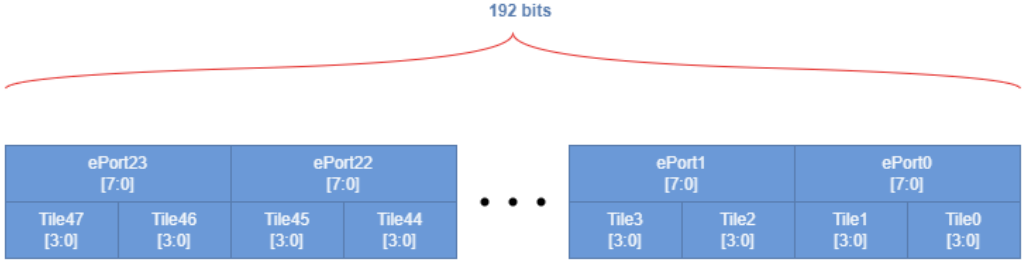
8 frames to reconstruct tile word

5 Gbps / 40 MHz



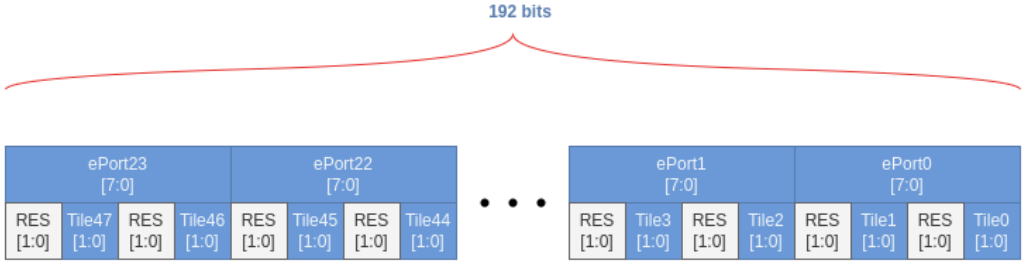
16 frames to reconstruct tile word

10 Gbps / 160 MHz (3 links)



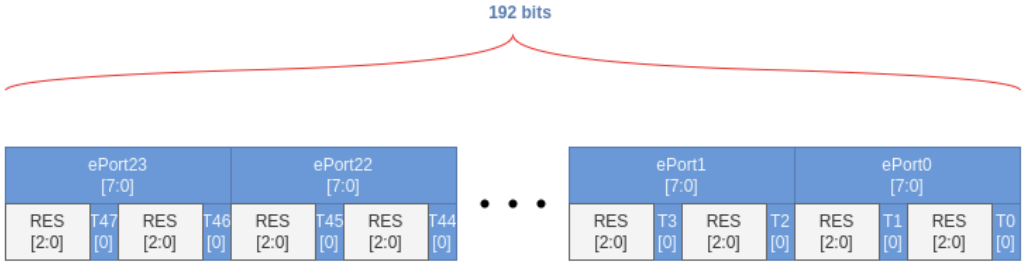
4 frames to reconstruct tile word

10 Gbps / 80 MHz



8 frames to reconstruct tile word

10 Gbps / 40 MHz



16 frames to reconstruct tile word

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SVT Counts

	width (mm)	length (mm)		# pixels per RSU:						
Reticle size	19.564	21.666		**831,168**						
Pixel size	0.0208	0.0228								
Barrel						**10x275 GeV**				
Layer Index	**Area (mm^2)**	**# sensors**	**# pixels**	**# Data Fibers**	**Hit Rate/ms**	**Data Rate (Mbps)**	**Data Rate / Fiber (Mbps)**	**Epty Rate (Gbps)**	**Epty Rate / Fiber (Mbps)**	**Number of SC channels**
L0	58,811	4	119,688,192	96	1791732.00	218717.29	6075.48	12.875	366.211	6
L1	78,414	4	159,584,256	128	1095604.00	133740.72	2786.27	17.166	366.211	8
L2	196,035	8	398,960,640	320	600729.00	73331.18	611.09	42.915	366.211	20
L3	882,158	368	1,835,218,944	368	1645551.00	200872.92	545.85	205.994	549.316	16
L4	2,216,706	1120	4,654,540,800	1120	888591.00	108470.58	96.85	529.289	457.764	48
e-endcap										
Disk index										
ED0	176,710	96	398,960,640	96	538309.00	65711.55	684.50	42.915	457.764	8
ED1	536,815	334	1,388,050,560	334	976195.00	119164.43	356.78	149.310	457.764	16
ED2	553,632	334	1,388,050,560	334	940608.00	114820.31	343.77	149.310	457.764	16
ED3	552,835	334	1,388,050,560	334	618422.00	75490.97	226.02	149.310	457.764	16
ED4	551,127	334	1,388,050,560	334	97019.00	11843.14	35.46	149.310	457.764	16
h-endcap										
Disk index										
HD0	176,710	96	398,960,640	96	438216.00	53493.16	557.22	42.915	457.764	8
HD1	536,815	334	1,388,050,560	334	624534.00	76237.06	228.25	149.310	457.764	16
HD2	553,216	334	1,388,050,560	334	165565.00	20210.57	60.51	149.310	457.764	16
HD3	548,909	334	1,388,050,560	334	14334.00	1749.76	5.24	149.310	457.764	16
HD4	542,422	334	1,388,050,560	334	7064.00	862.30	2.58	149.310	457.764	16
TOTAL	**8,161,315**	**4448**	**19,070,318,592**	**4896**	**1.0442E+10**	**hits/s**		**Empty Rate:**		**242**
						1244.84	**Gbps**		**2088.5**	**Gbps**
			Noise Rate			1.00E-08	(1/pixel/10us)			
			Total Noise Pixels/s			**1.91E+07**	**pixel/s**			
			Total Noise Rate			**1.14**	**Gbps**			

16bit/tile

32bit/pixel

64bit/pixel

Max Rates after Shuji's recent updates (11/2025)

DATA RATES

Data from Shujie November

- **Max Hit Rate per RSU ED0: < 1072 hits per tile per ms**
- 1072 hits/ms/tile * 1000ms/s * 4 pixels per hit * 32 bits/pixel = **137.2 Mbps**

- **Max Hit Rate per RSU L0: < 2301 hits per tile per ms**
- 2365 hits/ms/RSU * 1000ms/s * 4 pixels per hit * 32 bits/pixel = **294.5 Mbps**

NOISE RATES

- **10E-8 per pixel per 10us timeframe** * 100,000 * 69,264 pixels/tile * 64bits/pixel = **4.33 kbps**

- **10E-6 per pixel per 10us timeframe** * 100,000 * 69,264 pixels/tile * 64bits/pixel = **443 kbps**

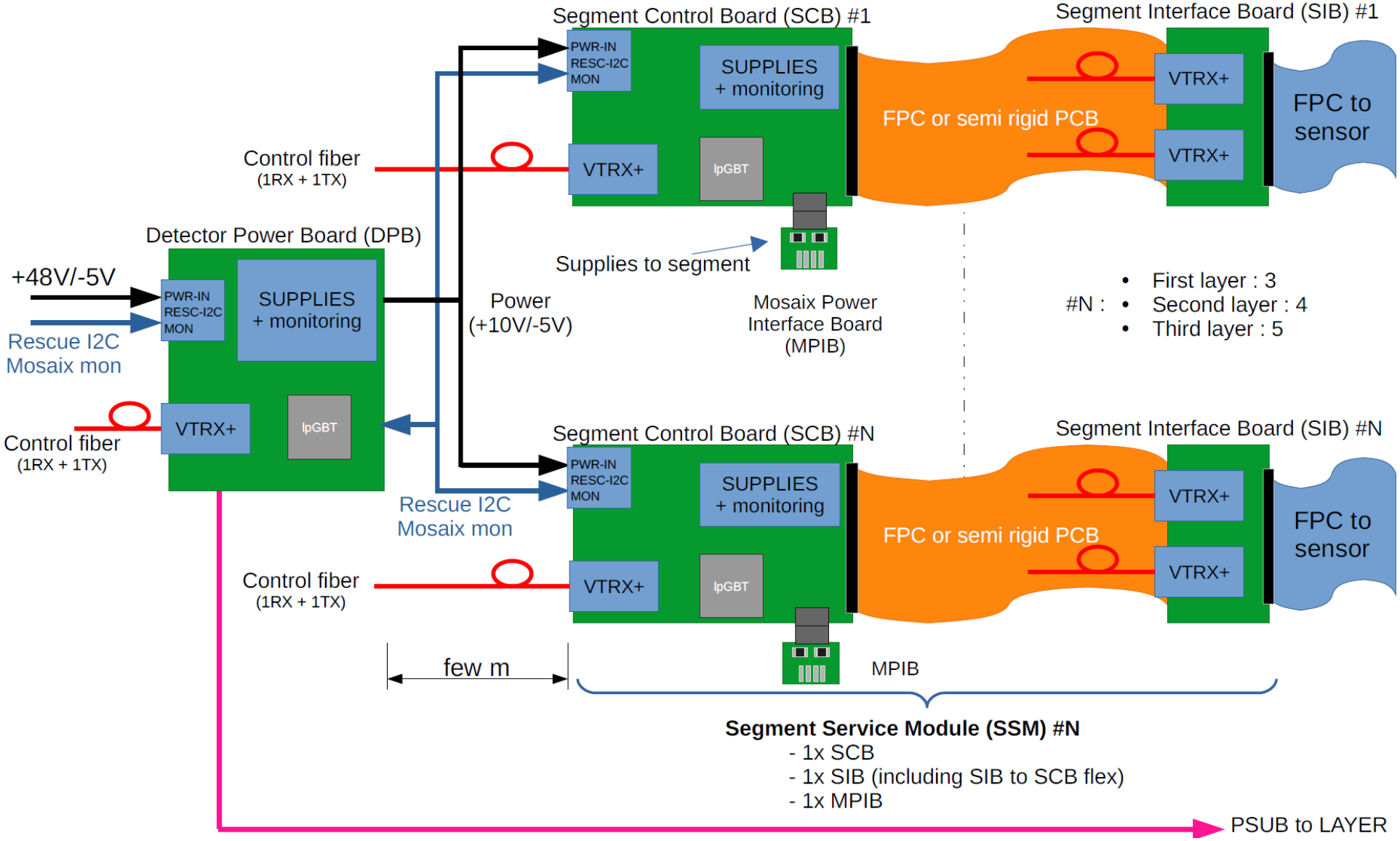
TOTAL

130.2 Mbps + 443 kbps = **137.7 Mbps**

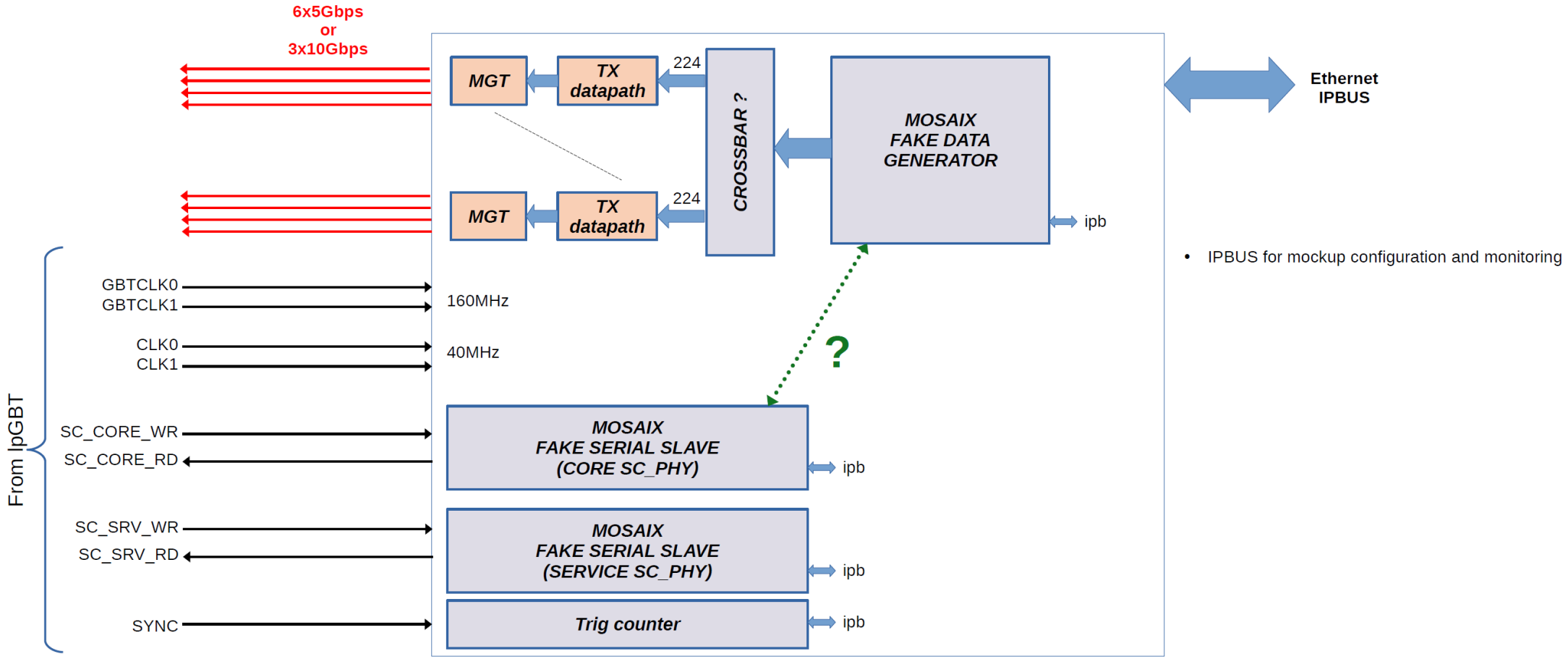
J. Schambach

DAQ Test Setup

IB Readout Architecture



Mockup of MOSAIX by an FPGA (ITS3 WP6)



- IPBUS for mockup configuration and monitoring

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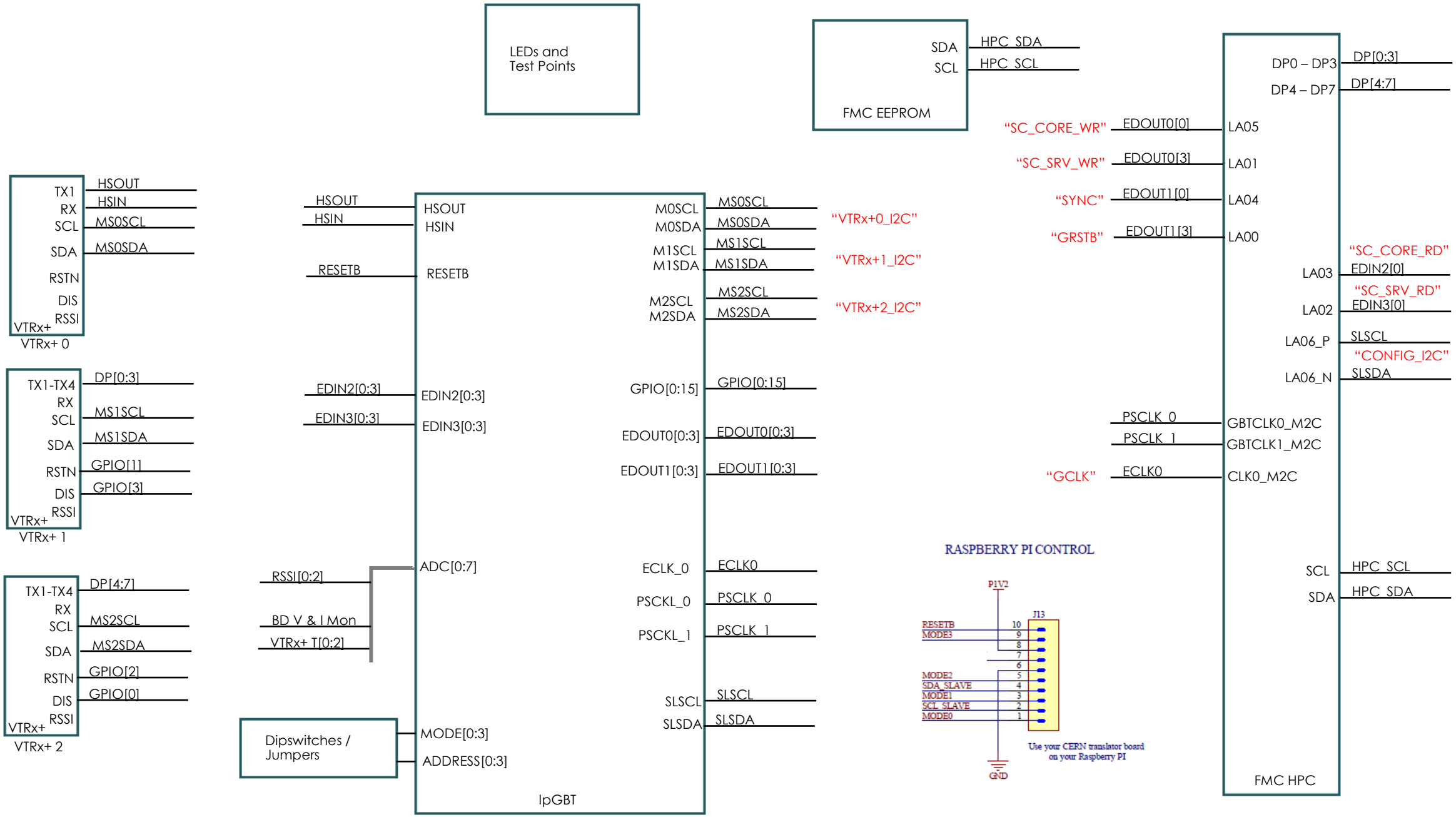

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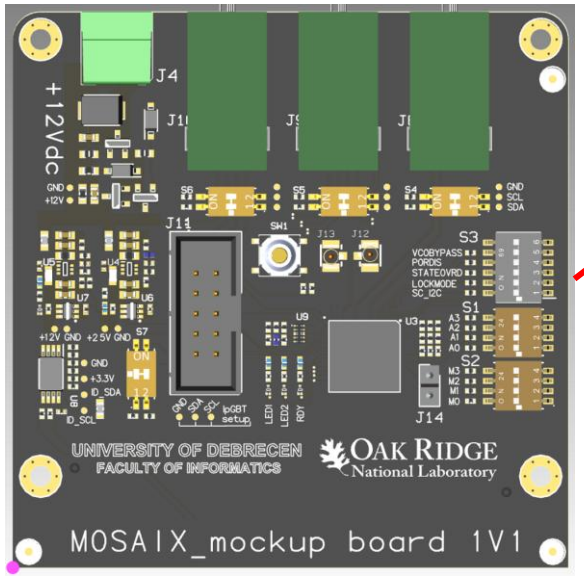
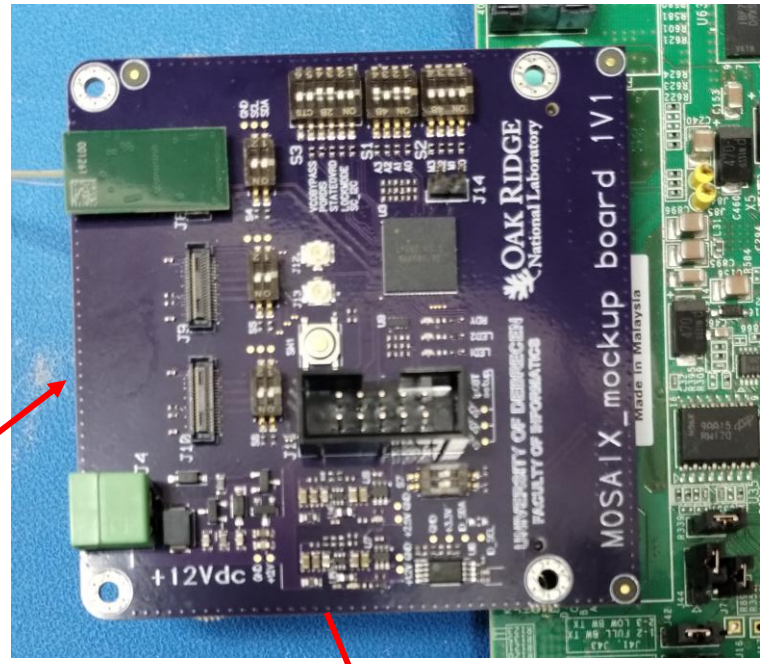
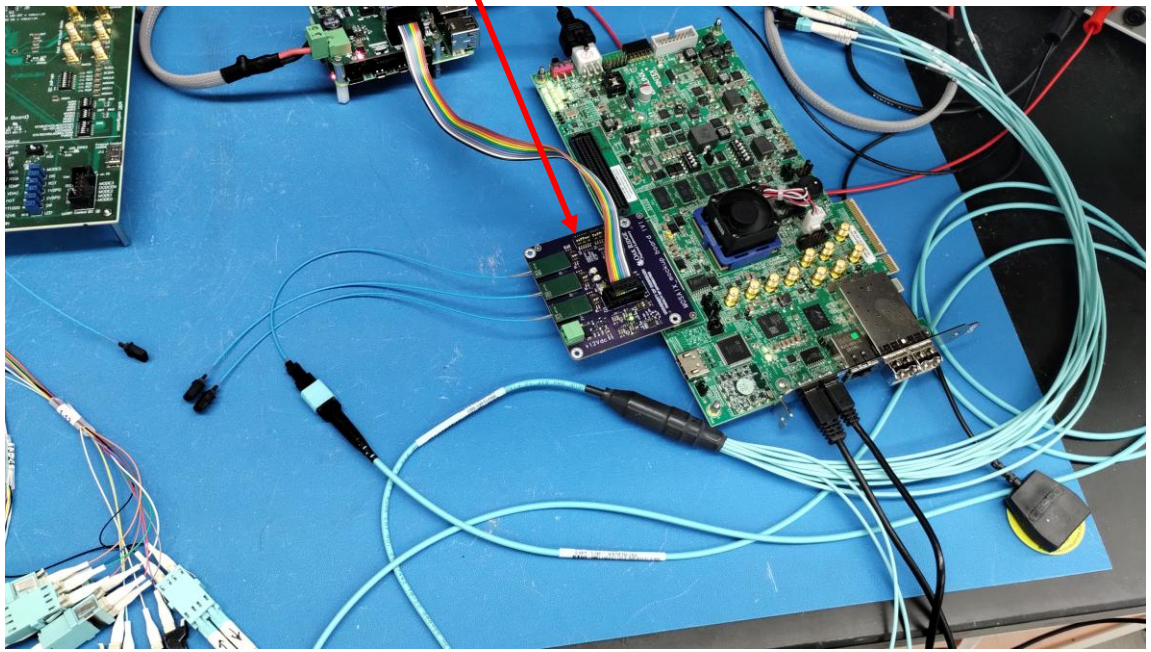
V1.1 Pictures







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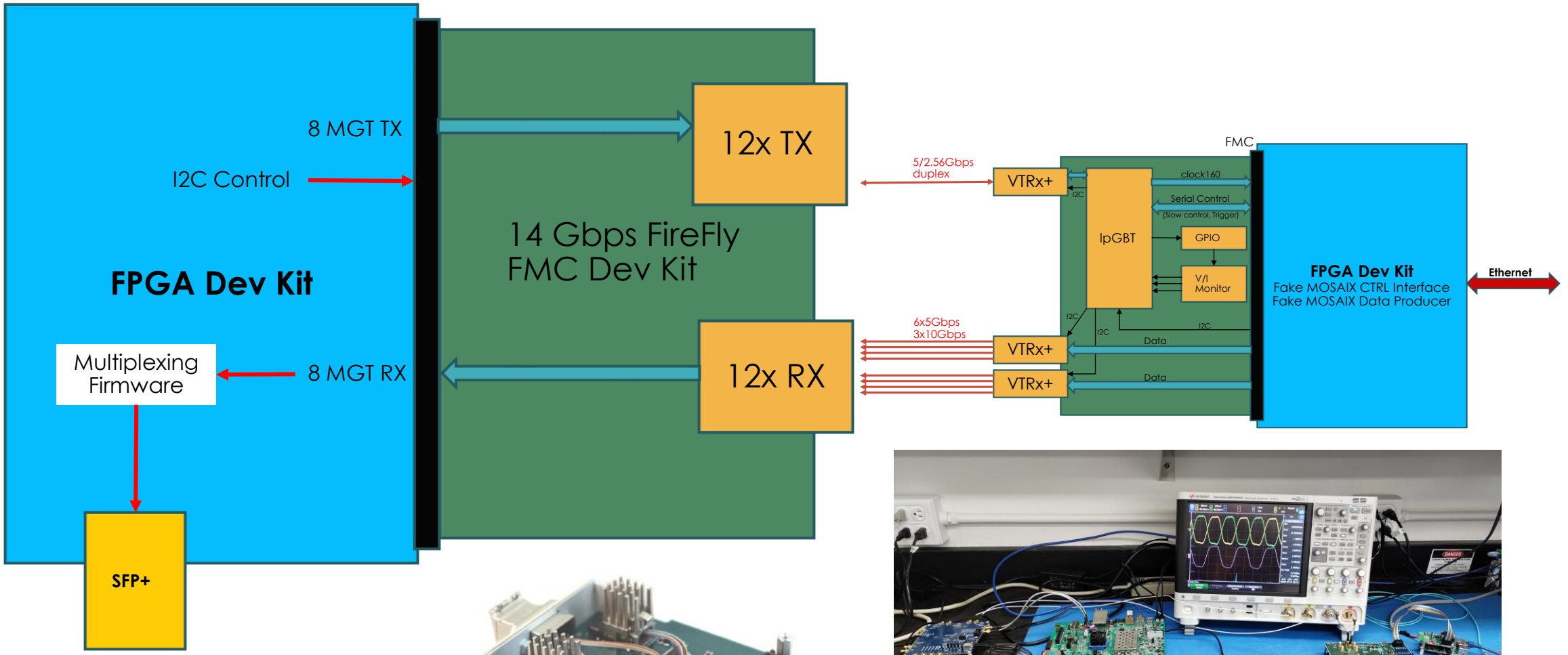
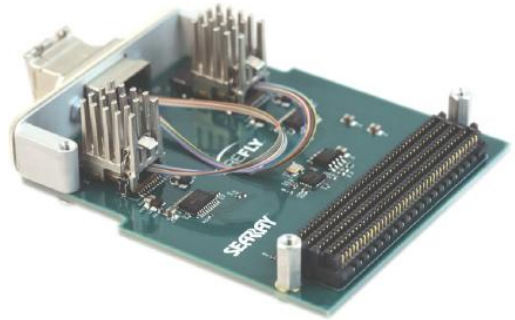
Aggregator Board Prototyping





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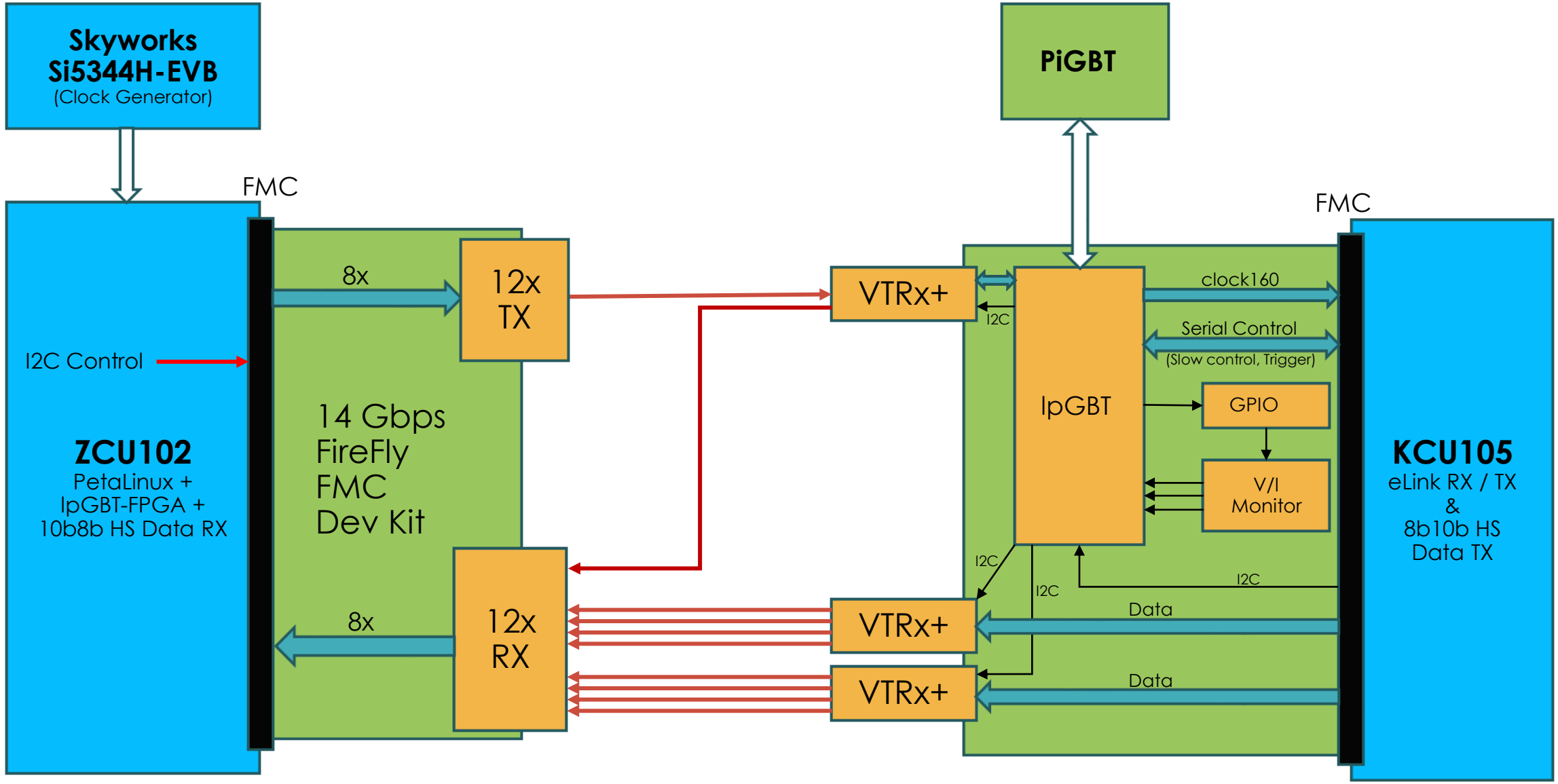
MOSAIX Hardware Mockup Test Setup



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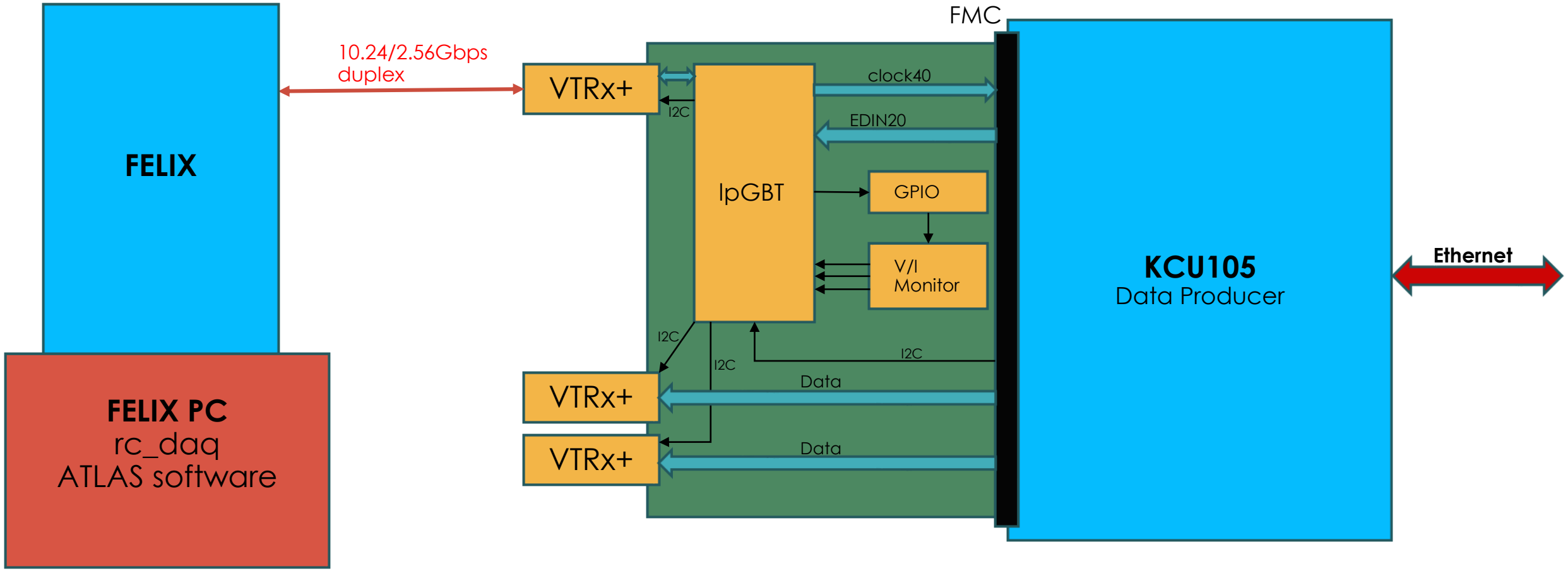
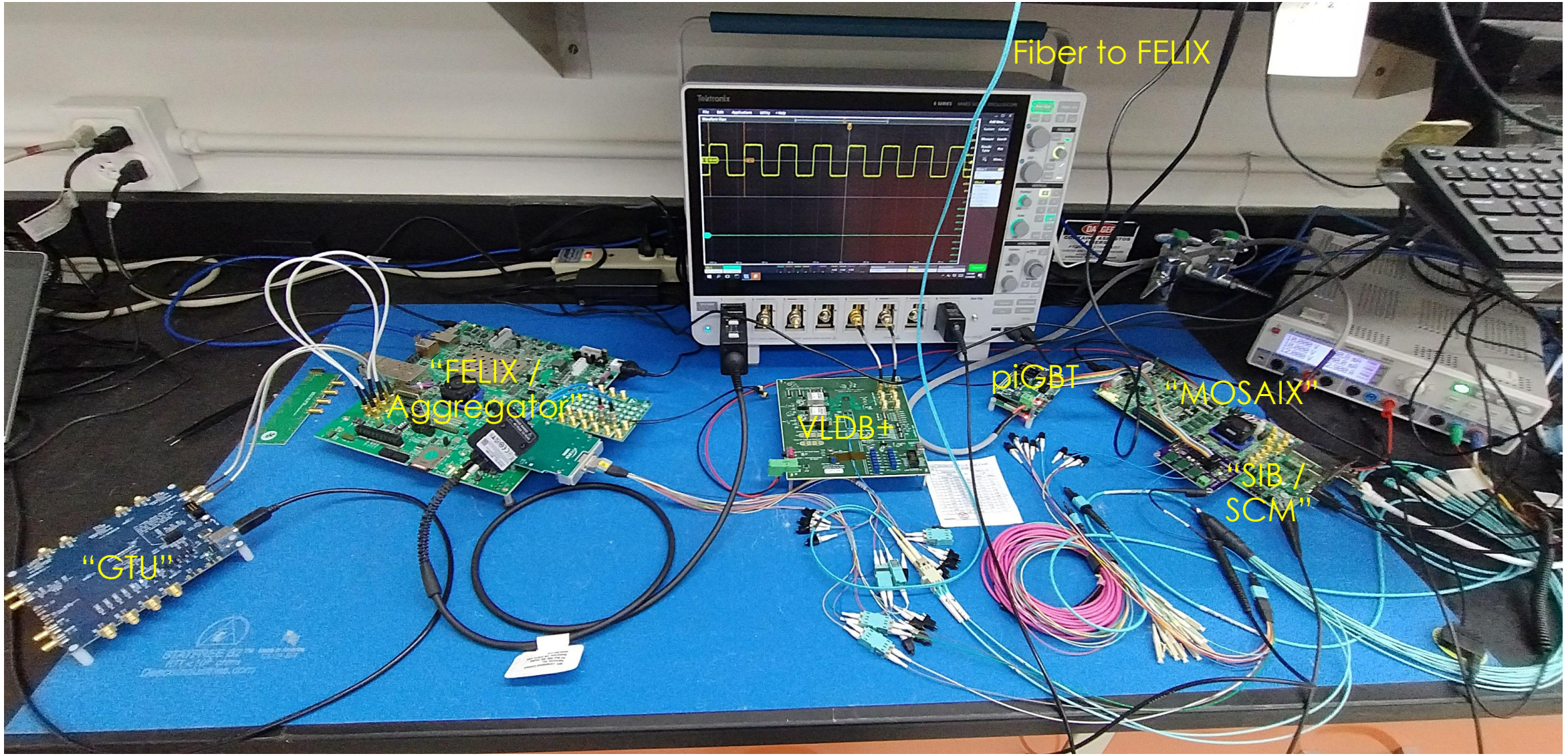
lpGBT DAQ Hardware Setup



Readout Chain:

FPGA BRAM -> FMC -> MOSAIX Mockup Board – lpGBT elink EDIN20 -> fiber 10.24 Gbps -> FELIX -> PCIe -> Workstation RAM -> rc_daq -> disk

Full Test Setup



lpGBT DAQ setup

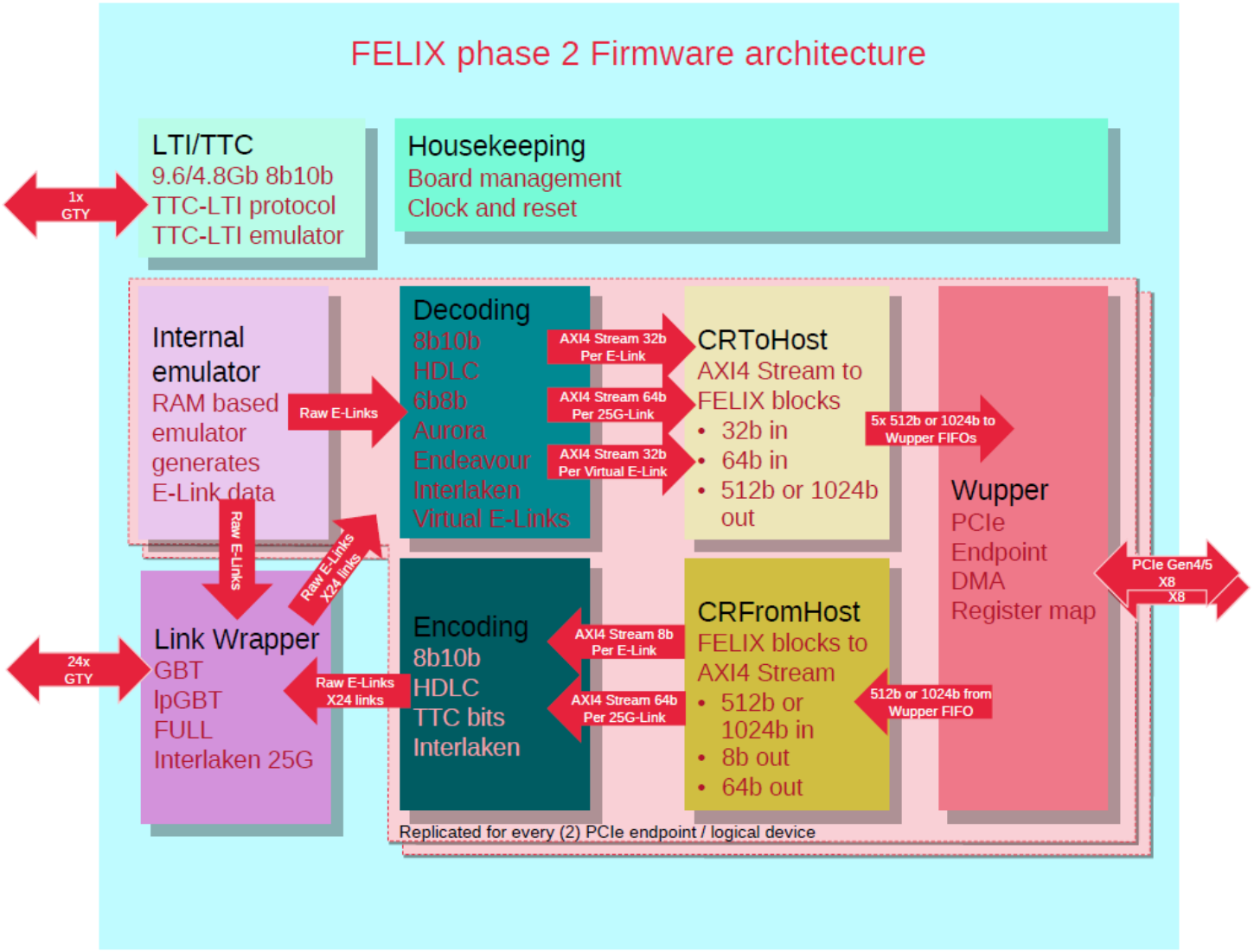
- FELIX **FLX-712** from sPHENIX, running ATLAS lpGBT firmware configured for 4 bidir lpGBT links
- Supermicro AMD EPYC based workstation (PCIe Gen3) running **RHEL9.7**
- ATLAS **tdaq** software stack (lpGBT register R/W over IC bits in fiber lpGBT frame; driver & libs for PCIe "wupper")
- sPHENIX rc_daq software
- sPHENIX **MVTX rc_daq plugin** (does "streaming" readout)
- **KCU105** with HPC FMC
- FPGA firmware: serialized data from FPGA BRAM @1280 Mbps, "ATLAS elink data format" (10b8b "chunk" data)
- **MOSAIX Mockup Board** to receive FPGA data to lpGBT elink **EDIN20**
- lpGBT configured with 10.24Gbps FEC12; elink EDIN20 configured for 1280Mbps

FELIX Firmware Flavors available from ATLAS

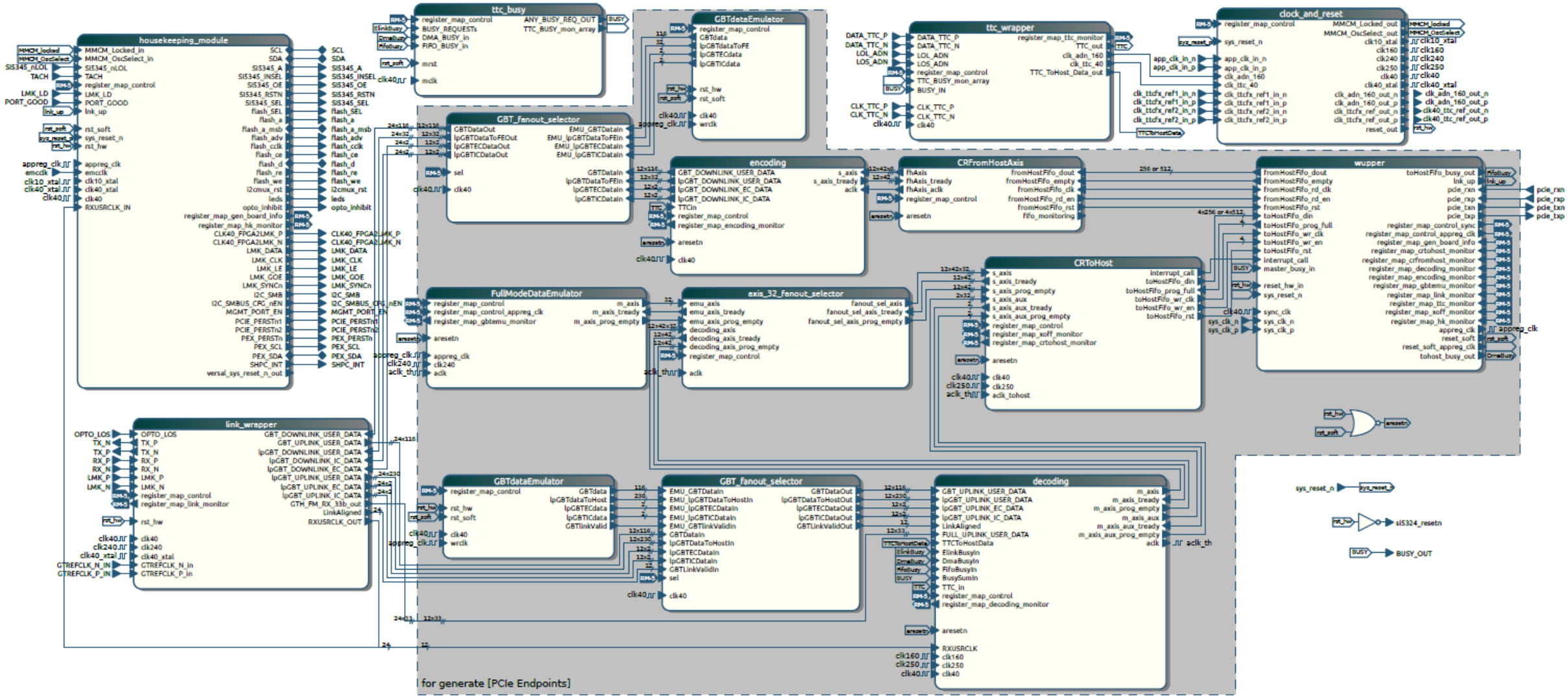
Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.
12: HGTD_LUMI	lpGBT	6b8b		
13: BCMPRIME	lpGBT			
14: FELIG-PIXEL	lpGBT-FE			

My Choice

FELIX Firmware Top Level



FELIX Firmware detailed



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ATLAS e-link Data Format

Block header : 32 bits
- Start of block symbol
- Block Size
- AXI-Stream ID
- Block sequence

(Sub)chunk header : 32 bits
- Fragment type
  - First, Last, Complete, Middle, NULL, Timeout, OOB
- Flags
  - Truncation, Error, CRC error, BUSY
- Reserved (9b)
- Subchunk length (16b)

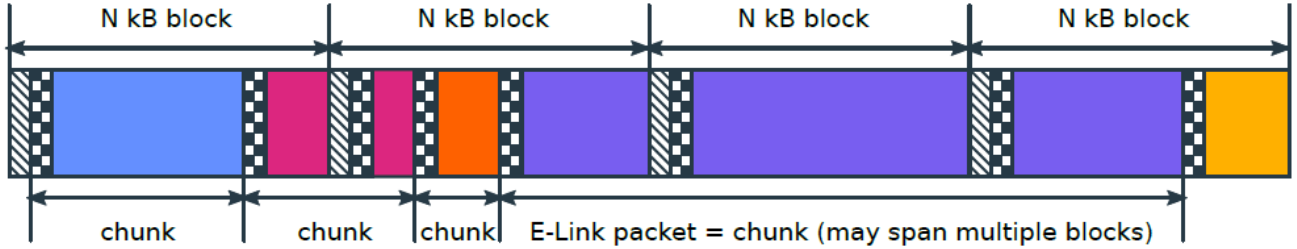


Figure B.2: FELIX ToHost Block format with chunk headers.

Table 3.1: K-characters used for 8B/10B coded links. BUSY-ON/OFF arrive from the front-end in both FULL mode and GBT mode cases..

K-character	8-bit value	Use
K28.1	0x3c	Start-of-Packet (SOP)
K28.6	0xdc	End-of-Packet (EOP)
K28.5	0xbc	idle
K28.2	0x5c	BUSY-ON (from front-end), XOFF (to front-end for FULL mode with GBT downlink)
K28.3	0x7c	BUSY-OFF (from front-end), XON (to front-end for FULL mode with GBT downlink)

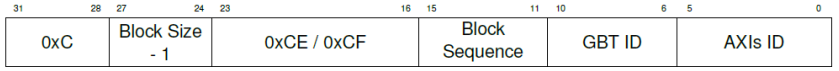


Figure B.3: Block Header Format.

- **0xC** 4b, Header identifier
- **BlockSize - 1**: 4b, Block size in kB-1, 0: 1kB, 3: 4kB etc.
- **0xCE** / **0xCF** 8b, Header identifier. 0xCE for chunk trailers, 0xCF for chunk headers.
- **Block Sequence** 5b, Incremental number per E-Link
- **GBT ID** 5b, Link index starting at 0 for every PCIe endpoint. For a 24 channel firmware with two PCIe endpoints, Link 12 will generate a GBT ID 0 in endpoint 1.
- **AXIs ID** 6b, Index of the E-Link on the AXI-Stream array. For GBT this number is equal to the Egroup * 8 + the Epath ID within the E-Group. For lpGBT this number is equal to the Egroup * 4 + the EPath ID within the E-Group. In Pixel firmware, each decoder separates DAQ and register read data. DAQ data gets AXIs ID 0, 4, 8, etc. Register data gets AXIs ID 1, 5, 9, etc.

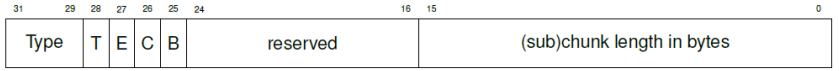


Figure B.4: Chunk trailer/header format.

- **Type** 3b:
  - 0: NULL header, padding
  - 1: First part of a chunk consisting of more than one part
  - 2: Last part of a chunk consisting of more than one part
  - 3: Chunk consists of one part
  - 4: Middle part of a chunk, consisting of more than two parts
  - 5: Timeout trailer
  - 6: Reserved
  - 7: Out of band (OOB)
- **T** Truncation flag, indicating that a decoder truncated the data to a maximum length, or because the FIFO was full.
- **E** Framing error, Front-End data does not comply with the specified data format. For instance a missing SOP, EOP, or payload data not within SOP/EOP.
- **C** CRC error, if implemented by the decoder.
- **B** E-Link BUSY indication
- **reserved** 9b, reserved for future use.
- **Length** 16b, Length in bytes of the chunk of subchunk. If the chunk spans multiple blocks, only the sub-chunk length is given.

Emulated Data: Chunk Format

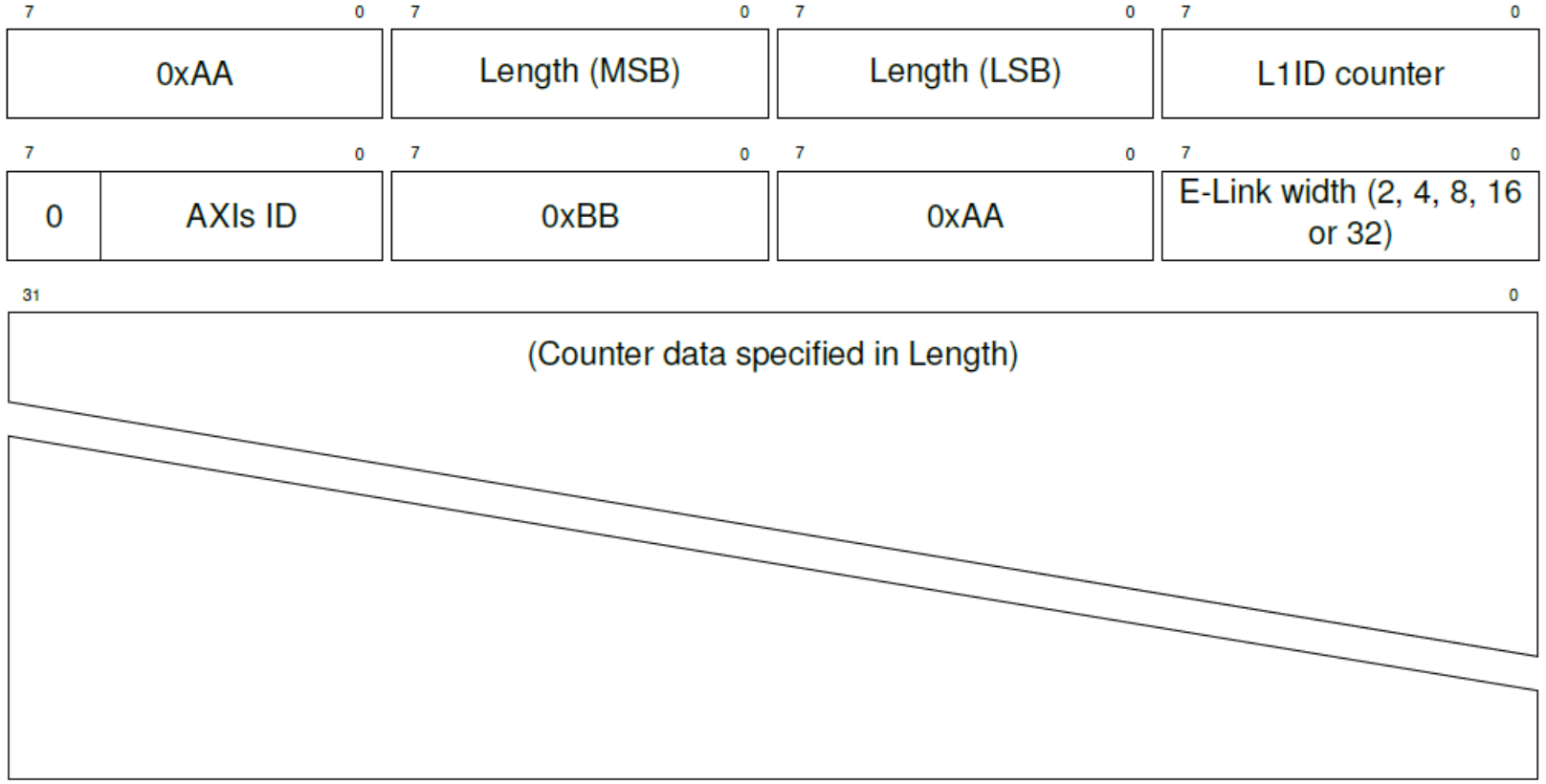
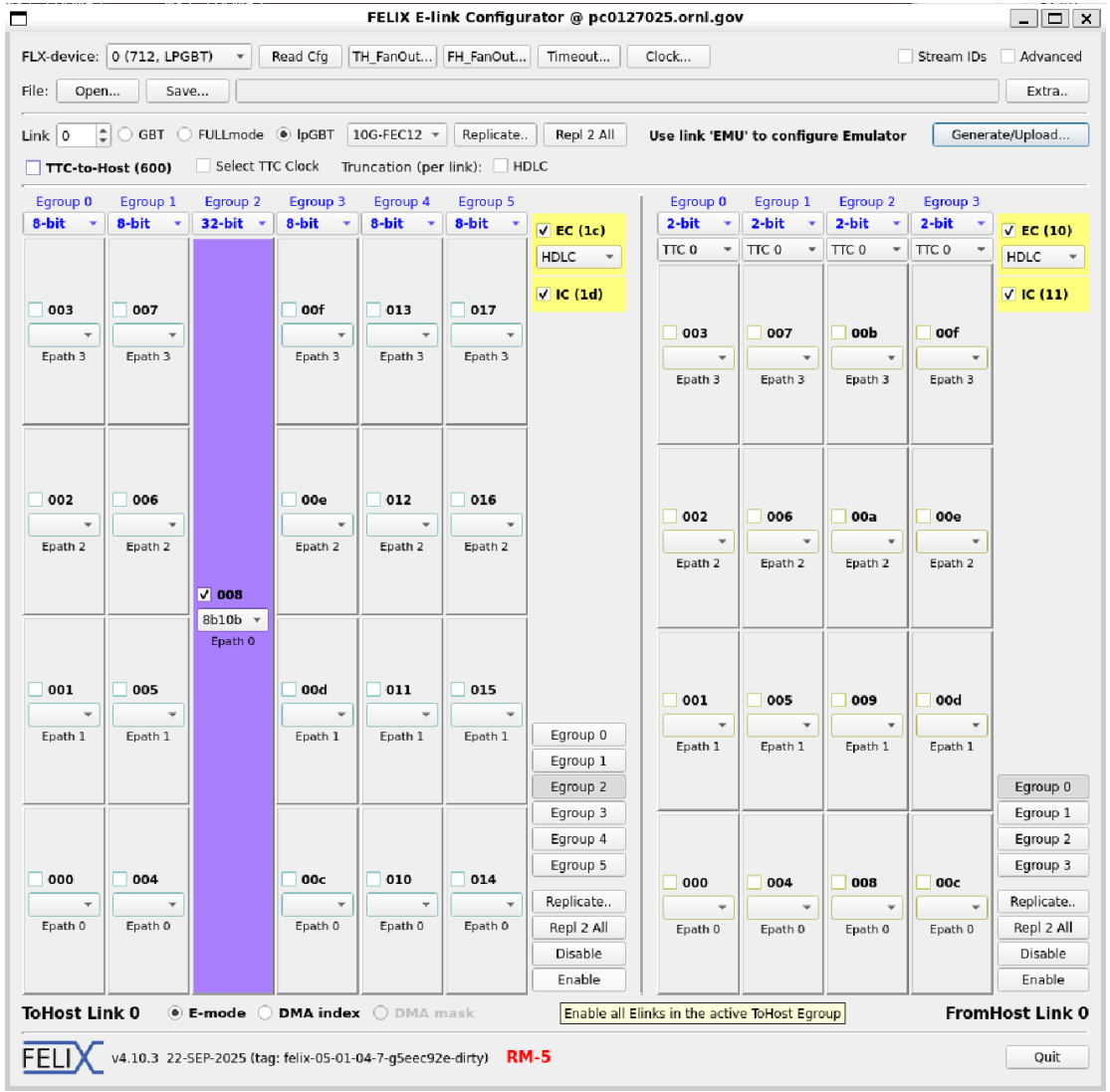


Figure B.12: Default Emulator payload.

This is loaded into the FPGA BRAM to be sent as 108b words over the elink

ATLAS tdaq Software: FELIX E-link Configurator



- Allows to configure FELIX elinks decoding and routing via PCIe bus

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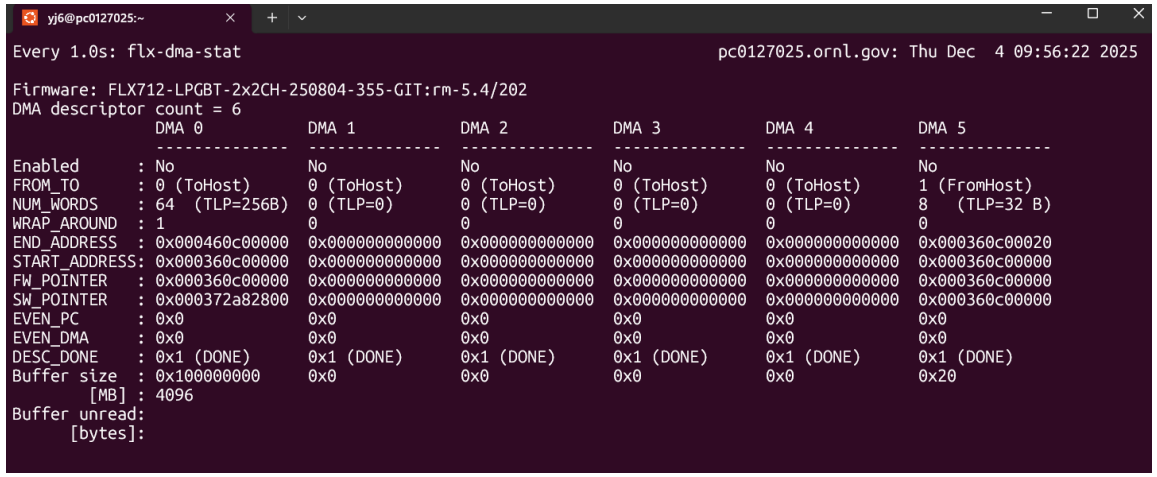
rc_daq Data taking

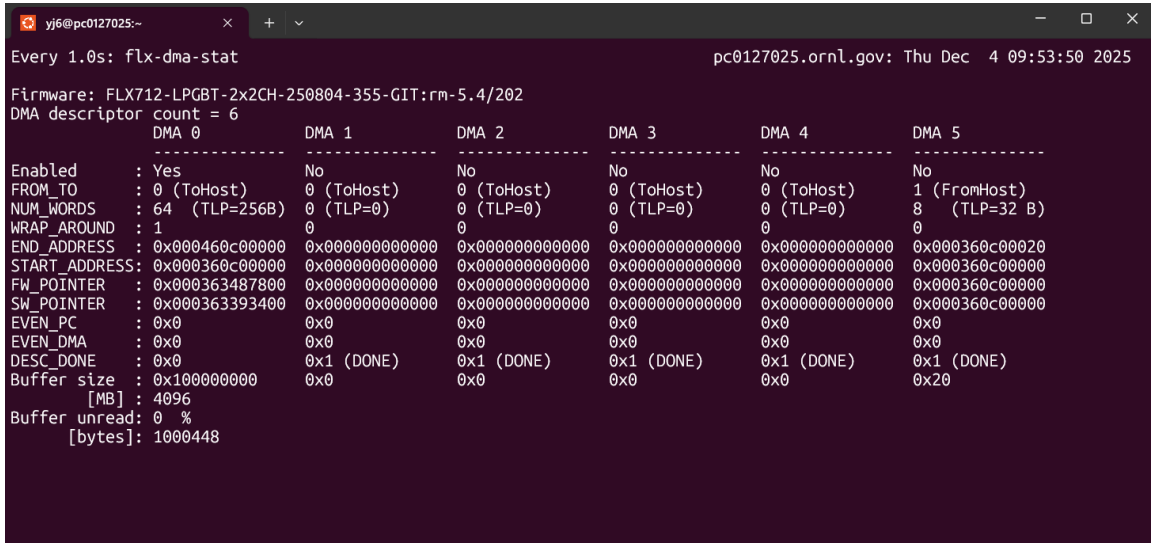
```
[yj6@pc0127025 rcdaq]$ watch –n 1 flx-dma-stat
[yj6@pc0127025 rcdaq]$ daq_begin
[yj6@pc0127025 rcdaq]$ daq_end
```

```
# dump the data using rc_daq provided dump command:
[yj6@pc0127025 rcdaq]$ ddump -g -s -p 2001 -n 0 /data/rcdaq/test_00000224-0000.prdf | hexdump -v -e
'"%010_ad: " 1/4 "%08x " "\n"' | less
0000000000: c0cf0008  # Block Header: Block size=0 (1kB), Block sequence=0, GBT ID=0, Axis ID=0x8
0000000004: 60000010 # Chunk Header: Type=011 (3=chunk consists of 1 part), length=0x0010 (16 bytes)
0000000008: 000800aa # Chunk 1st word (read from right to left): Length=0x0008 bytes
0000000012: 20aabb08 # Chunk 2nd word: elink width=x020 (32b), axisID=0x08
0000000016: 03020100 # Counter: 0,1,2,3
0000000020: 07060504 # Counter: 4,5,6,7
0000000024: 60000010
0000000028: 010800aa
0000000032: 20aabb08
0000000036: 03020100
0000000040: 07060504
0000000044: 60000010
…
```

DMA status when not taking data



While taking data: activity on DMA 0



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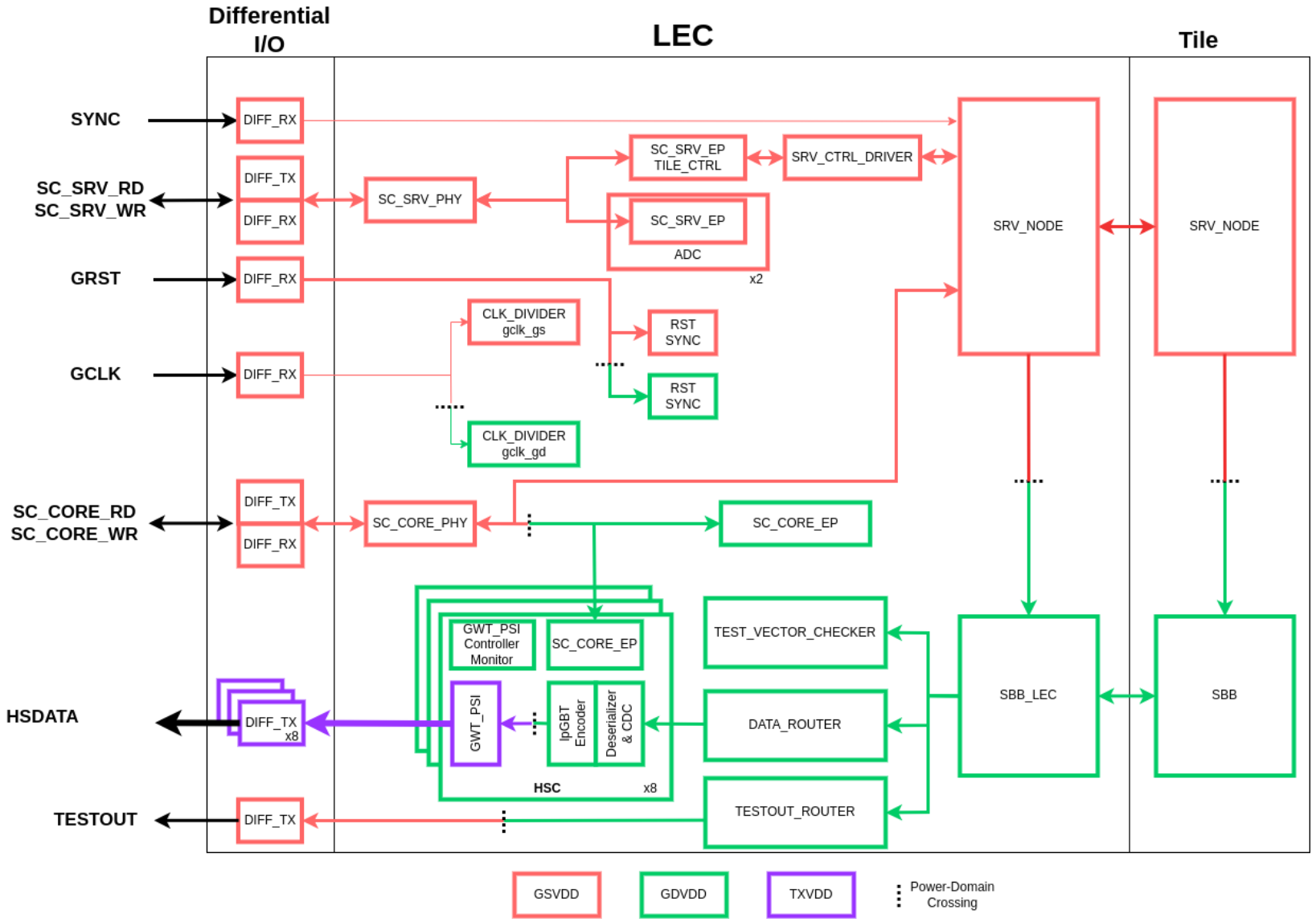
Slow Controls

LEC Block Diagram



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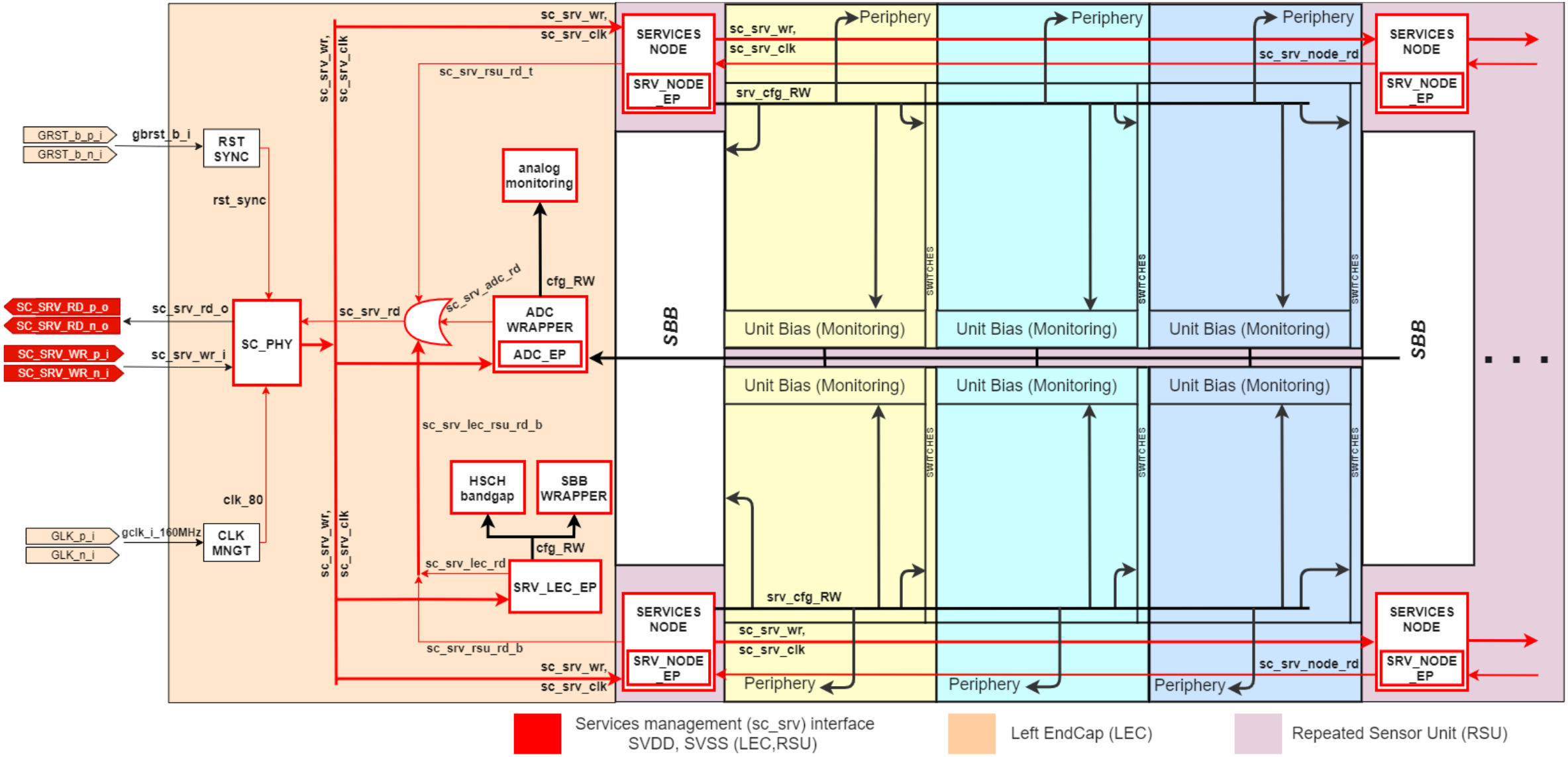
Service Slow Contol Block Diagram



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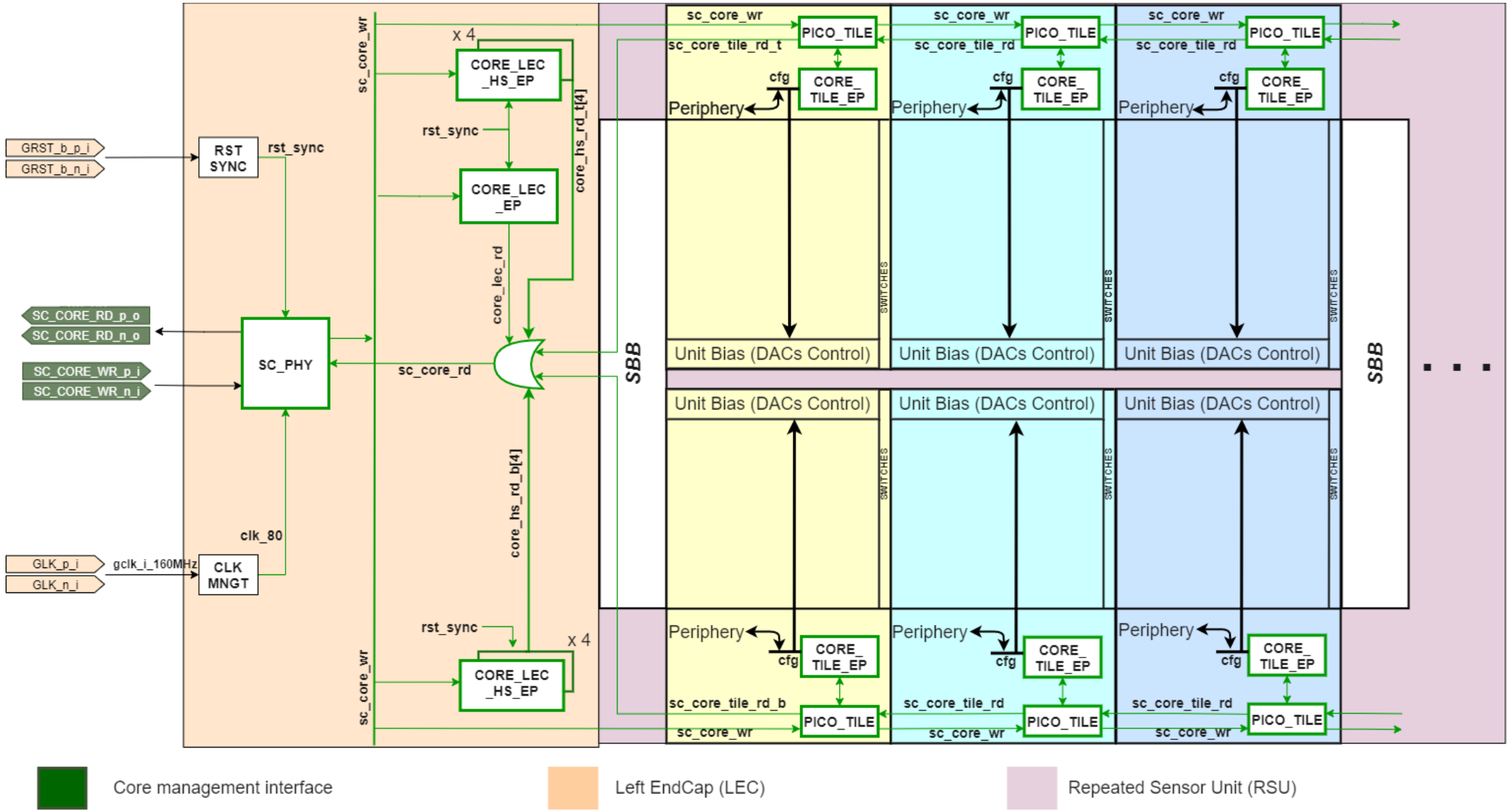
Core Slow Control Block Diagram



Core management interface

Left EndCap (LEC)

Repeated Sensor Unit (RSU)

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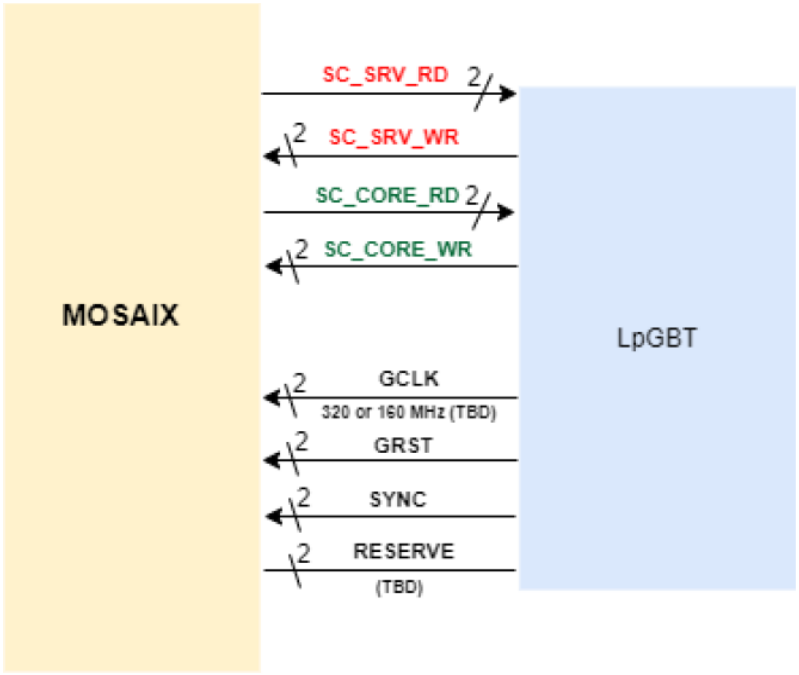
Control Interface

- **Services Management Interface:**
  - Reset management
  - Analog monitoring
  - Tile power switches and reset control
  - I/O configuration
  - Stitched backbone configuration
- **Core Management Interface:**
  - Readout control and configuration
  - Pixel matrix and bias configuration
  - High-speed channel operation
  - Tile and LEC logic control

Interface	Endpoint Flavor	# Instances	Broadcast	Description
Services	Services LEC	1	No	SBB and HSCH bandgap config
	Service Node	48	Yes	Tile reset, monitoring, power switch config
	Monitoring ADC	1	No	Analog monitoring ADC control
Core	Core LEC	1	No	LEC routing config
	Tile	144	Yes	Tile readout and matrix config
	High-Speed Channel	8	Yes	High-speed channel configuration

MOSAIX Slow Controls



Field ID	Field Name	Width	Description
A	HDR	4	Fixed 4bit (4'hA) value that indicates a start of transaction
B	RW	2	2bit field to indicate transaction type: b00 – WRITE_posted transaction, b01 – WRITE_non-posted transaction, b10/b11 – READ transaction
C	EP_ADDR	8	Endpoint Address
D	REG_ADDR	8	Register Address
E	REG_DATA	16	Register write or read data
F	PARITY	1	Transaction parity bit (bit-wise xor of RW, EP_ADDR, REG_ADDR and REG_DATA fields
G	STOP	1	Stop bit: 1'b0: Fixed 1bit (1'b0) value that indicates end of transaction

Slow Controls Physical Layer:

- CERN Low Power Signaling (CLPS)
- MSB first
- Manchester encoded
- 5 Mbps bit speed, 10Mbaud physical

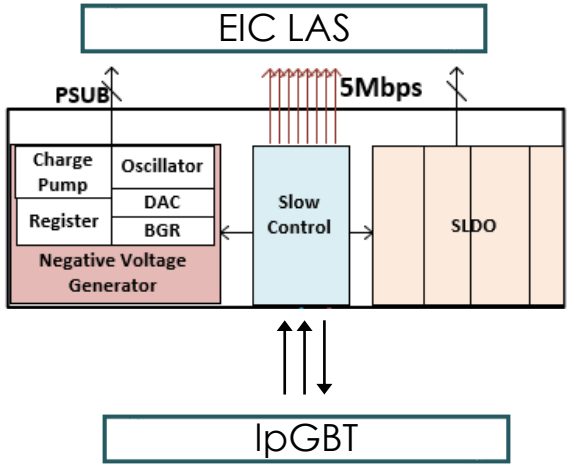
Transaction type	Direction	HDR	RW	ADDR	DATA	PARITY	STOP
WRITE_posted	Input to the ASIC	4'b1010	2'b00	Any valid register address	Data to write to the register	xor(HDR, RW,ADDR,DATA)	1'b0
WRITE_non-posted	Input to the ASIC	4'b1010	2'b01	Any valid register address	Data to write to the register	xor(HDR, RW,ADDR,DATA)	1'b0
WRITE-response	Output of the ASIC	4'b1010	2'b01	Register address as specified in the corresponding WRITE_non-posted transaction	Value of the register	xor(HDR, RW,ADDR,DATA)	1'b0
READ	Input to the ASIC	4'b1010	2'b10	Any valid register address	16'd0 (or 8'd0)	xor(HDR, RW,ADDR,DATA)	1'b0
READ-response	Output of the ASIC	4'b1010	2'b10	Register address as specified in the corresponding READ transaction	Value of the register	xor(HDR, RW,ADDR,DATA)	1'n0

Ancillary ASIC

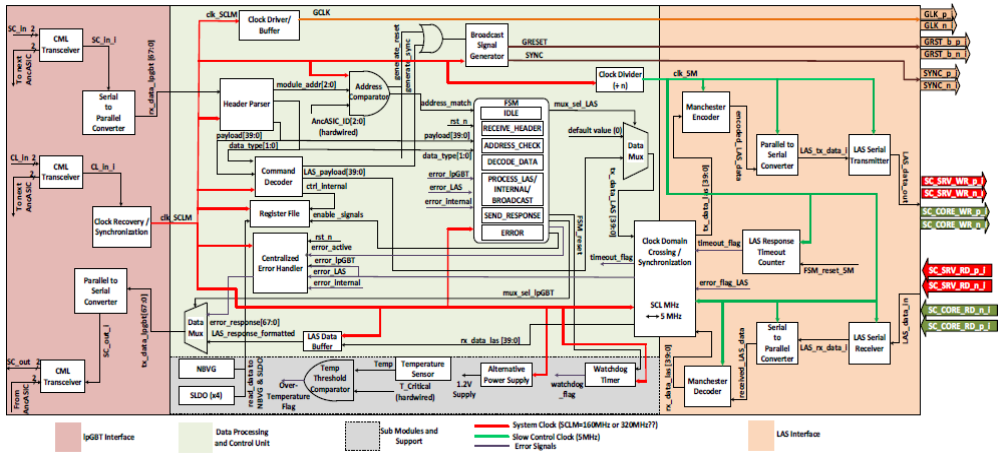
The Ancillary ASIC is designed to enable lightweight power distribution and signal transmission to the SVT for the OB, EE, HE

Being developed in a 110 nm SOI technology

- Shunt =-LDO (SLDO) regulators for serial powering
- Negative Voltage Generator (NVG) do deplete the sensor
- Slow Control (SC) interface between EIC-LAS and lpGBT



AncBrain block diagram



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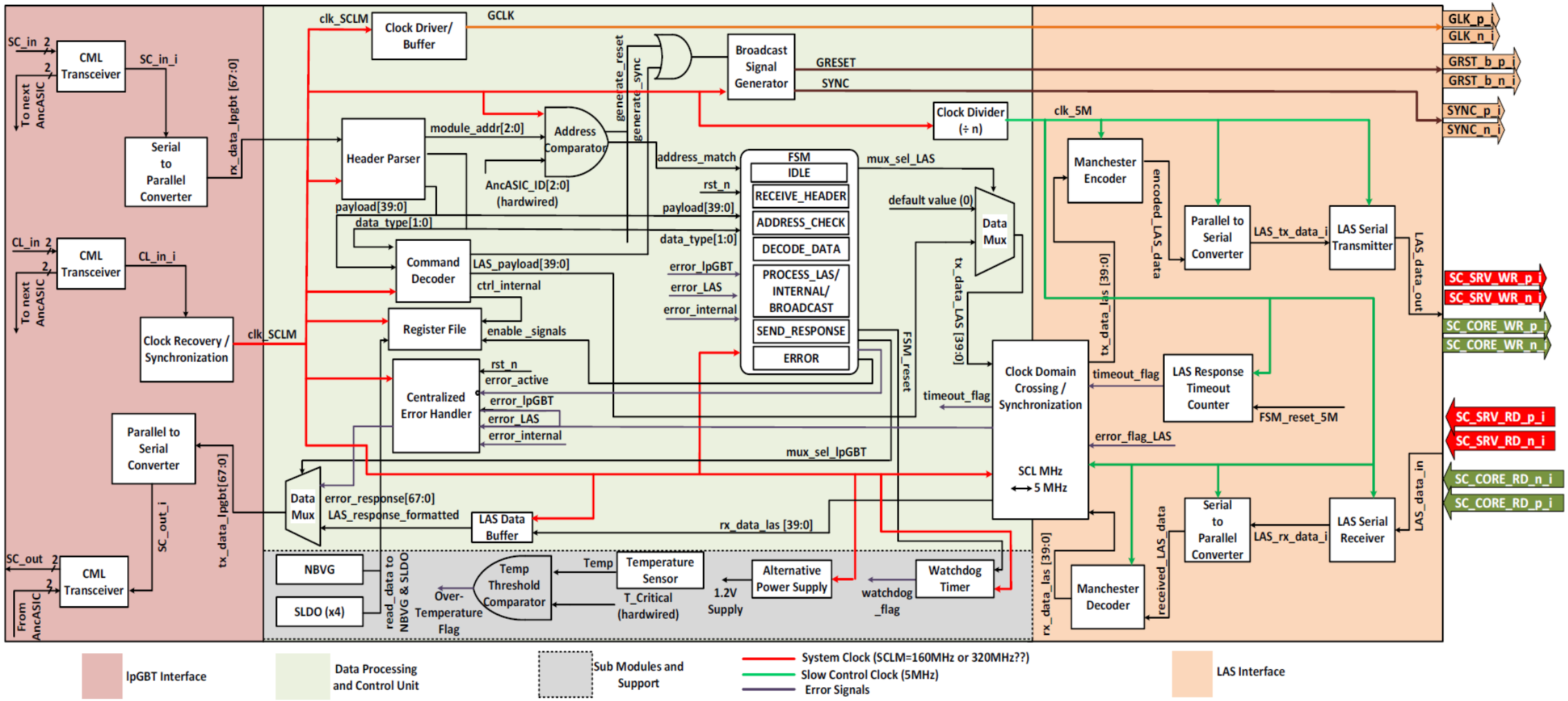
EIC AncBrain Block Diagram



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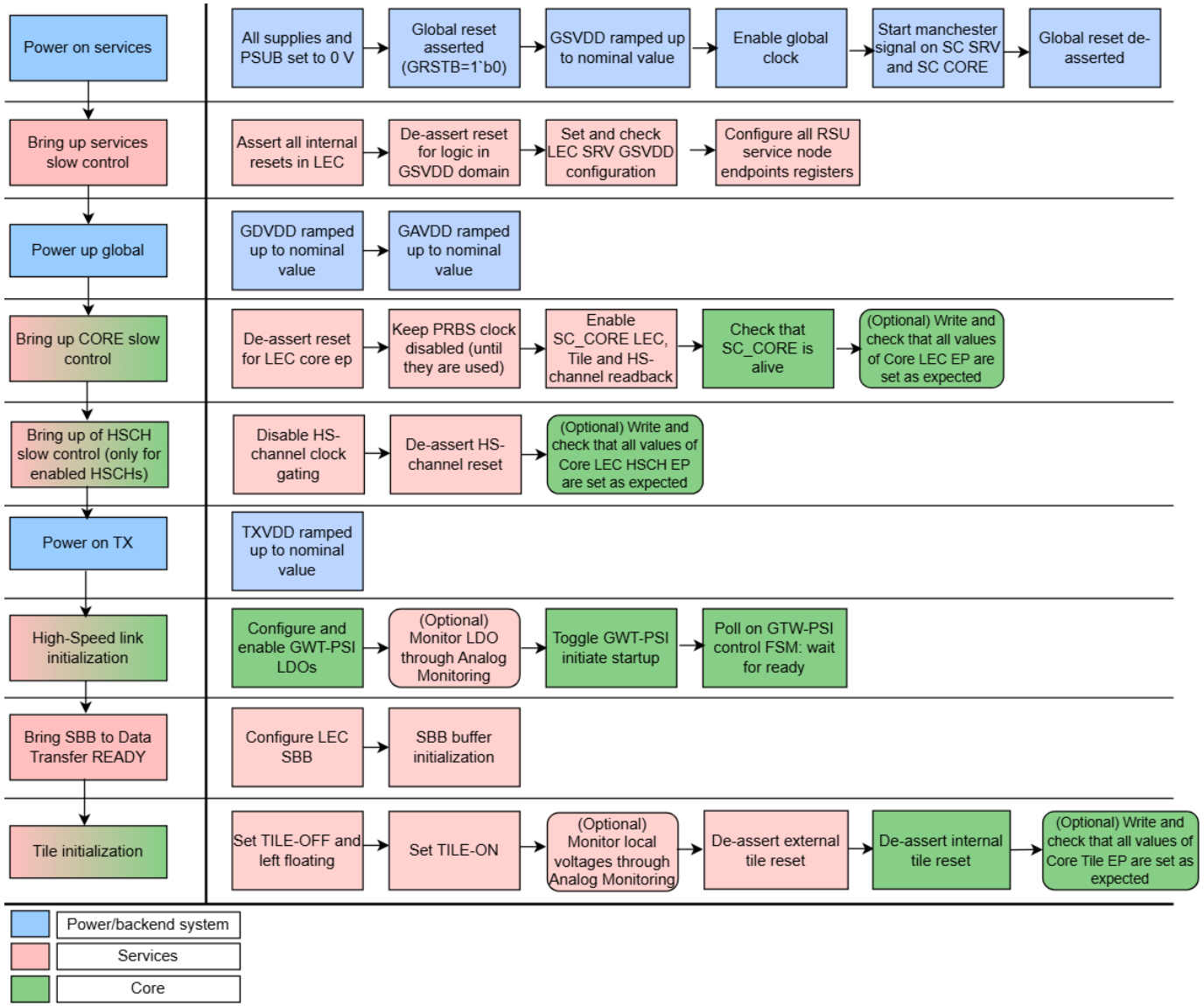
AncBrain Format

Field Name	Width (bits)	Description
Start of Frame	2	Predefined bit pattern to signal the beginning of a transaction (b01)
Module Address	4	Identifies the target ANC module within the daisy chain(0-7)
Data Type	2	00: Internal, 01: LAS Service Management, 10: LAS Core Management, 11: Reserved
40-bit Data Frame	40	Details in separate table. LAS or Internal
Frame Checksum (CRC)	16	CRC-16 for error correction
End of Frame	2	Predefined bit pattern to signal the end of a transaction (b01)

LAS Service or Core Data Format as in previous slide.
Internal:

Field Name	Width (bits)	Description
HDR	4	Fixed value (4'hA) indicating start of transaction
R/W	2	Transaction type: Write or Read
Register Address	8	Register address within the target sub-module
Control/Data	4	Sub-module control data or internal signaling
Parity	1	Transaction parity bit
Stop	1	Internal signaling (or reserved)
Unused	20	Reserved for future use

Power-up and Reset Procedure



Demonstrate Procedure times (Jupyter)

Calibration Procedure Estimates from Jupyter Notebook (1)

Configuration: The configuration transactions will be different for each RSU/tile/etc, no broadcast can be used to speed up the process, i.e. each tile is configured sequentially:

Posted:

	Bandwidth (MHz)	Transaction (s)	Pixel (s)	Tile (s)	Segment (s)
0	5	0.000008	0.000041	0.028052	4.039476

Non-Posted:

	Bandwidth (MHz)	Resync stages	Mean Transaction (s)	Mean Pixel (s)	Mean Tile (s)	Segment (s)
0	5	24	0.000021	0.000104	0.072381	9.554276
1	5	12	0.000018	0.000092	0.064069	8.457134
2	5	6	0.000017	0.000086	0.059536	7.858693
3	5	4	0.000017	0.000084	0.058024	7.659213
4	5	2	0.000016	0.000082	0.056513	7.459733
5	5	0	0.000016	0.000080	0.055758	7.359993

Configuration Scrubbing: To ensure that all pixels keep their configuration during a run, the configuration must be updated with regular intervals.

Posted:

	Bandwidth (MHz)	Transaction (s)	Pixel (s)	Tile (s)	Scrub cycle segment (s)	Scrub cycle segment weighted (s)
0	5	0.000008	0.000041	2.805192	403.947648	807.895296

Non-Posted:

	Bandwidth (MHz)	Resync stages	Transaction (s)	Pixel (s)	Tile (s)	Scrub cycle segment (s)	Scrub cycle segment weighted (s)
0	5	24	0.000021	0.000104	7.238088	955.427616	1910.855232
1	5	12	0.000018	0.000092	6.406920	845.713440	1691.426880
2	5	6	0.000017	0.000086	5.953556	785.869344	1571.738688
3	5	4	0.000017	0.000084	5.802434	765.921312	1531.842624
4	5	2	0.000016	0.000082	5.651313	745.973280	1491.946560
5	5	0	0.000016	0.000080	5.575752	735.999264	1471.998528

Monitoring:

	Bandwidth (MHz)	Resync stages	Monitoring cycle segment (s)	Monitoring cycle segment weighted (s)
0	5	24	0.26928	0.53856
1	5	12	0.25056	0.50112
2	5	6	0.24048	0.48096
3	5	4	0.23712	0.47424
4	5	2	0.23376	0.46752
5	5	0	0.23184	0.46368

Calibration Procedure Estimates from Jupyter Notebook (2)

Calibration: An example calibration run where the impact of a DAC setting is tested on all pixels of the sensor. A number of pulses are injected for each setting and data is read out. The calculation shows the time required to urn both assuming full parallel control of all tiles of a segment, and in the case of sequential control of all tiles of a segment.

Parallel calibration procedure estimates (s):

	SC Bandwidth (MHz)	Power (s)	Config (s)	Integration (s)	Readout chip (s)	Readout RU (s)	Total (s)
0	5	0.5011	64	568	92	424	1149

Sequential calibration procedure estimates (s):

	SC Bandwidth (MHz)	Power (s)	Config (s)	Integration (s)	Readout chip (s)	Readout RU (s)	Total (s)
0	5	72.16	9212	81838	13258	424	104804