FPC status

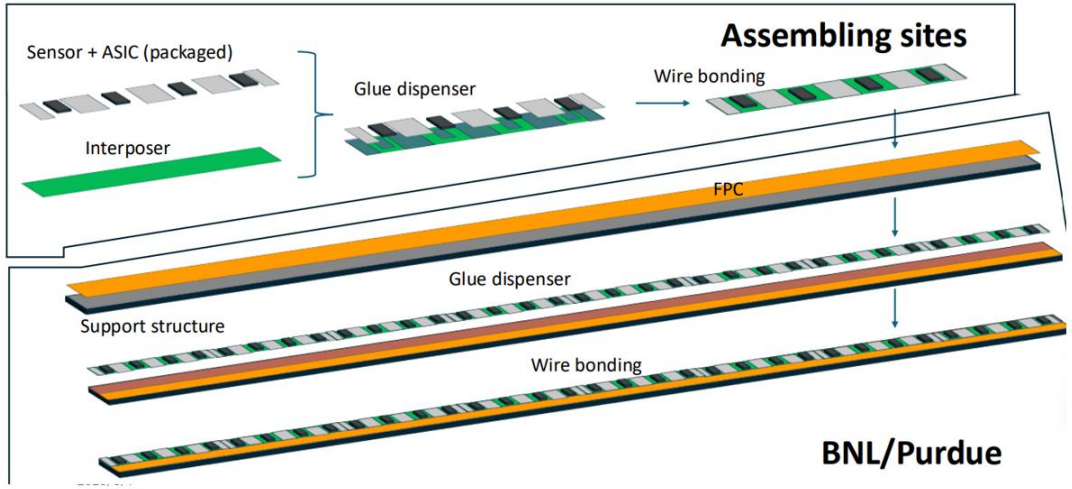
Takashi Hachiya
Nara Women’s University

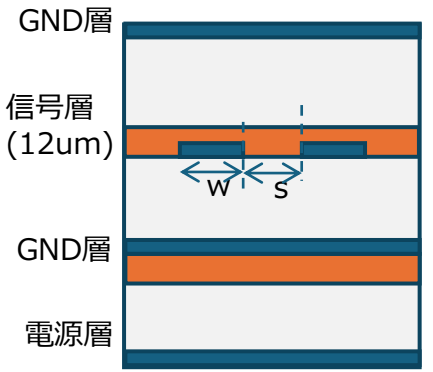
Line&Space test

- FPC design is constrained by
  - # of signal lines
  - **line&space for signal line**
  - # of LV & HV lines (layers)

- Need to know how narrow line&space can be made.
  - we are discussing with the manufacturer in Korea who has ability to make long FPC
  - We are testing 50, 70, 100um L/S for 130cm FPC (signal layer only) and will check uniformity of the line/space
  - We will visit the manufacture in Nov.

FPC design





接着シート
(25um)
LCP (100um)

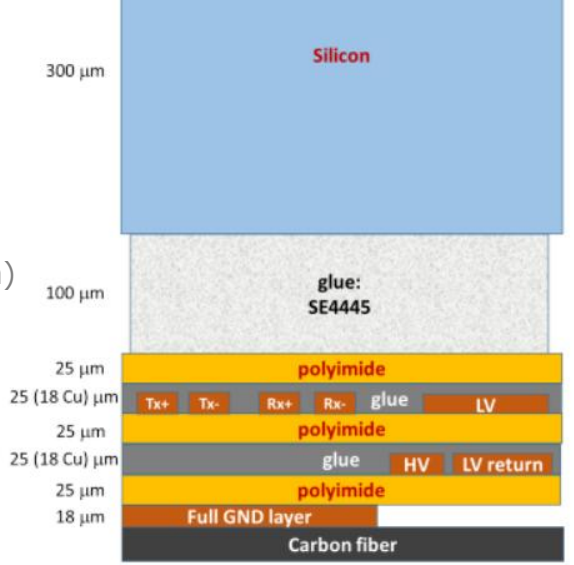
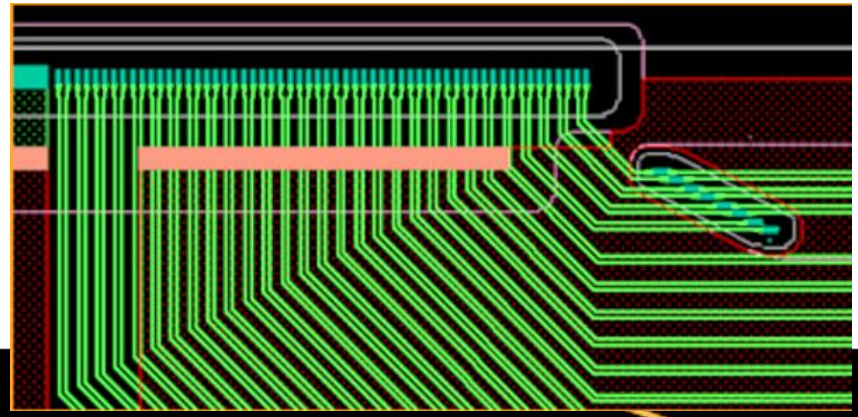
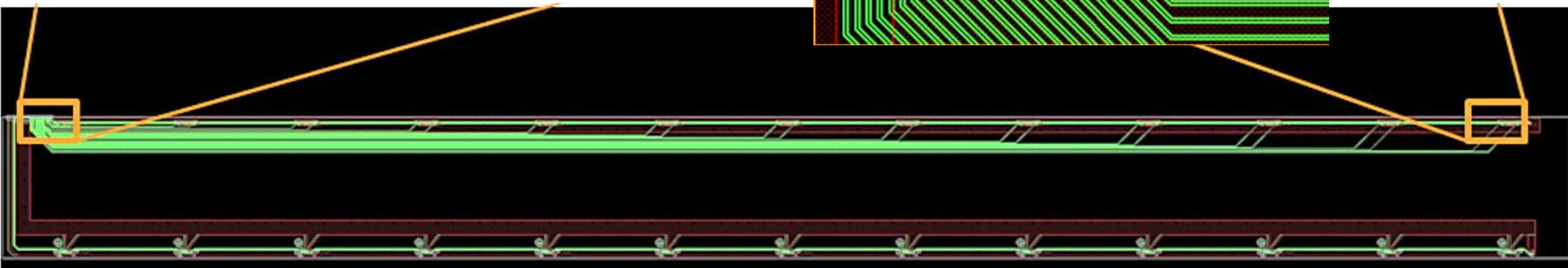


Figure 7. Recommended future bus tape stack-up.

- Consider ITK-FPC like structure
  - Integrate Signal, HV, and LV into a single FPC
- Needs for FPC design
  - Number and width of signal lines, #LV & HV)
  - Microstrip line? Strip line?
    - Strip line offers better signal quality but increases

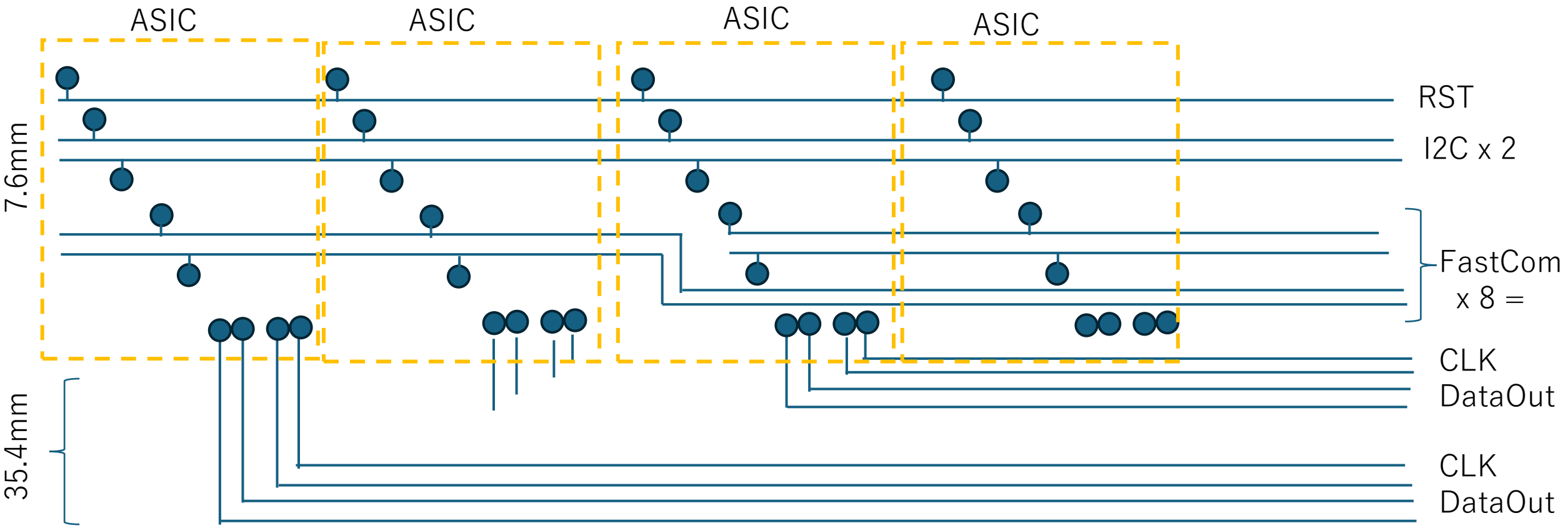




#Signal lines based on ETROC2

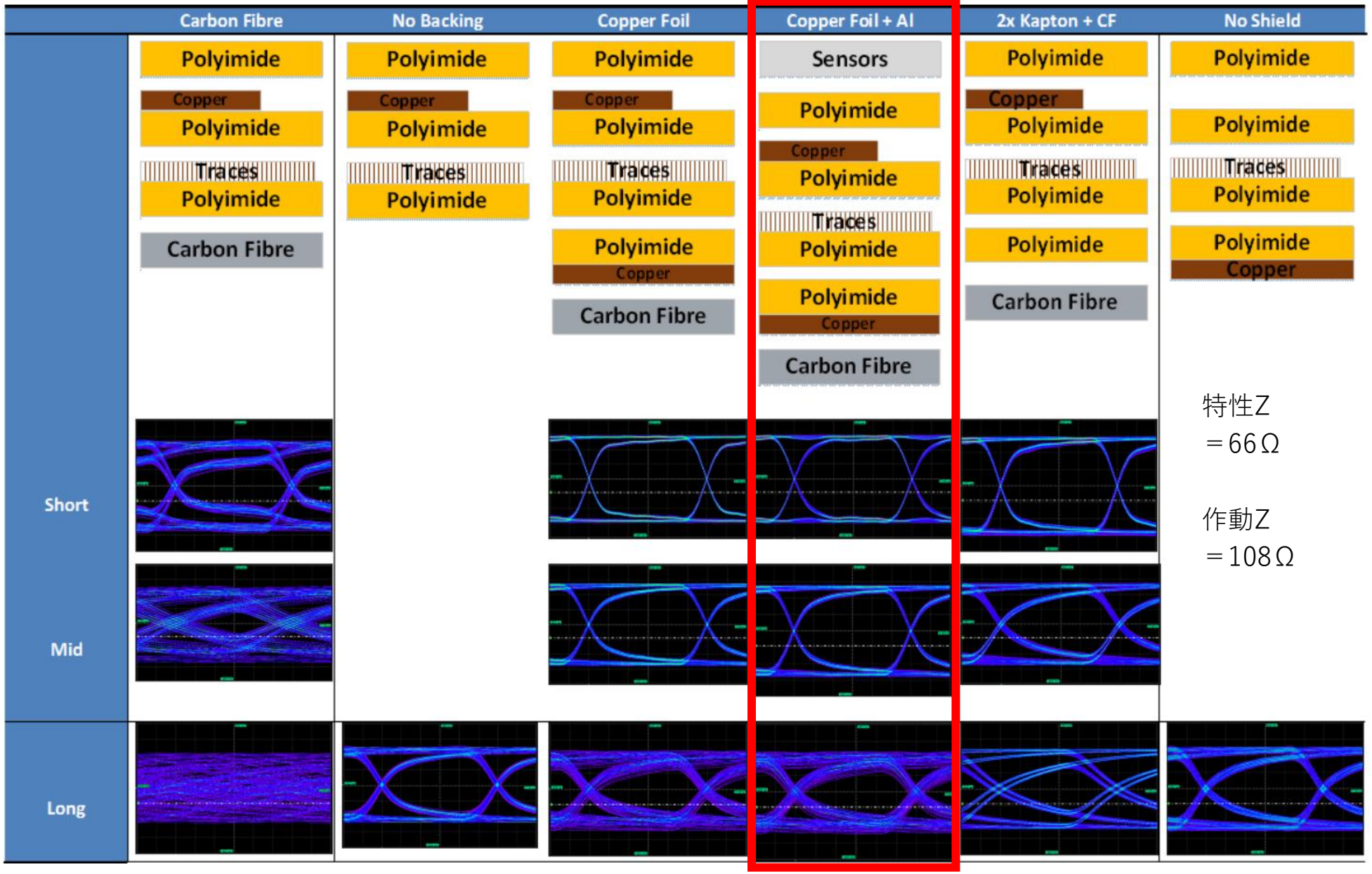
- Nsignals:
  - Digital lines:
    - Tx: 1x DataOut (pair = 2lines) -> p2p
    - Rx: **CLK40** (**pair** = 2lines) -> **p2p**
    - Rx: **FastCom** (**pair** = 2lines) -> **4 chips shared**
    - Rx: **I2C (2 lines, SCK, SDA)** -> **16 chip shared**
    - Rx: **RSTn (1 line)** -> **all chip shared**
    - Rx: I2C addr (5bits)
  - Analog : 1 line (Vtemp) -> p2p
  - 130 cm FPC = 32 ASICs/FPC（x2 FPC x 2cm/sens）
- # of signal lines for 32 ASIC's in a FPC = 32 x {2 + 2 + 2/4+ 2/16 + 1/32+1} = 177
  - -> if assuming the width of signal line = N, 177*(N*2) = (2 from line& space)
  - if N=100 (70) um, 177*100*2 + 1.3(ランドや余裕) = 4.6cm (3.2cm)（5.6cm is maximum width of FPC）
- Power lines : LV(1.8V), GND, HV.
  - There was no quantitative discussion in the past. How many sensor is a HV line shared? One HV line or multiple lines or one for each? Each stavelet? 8 stavelets for one FPC ?

Strawman ideas of routing the signal lines in FPC



- Line arrangement in signal layer : No cross-over of lines arrowed
  - Line (N-um) + space (N-um) + Land (for thru hole, N*2 ~ 4 um)
- Thru hole width : ~ 8.8mm (0.6mm*7+ 0.52mm*8 + 0.6mm = 4.2+4+0.6)
- Line area width: 32 * 4 * (2*N-um) =
- Land for powers and GND are also necessary

~44.2mm :
signal lines occupy < 5cm width



0.3% 0.3% 0.5% 0.5% 0.3% 0.3%

特性Z
＝66Ω

作動Z
＝108Ω

Cu:18um (0.13%)

PI:25um (0.01%)

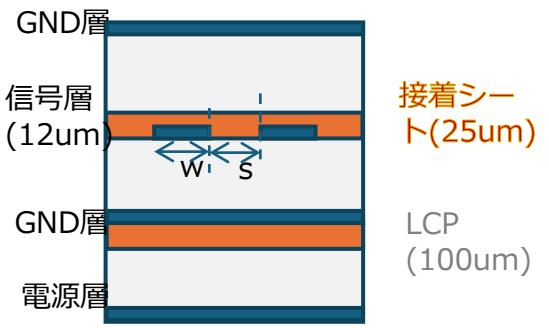
Glue:25um (PIと同じ)

L/S = 100um

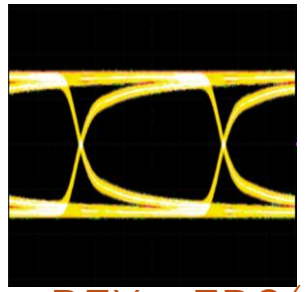
物質量少ない理由

- マイクロストリップ構造
  - 電源、GND層で挟んでいない
- スルーホールがないのでメッキしていない

INTT BEX



4層は接着剤によって張り合わせている



特性Z
＝47Ω

作動Z
＝93Ω

130cm BEX＋FPC(20cm)

Lessons learned in high frequency data transmission design: ATLAS strips bus tape
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