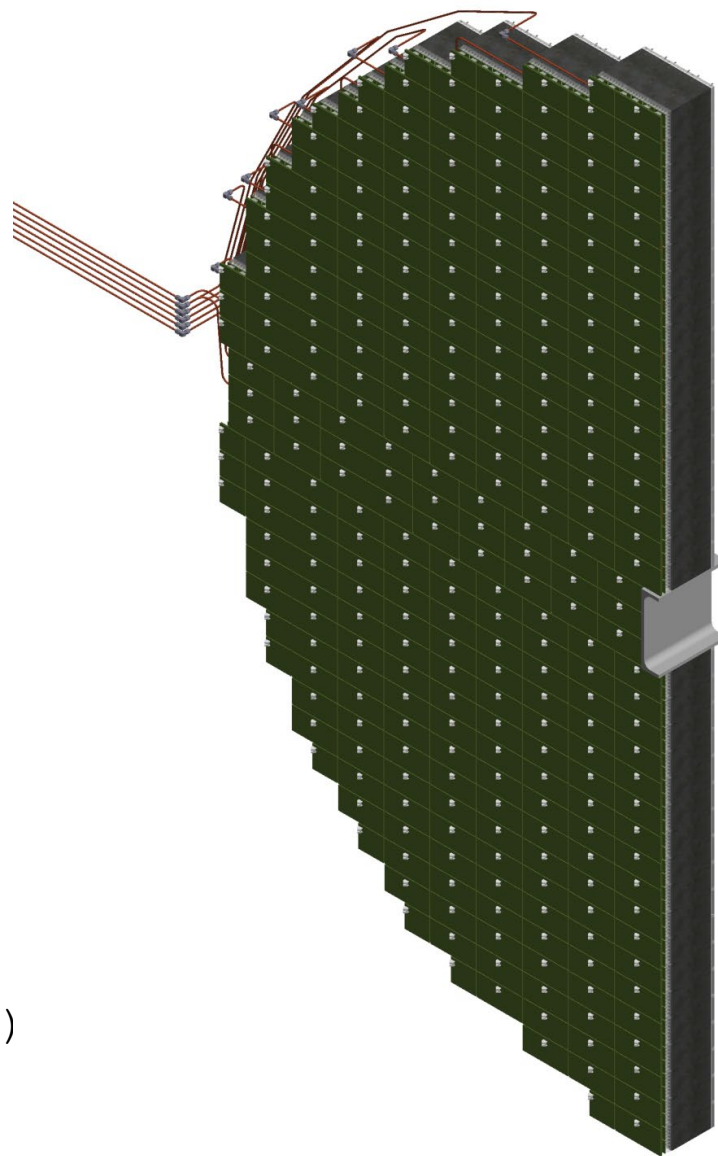


eRD109 COTS Waveform Readout FEB – update Nov 6, 2025

G. Visser, Indiana University



FEMC:

1145 blocks, 18320 channels

551 'regular' 32-ch FEB

43 'mini' 16-ch FEB (some outer locations)

38 RDO (16-FEB ea.)

J. Harvey

Recent work / work-in-progress / next steps

- SiPM dark count noise hit rate simulations – basically done now except need to rerun finer grid
 - Akio (BNL) putting this together with physics and beam-gas hit rate simulations
 - Rates per FEB should be available soon (December) → Jeff
 - Thresholds need to be raised at higher η – subject of discussion at upcoming TIC meeting (Sasha, Oleg)
- Reviews (Electronics PDR & FEMC PDR)
 - No concerns on FEMC SiPM & FEB plans
 - Recommendation to directly verify effect of dark count fired pixels on effective PDE, i.e. pixels fired by dark counts are not available to see real signals – setting up to test this at IU (December?)
- Production cost estimates for FEMC FEB and for FEMC SiPM board – work in progress
- bPOL48 prototyping
 - chips received from Norbert (thanks!); planning a small test PCB with new EPC23104 GAN chip (expected much superior for small loads, compared to bPOL48 “standard” EPC2152)
- Two-channel prototype layout: *Converting unfinished layout from obsolete P-CAD to kicad*
 - It’s an effort, mainly for parts library creation, but finally decided it’s unwise to keep using obsolete tool
 - I hope to finish this layout in a couple more weeks
- SiPM bias regulator board preparation for EEEMC DESY test beam (Dec 8th – 19th , attending in person)
 - Will connect to same preamp boards as last time, with CAEN V1725S 14-bit 250 MSPS readout
 - Hope for better results compared to Feb. test beam (bias unstable perhaps, other mysteries, snafu’s)