FCFD status

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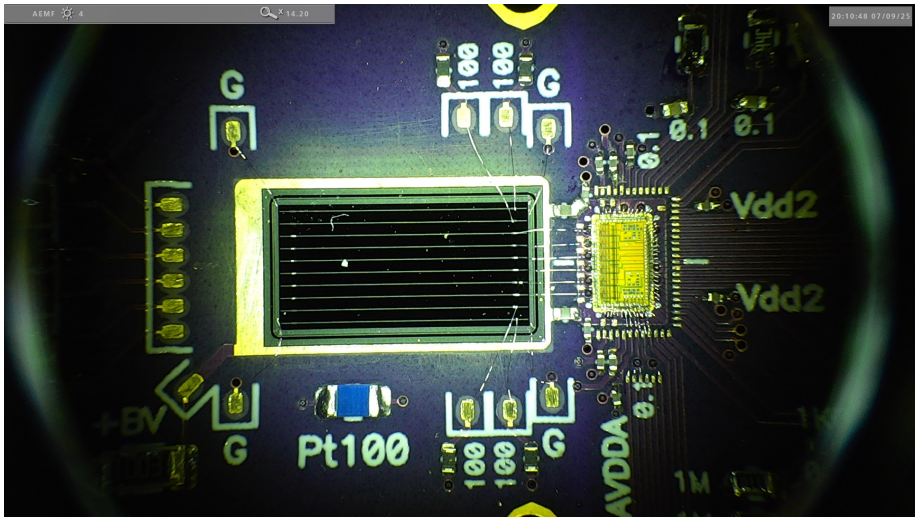
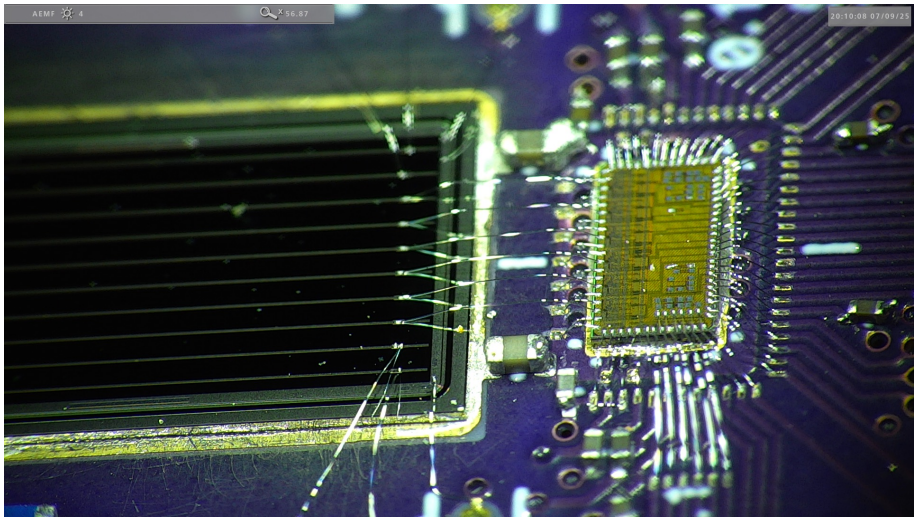
FCFDv1.1 testing status

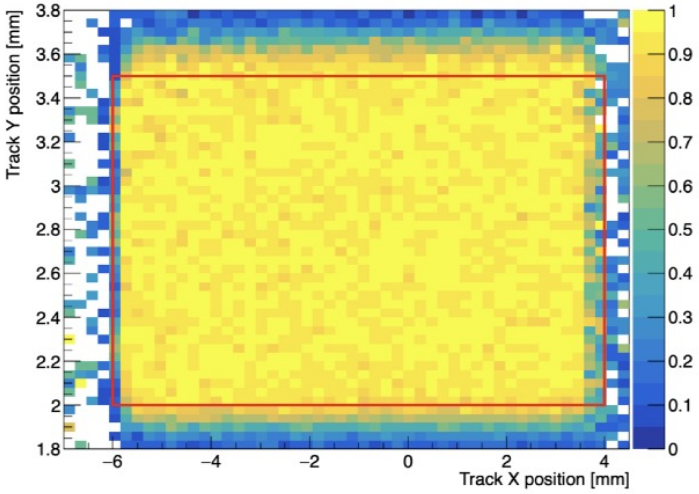
- Chip was received in Fermilab in early June.
- Mounted on testing board and testing started immediately
  - Wirebonded to a HPK 1-cm strip sensors, 6 strips connected
  - Sensor specs as we agreed in the previous presentations
- Test-beam campaign in DESY and CERN in Summer 2025

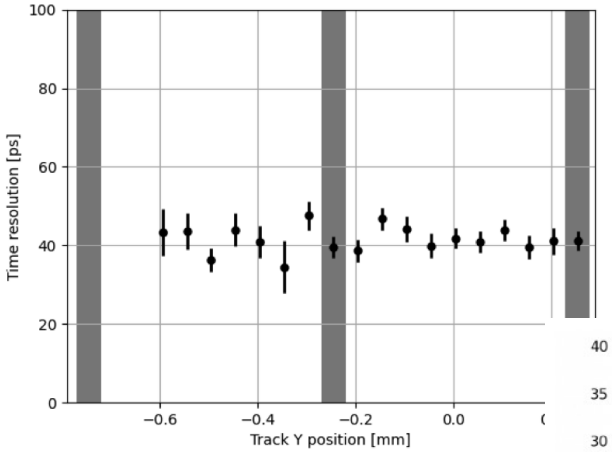


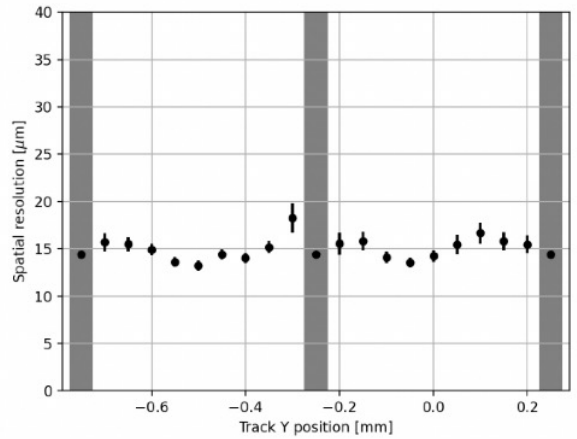


Test beam measurements with FCFD1.1

- Performance of the front-end matching specs
  - Measured **time resolution ~40 ps** across sensor surface
  - Measured **spatial resolution ~15-20 µm**
  - Fully efficient across the sensor surface

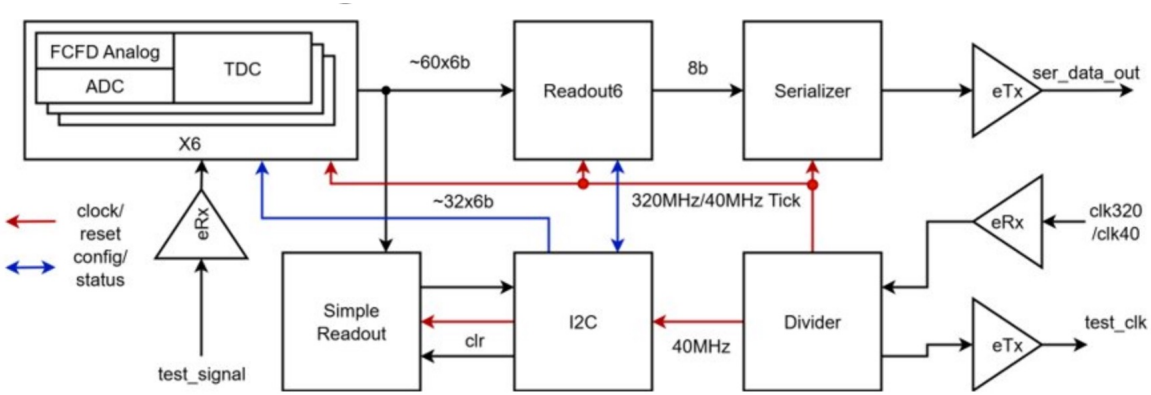


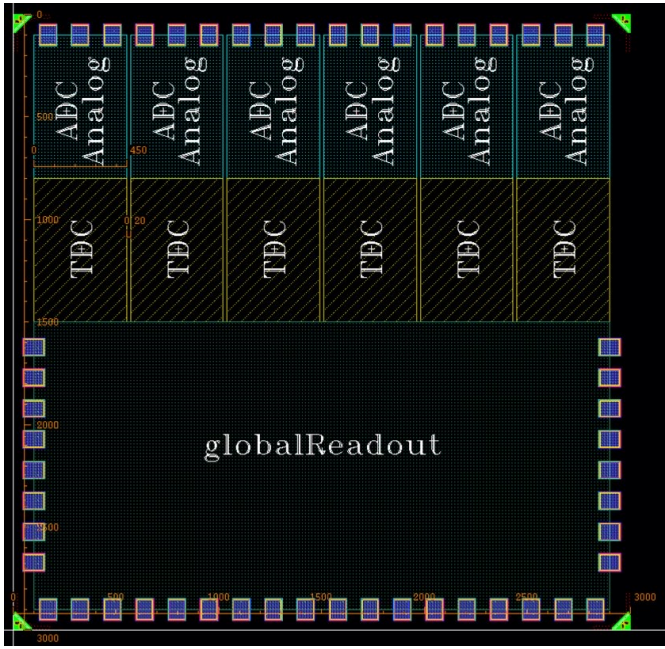




Design status for FCFD1.2

- FCFD1.2 will implement TDC, ADC, I2C, and simplified readout on a 6-channel chip
  - Goal is to verify all required main components on a small-scale chip





Floorplan and I/O

Fermilab

Design status for FCFD1.2

- Status of various blocks
  - Analog front-end unchanged from FCFD1.1
  - Design of the TDC, I2C and Divider is complete
  - ADC design is nearly complete
  - Data format defined
  - Work on power distribution is ongoing
  - Work on floorplan and PADs is ongoing
  - eTXs and eRXs are from CERN IP, these only need integration
- Next priorities:
  - Readout and Serializer designs
  - Started verification of completed modules