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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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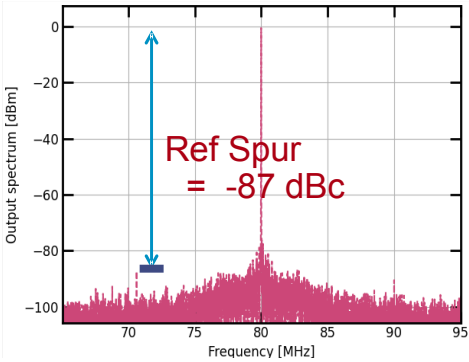
STATUS OF THE PROTOTYPES

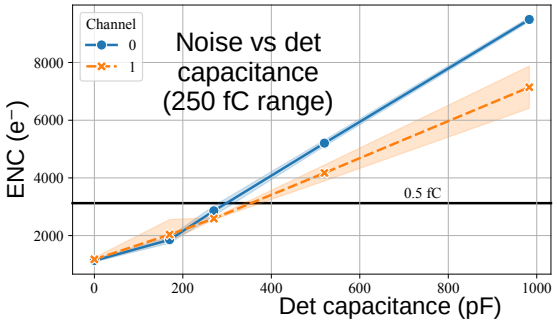
PRISMEv1 prototype (PLL test chip)

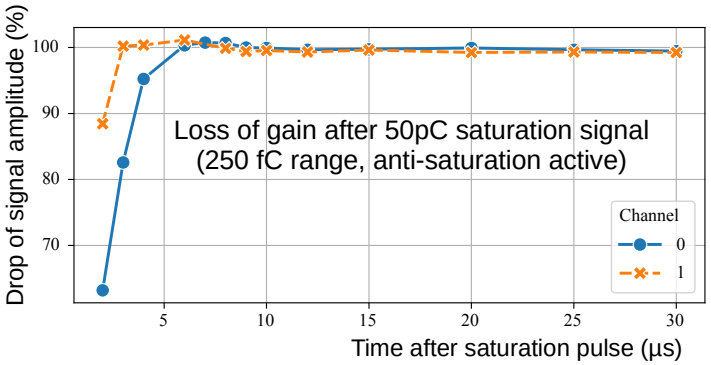
- Test finalized excepted radiation
- Main results
  - PLL phase noise between 1.5 and 2.5 ps, even improved to 1.1-1.3 ps with THCP technique (Track-and-Hold Charge Pump)
  - less than -120 dBc/Hz in-band noise
  - -87 dBc of largest harmonic compared to main 80 MHz carrier (reference spur)
  - 6.2 mW power consumption (PLL only)
- Radiation tests foreseen in November postponed to March (BPOL12 problem)

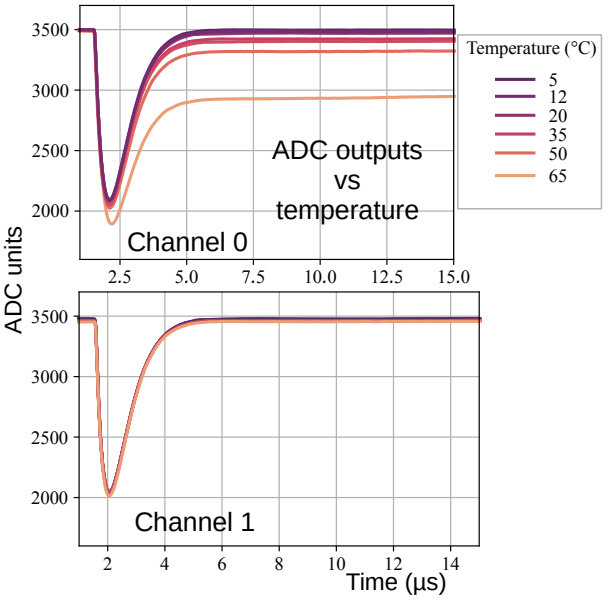


SALSA1 prototype

- Further studies done on noise and saturation
- Temperature tests between 5 and 65°C
- → channel 1 with less noise, more resistant to saturation, stable response vs temperature
- Radiation tests postponed to February







CURRENT STATUS: SALSA2

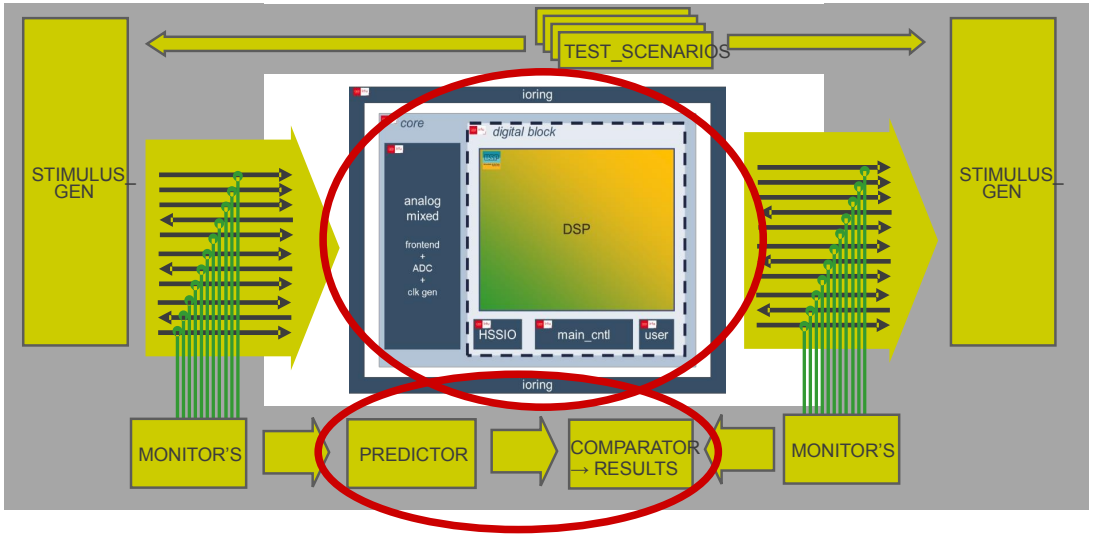
SALSA2 development status

- Corrections ongoing on RTL code
- Integration ongoing, some adaptations to be done on interface between DSP multiplexer output and high-speed link
- Development of digital test-bench and UVM environment, in order to play data in DSP and compare with golden model. Work ongoing on implementation of test functions in SALSA2
- Definition of floor plan in progress

Timeline

- Still a lot of works ahead:
  - code validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen beginning of 2026
- Tests end of 2026
- Distribution to users in 2027

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming beginning of 2026
- Beginning of SALSA2 tests → 2nd semester 2026

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 1st semester 2026
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

Very next steps

- SALSA1 tests → finalization of FE and ADC tests, TID tests in February
- PRISMEv1 chip → TID tests in March
- SALSA2 development → in progress