Report of the Global Timing Unit Internal Review

Performed at Jefferson Lab (Remotely)

Newport News, Virginia

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Table of Contents

Summary

The Global Timing Unit (GTU) internal review was set up to offer detailed feedback on the electronic design of the GTU prior to fabricating the first engineering article. The design was presented by William Gu according to materials available at https://indico.bnl.gov/event/30458. The reviewers would like to thank William Gu for the presentation. The reviewers note that the design is in an advanced state and will be ready to fabricate after incorporating recommended updates.

Reviewer Comments and Recommendations

1. The possibility that future upgrades of ePIC require supporting more than 120 DAM must be kept in mind. It is desirable if there is a path for expansion inherent in the design, this should be clarified.
2. The clock input receive circuit does not present a good termination to the input line. This is undesirable and can lead to unstable phase or jitter issues from reflections on the line affecting the waveform at threshold crossing. We advise changing the circuit design to have a good wideband termination (better than 10 dB to 500 MHz is suggested). External inputs should be buffered to decouple from PCB active circuitry. This should also be implemented to improve signal integrity where transmission line terminations are critical.
3. We agree copper clock / revtick input is a reasonable plan.
4. We recommend placing the clock / revtick input circuit on a small daughterboard rather than the main motherboard in order to eliminate the risk of revising the expensive main PCB if this interface changes in future, or if the circuitry has to be improved. (The present design with 'flaw' in input termination could be acceptable if it really is proven to work in practice, for instance, and this would be much less risky on a small inexpensive daughterboard.)
5. External copper interfaces, especially DC coupled ones, wherever possible, should not connect directly to FPGA pins. There are several motivations for the 'rule': Surges may latch up and destroy an expensive FPGA. FPGA differential receivers usually have poor and poorly specified CMR. All I/O analog specifications may not be as completely specified, leading to interface malfunctions later if something changes in system.
6. A jitter cleaner downstream of the master clock mux would provide a smooth transition from one clock to the next. This could be beneficial.
7. It is important - certainly GTU designers already have this in mind we know - that downstream electronics not crash after a GTU clock switch operation. It is OK / probably expected that some downstream electronics needs to be configured/reset after a small delay after a clock switch operation.
8. A precise frequency monitor of the ePIC clock is necessary. This can be a commercial frequency counter, probably it does not make sense to build this function into GTU, but a diagnostic output should exist to use for this. However, this precise clock value needs to be available to general Run Control as well as entered

in the database at Run Start time, so a device with e.g. ethernet readout is necessary.

9. A small/simple ASCII text display unit on the front panel connected to the main FPGA would be useful.
10. There are a number of LDOs on the main board – is cooling design sufficient? It's suggested to make power dissipation estimates for LDO's (and any other high power components), and consequent temperature estimates. The total power consumption for the chassis was stated to be around of 500 W: the power supply and cooling of the chassis must be well specified with the appropriate EMI rating (FCC Class B).
11. Add LDOs to provide power to sensitive circuits (low jitter/jitter cleaning clock ICs) instead of using ATX power directly. This benefits signal integrity by filtering and decoupling.
12. Check that power sequencing (between the external supplies) is compatible with the design. The FPGA daughtercards take care of most sequencing issues, but their I/O may still have some sequencing issues in the overall design. None identified.
13. Opto daughtercards may need some mechanical support. For the SFP versions they will be supported by the box panel, however that may not be in place for prototyping & development. Suggest adding some mounting hole or other feature on the opto daughtercard that could optionally be used for a support.