



IN2P3
Les deux infinis



EICROC status and plans ePIC collaboration meeting BNL 21 jan 2026

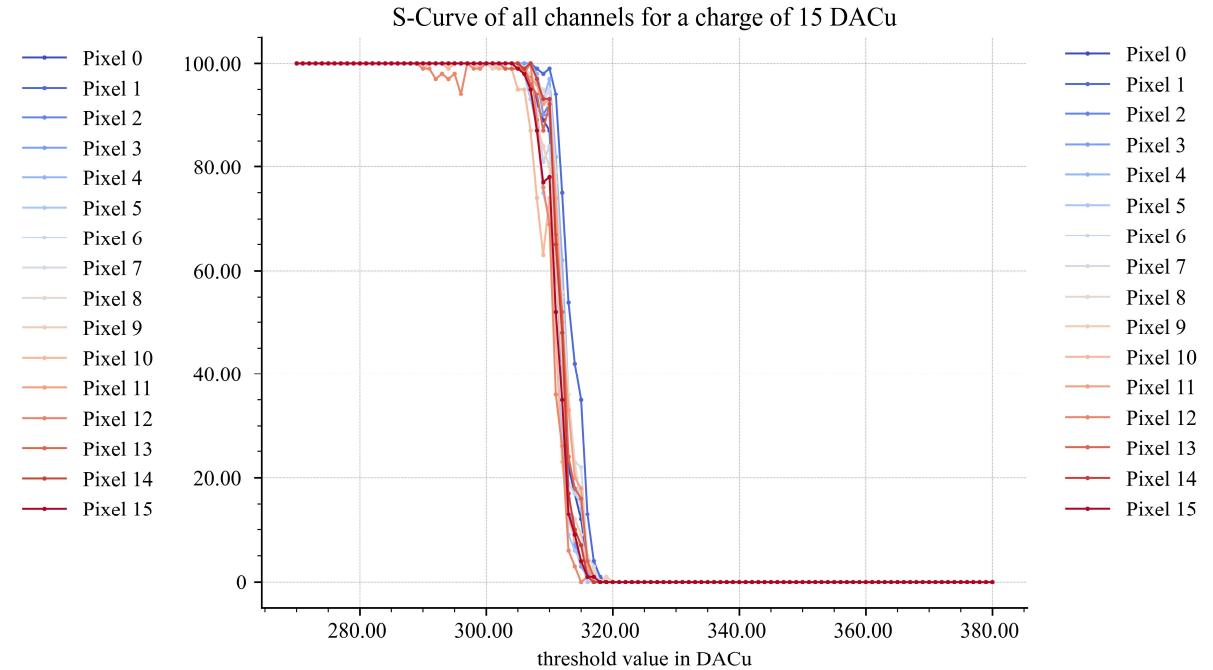
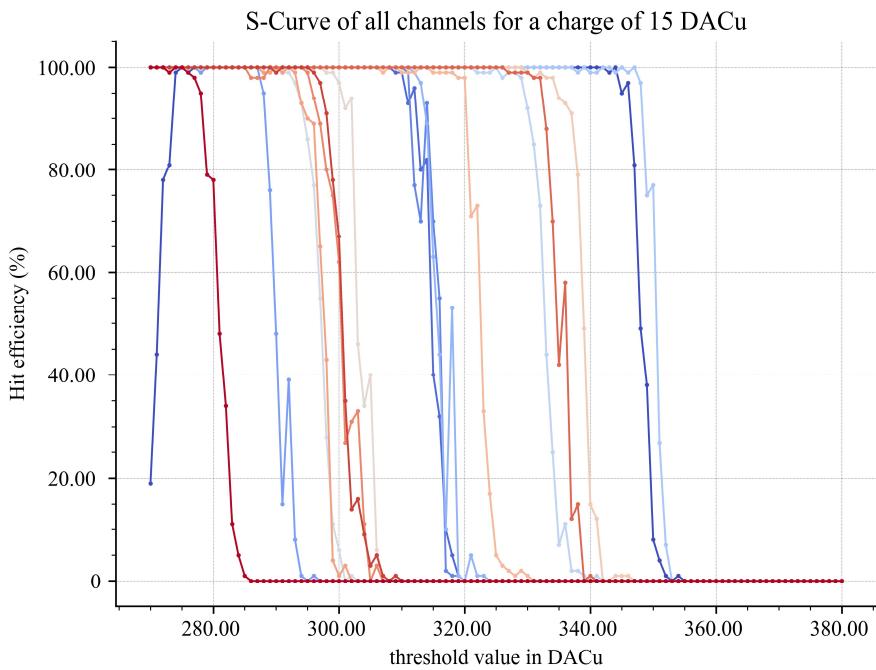
F. Bouyjou, H. Chanal, F. Dulucq, M. El Berni, S. Extier, M. Firlej, T. Fiutowski, K. Guillossou, F. Guilloux, M. Idzik, N. Kachkachi, B.-Y. Ki, C. de La Taille, J. Moron, D. Marchand, L. Royer, N. Seguin-Moreau, L. Serin, A. Shama, A. Soulier, K. Swientek, D. Thienpont, A. Verplancke

Organization for Micro-Electronics design and Applications



- 6-bit DAC for channel-wise threshold alignment

Correction of channels for a charge of 5 fC

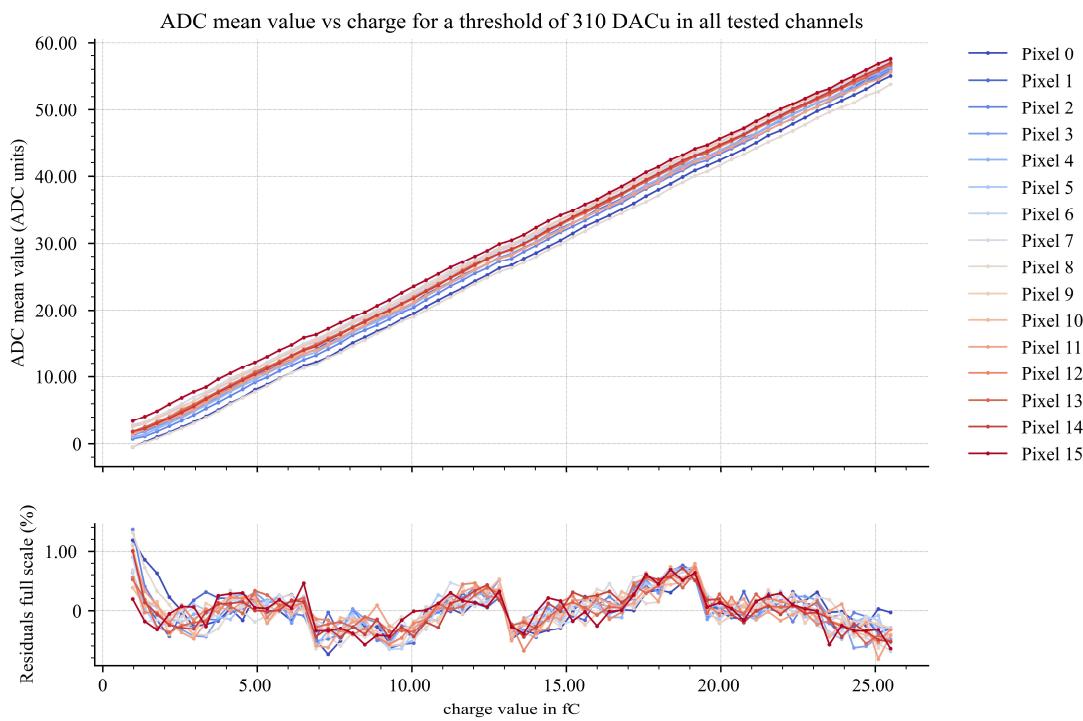


EICROC0 measurements : ADC linearity

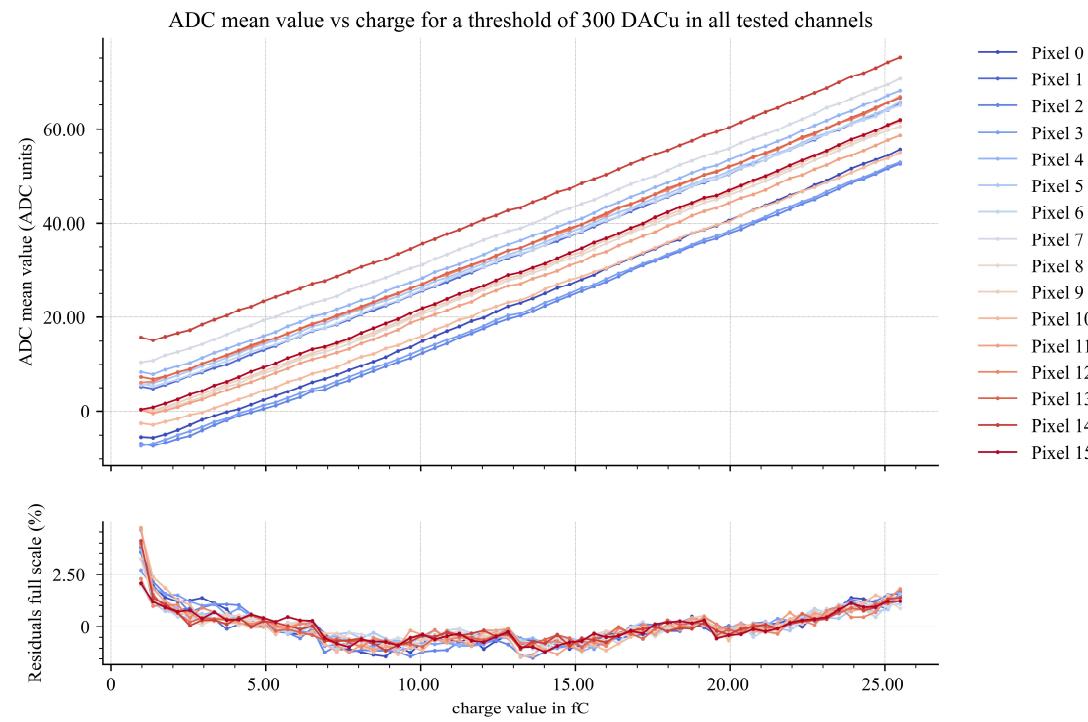


- 8 bit 40 MHz SAR ADC [Krakow]
 - Noise ~1 UADC but large common mode noise
 - Signal 50 UADC ~500 um => 1 UADC ~10 um

ADC mean & residuals – no sensor



ADC mean & residuals – BNL Flipchip sensor

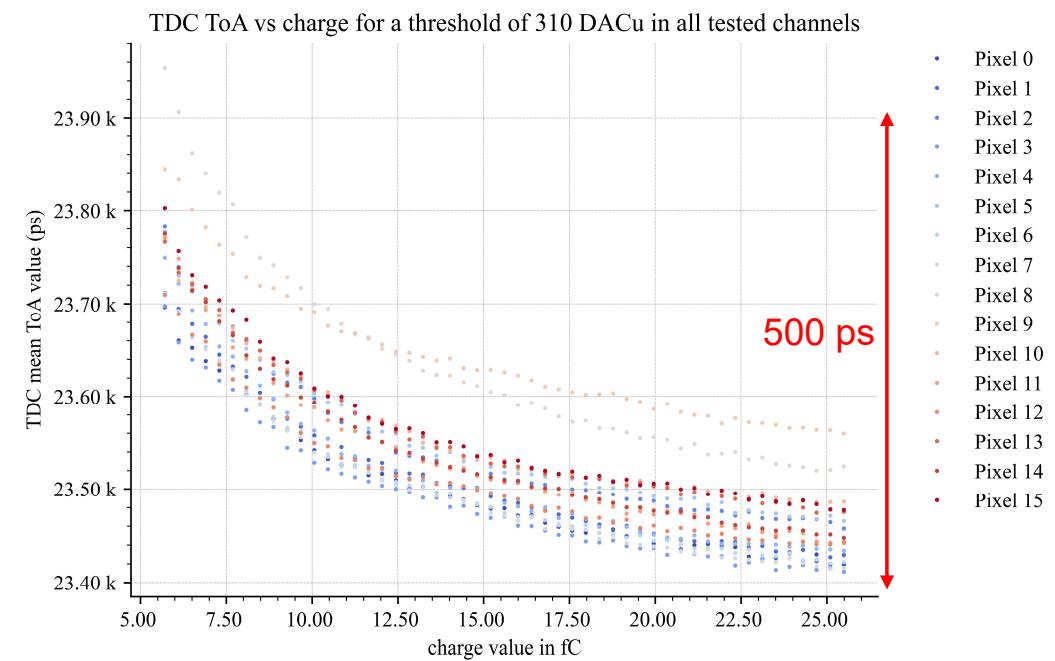


EICROC0 measurements : TDC ToA

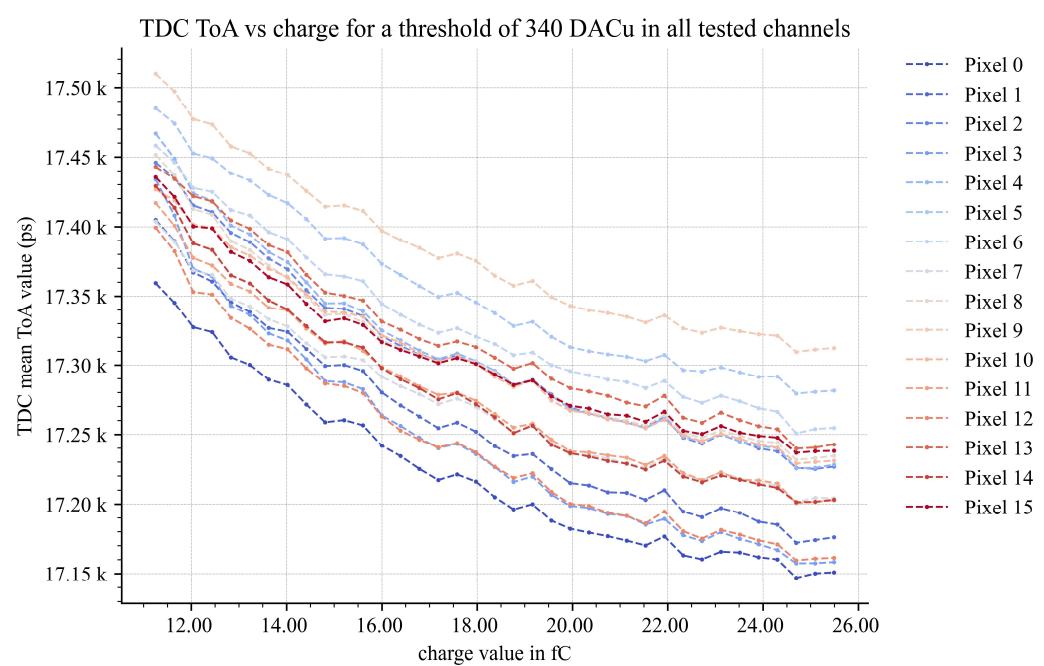


- Time walk measurement :~400 ps

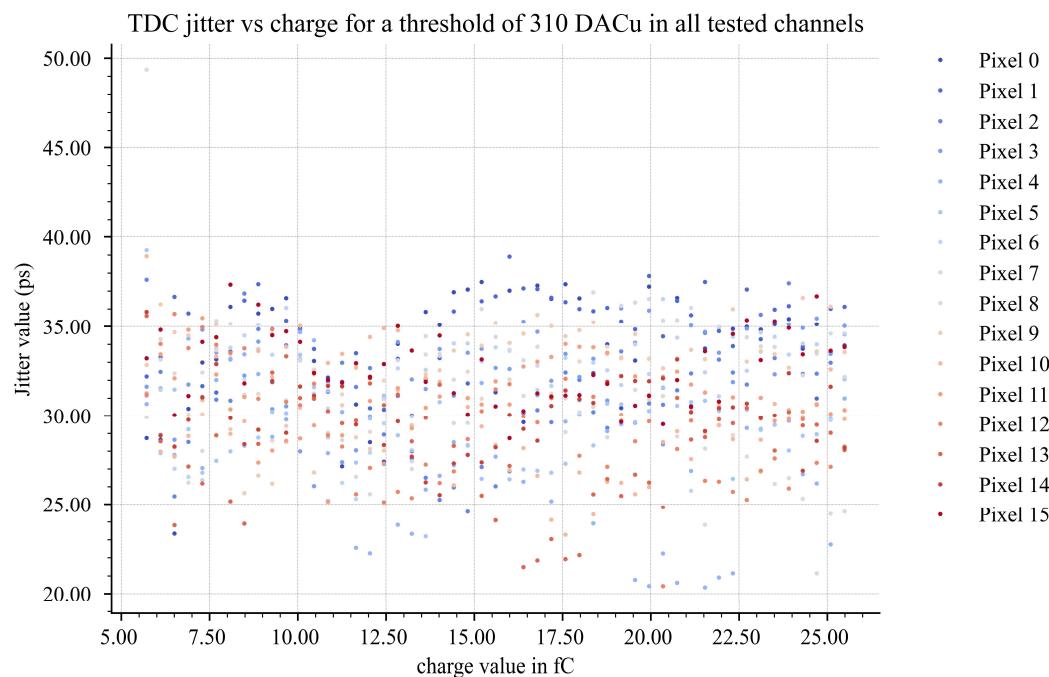
TDC ToA – no sensor



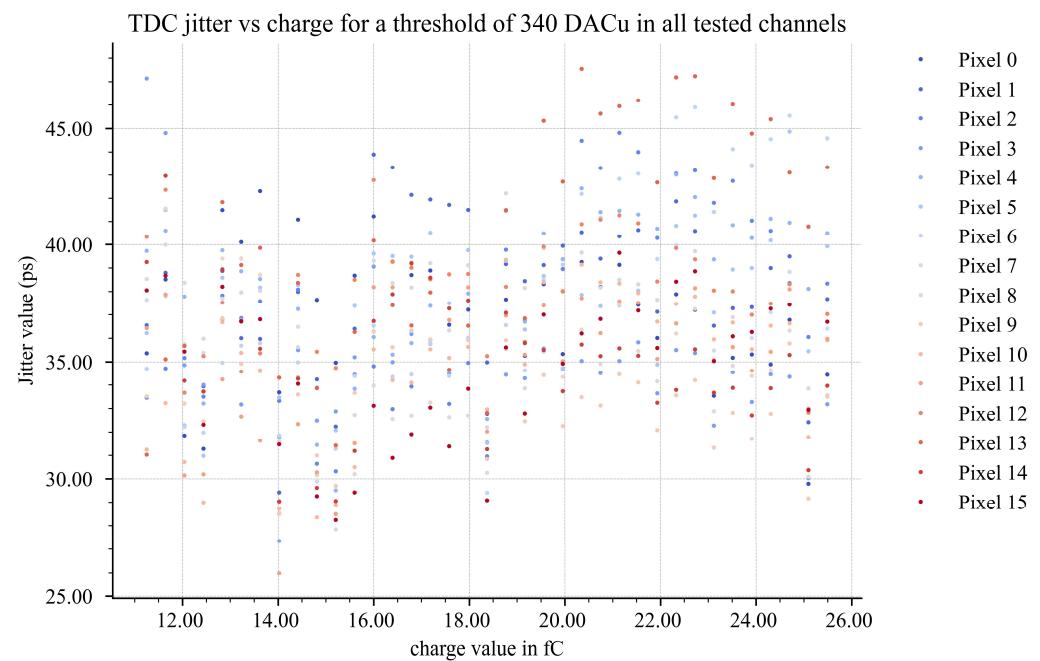
TDC ToA – BNL Flipchip sensor



TDC jitter – no sensor



TDC jitter – BNL Flipchip sensor

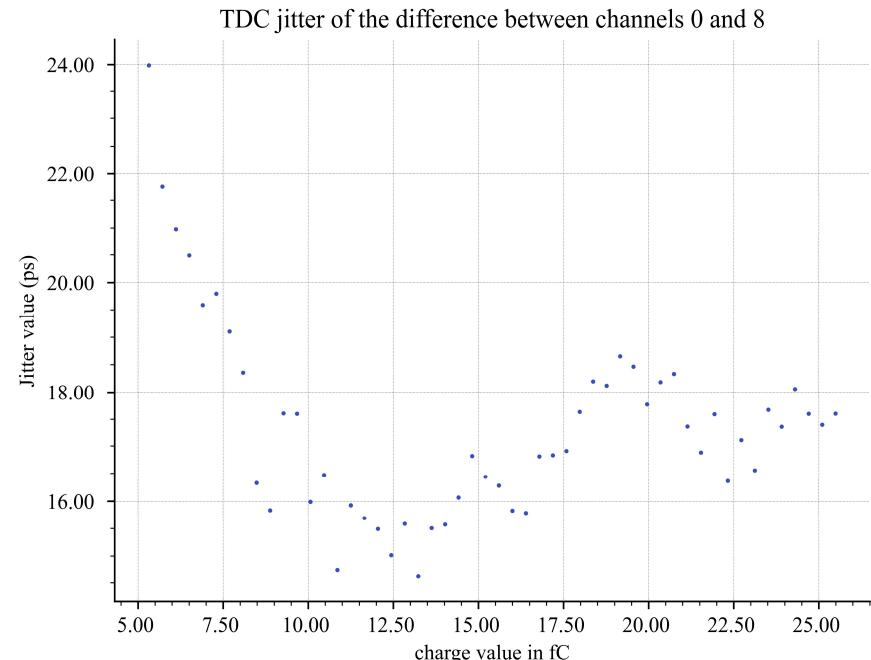
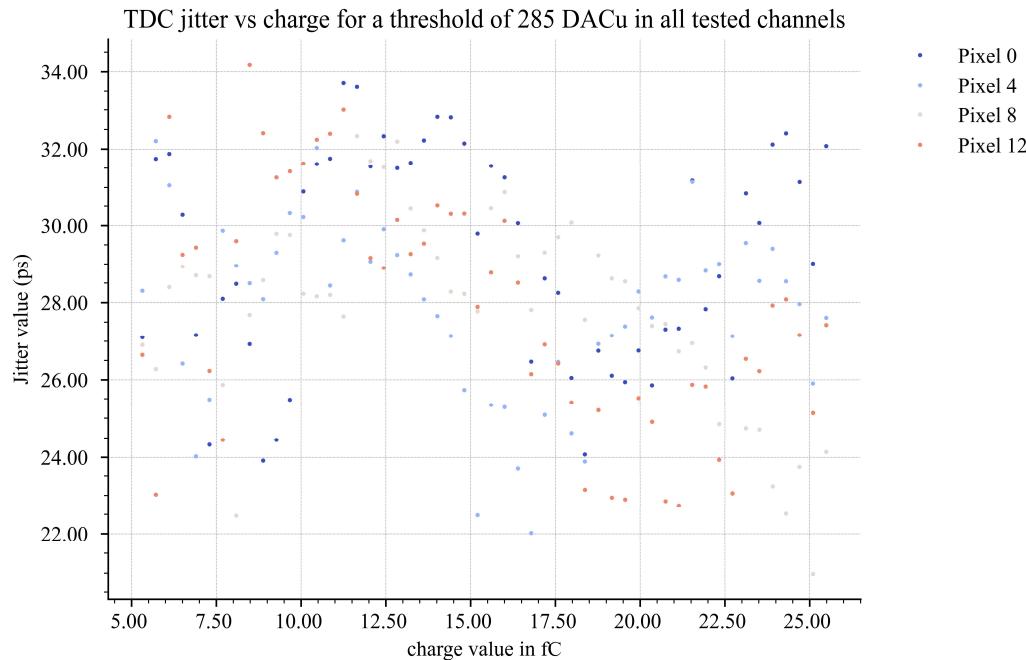


Charge range degraded with sensor, still need to properly calibrate the TDC for each channel and remove correlated noise

EICROC0 measurements : TDC jitter



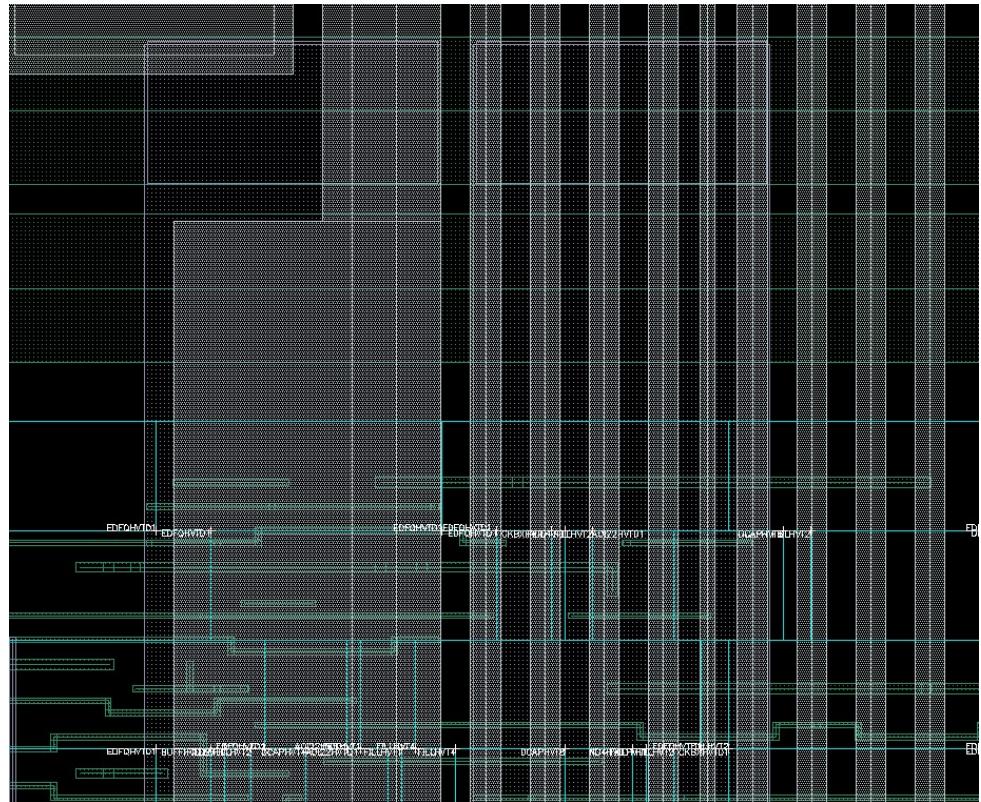
TDC jitter results for a simultaneous injection in pixels of line 0 (0, 4, 8, 12)



- We can also inject in channels simultaneously with the test pulse to then **remove the correlated noise** from the TDC measurements
- The plot represents the TDC jitter for the difference of two channels that we injected in simultaneously
- Performance approaching what is measured with the oscilloscope

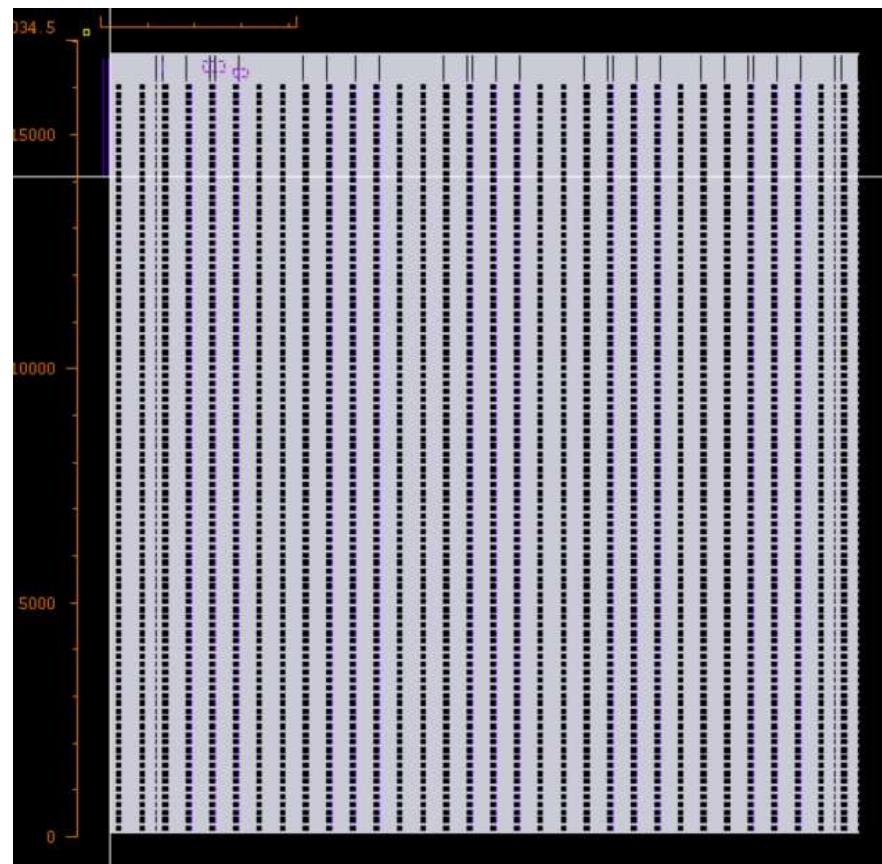
EICROCCO Coupling investigation

- Large coupling seen on the ADC data which was completely hiding the signal up to 20 fC
- Large coupling capacitance between local (pixel) digital block and preamp / shaper bias lines
- Layout improved by adding exclusion zones and a shield between bias lines and digital
- Done in EICROC0A

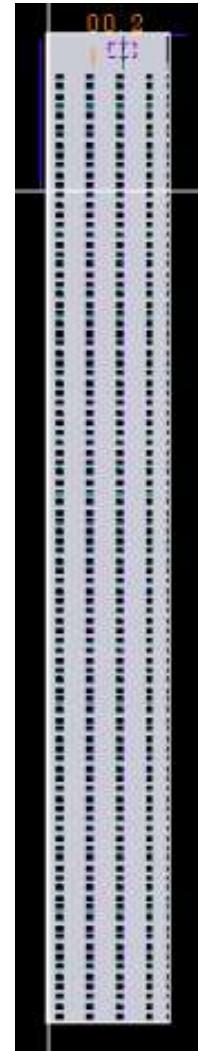


Bias / digital block layout in new EICROC ASICs

- 32x32 chip : final dimensions
- Goal :
 - test full-scale chip analog performance (IR drops)
 - Allow final sensor characterization
 - Test interface with DAQ : fast commands and 320 Mb/s data output
 - Progress on module/front-end boards
- Caveats :
 - Not (yet) zero-suppressed data
 - Still 2mW/ch
 - Still analog-on-top

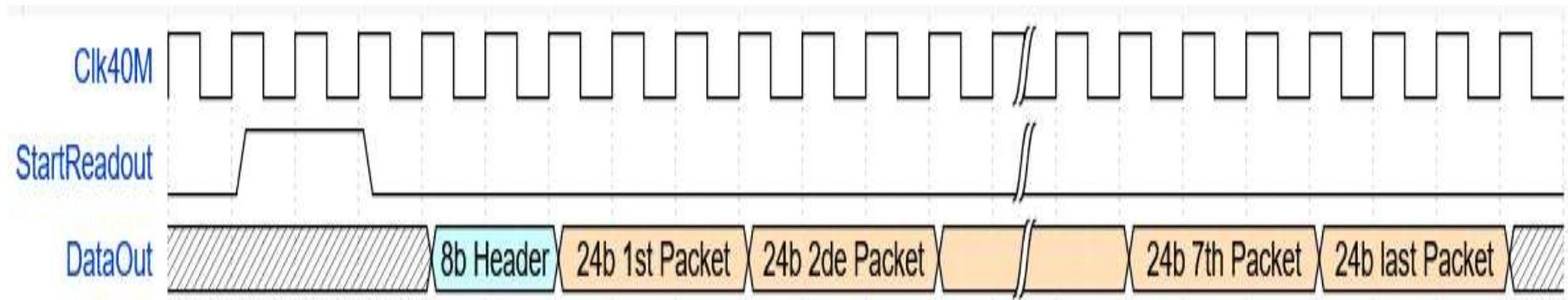


- Designed as 8 blocks of 4x32
 - Read out sequentially, like EICROC0
 - Pixel similar to EICROC0A
 - 8 CLPS outputs at 40 MHz
 - Clock tree for isochronous calib_pulse distribution
- Common balcony (End of column)
 - Biases and slow control
 - **New : fast command** decoder (clock, calib_pulse, enable_acquisition, start_readout)
 - Backup clock and cmd_pulse inputs available
 - **New : 320 MHz serializer** for 1 CLPS output



- Digital inputs
 - CLK_320 and FCMD (clock and fast commands) : CLPS
 - RSTb and RSTb_I2C : 1.2 V CMOS active low
 - SDA, SCL and 4b address : I2C slow control 1.2V CMOS
 - SEL_FCMD : 1.2V CMOS to select the backup inputs (below) (default fcmd)
 - Backup inputs : like EICROC0 (clk_160, cmd_pulse, en_acq, start_ro)
 - All unused inputs can be left floating (internal pull-ups/pull-downs)
- Digital outputs
 - 8 x 40 MHz data output (CLPS) by block of 4x32
 - one 320 MHz serialized data output (CLPS)
 - one trigger output (OR of all internal triggers) (CLPS)
 - One digital probe (1.2V CMOS) for debugging
- Analog outputs : for debugging (2 preamp outputs, analog probe, bias probe)

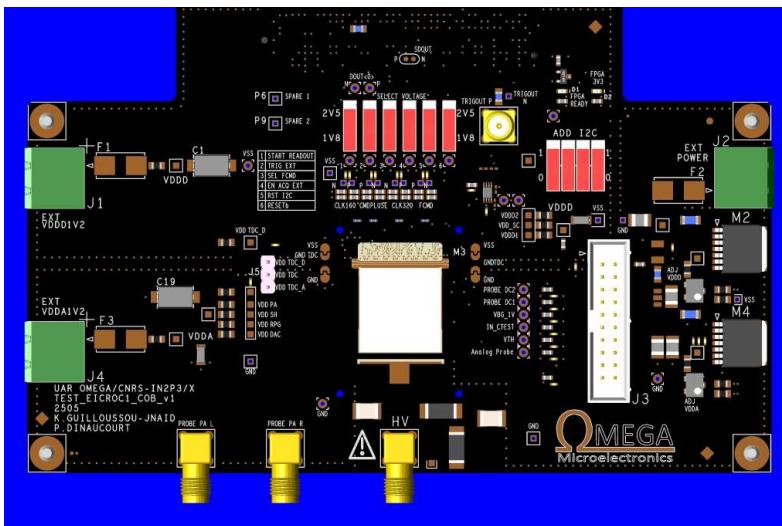
- Same as EICROC0 :
 - Data format : the 8 packets of 24 bits represent 8 successive samples of the data. One packet of 24 bits is ordered as followed : packet[23]=0, packet[22:12]=TDC[10:0], packet[11:9]=0, packet[8:1]=ADC[7:0], packet[0]=hit



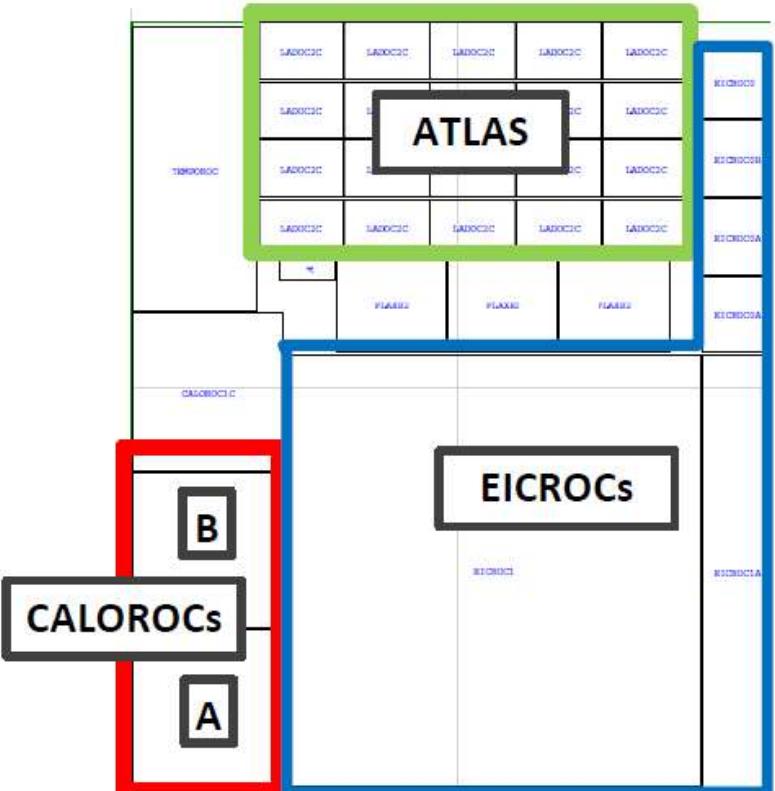
- Payload and readout speed
 - Each pixels provides 8 samples of 24 bits (12b TDC 12b ADC) at 40 MHz + header
 - 200 bits * 25 ns = 5 us/pixel
 - 128 pixels * 5 us = 640 us => ~1.5 kHz maximum rate per block of 4x32 ~10 Hz/pixel
 - Same rate for full chip with serialized 320 MHz output
 - Spec for RPs is 15 Hz/pixel (max 28 Hz)
- Future improvements
 - Payload reduction to 12b TD C + 5 samples of 8b ADC = 64 bits => ~30 Hz/pixel max rate
 - Zero-suppression : read only channels with hits and their (4-8) neighbours (for barycenters)
 - With 1 hit/column gives ~10 improvement => ~300 Hz/pixel max rate
 - A derandomizer would also be needed

EICROC1 status

- Wafers received mid december and sent to dicing company (NCAP China)
- Complex dicing as multiple chips
- Expect first chips in **february**
- Testboard fabricated : 10 boards received just before Xmas
- Now at assembly in Clermont



CdLT EICROC ePIC meeting 21 jan 2026



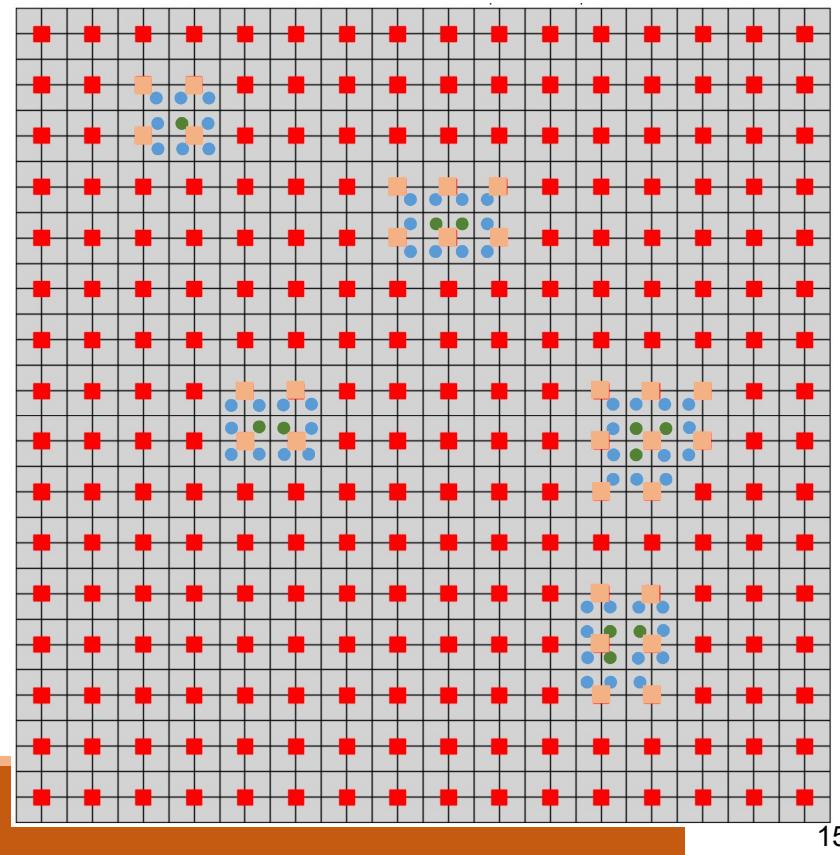
- What is missing in EICROC1 ?
 - Larger rate compatibility ?
 - Derandomizer for successive events (how many ?)
 - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
 - Auto-trigger and zero_suppressed data
 - Power reduction if possible down to ~1 mW/ch
- Clermont Ferrand lab has joined to take responsibility for the DoT
 - Already participated in ATLAS ALTIROC
 - The design and verification should take ~1 year from now
- Technology choice ?
 - Depends mostly on rate estimates and complexity of digital

- Goals
 - Less digital logic possible inside pixel/matrix
 - Less signals possible between matrix and periphery
 - Triplication of sensitive circuits (configuration registers for example)
 - No triplication on data path
 - Complexity on periphery side, simple logic inside pixel
- Proposal : **Based on clusters of 4 pixels, controlled by the periphery**
 - Some logic shared at cluster level
 - Shared data bus between 2 columns

First iteration of this architecture is ready at RTL level, some debug in progress

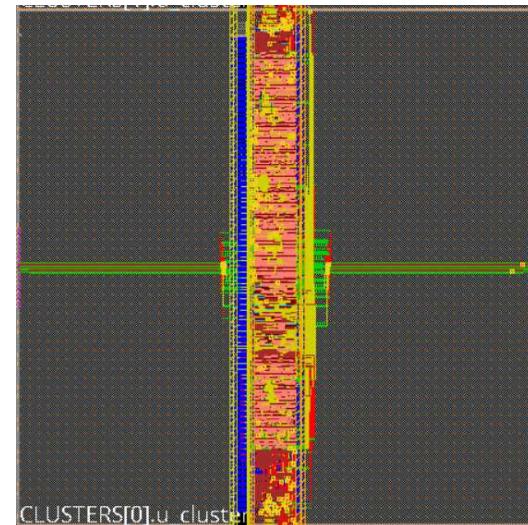
➔ Physical implementation can reveal new constraints, architecture may change

- Triggered Pixel (TP)
- Neighbor pixel (TL1)
- Busy cluster
- Cluster waiting for hit

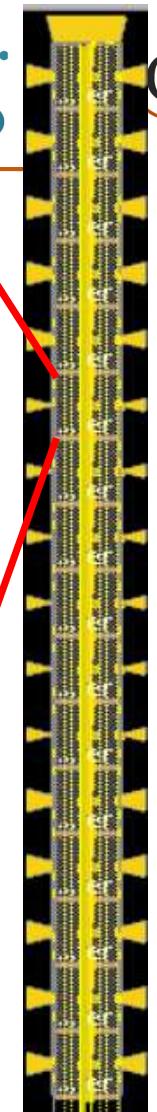


Physical implementation

- First physical implementation done in **130nm**
 - Check if we manage to fit digital readout inside pixel
- Preliminary layout of the cluster of 4 pixels and the column
- Triplication of cluster (probably need some refinement)
- Using a `pixel_analog_dummy` macro, not the real analog front-end
- **Need more time to validate that this architecture can fit using 130nm technology**



Cluster of 4 pixels



Double column

- EICROC now reached full scale 32x32 with EICROC1
 - Important for analog performance and sensor test
 - Also allows to progress on system design
- Small scale EICROCs 4x4 still under test to improve performance and reduce power
 - Foresee also version in 65n in case digital does not fit in 130n
- EICROC2 now needs its digital design : ~1 year design time from now
 - With the most welcome help from Clermont Ferrand lab
 - Main driving specification is the hit rate : 50 Hz/pixel OK ?
- System tests are (as always) an important input for chip(s) finalization

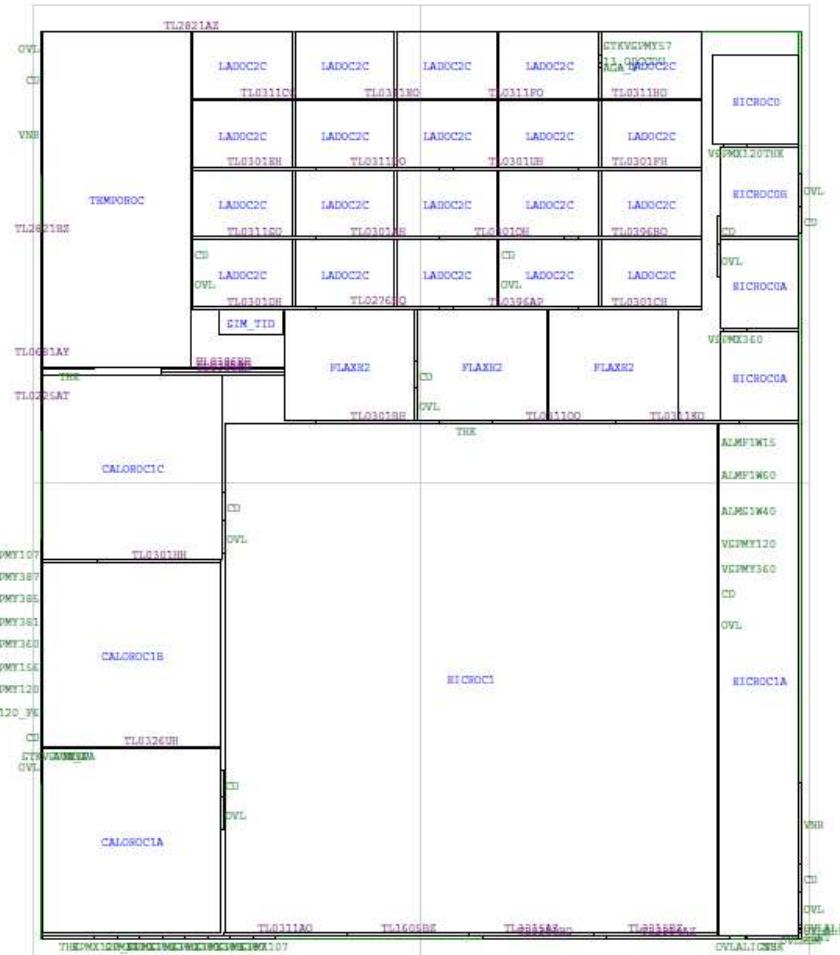
EICROC reticle 2025



- TSMC now requires to fully populate the reticle of 24x32
 - Cost ~300 k€
- For EIC we have
 - 1 EICROC1 32x32
 - 1 EICROC1A 4x32
 - 3 EICROC0/A/B 4x4
 - 3 CALOROC1A/B/C
 - ~70% of reticle area
 - EICROC1 is 40% of reticle area
 - **gds files loaded end of may**
- administrative issues delayed to september !

Layout Draft of E-ITO-TMVZ25-001

(As of 2025-08-18 16:06:04 GMT+8)

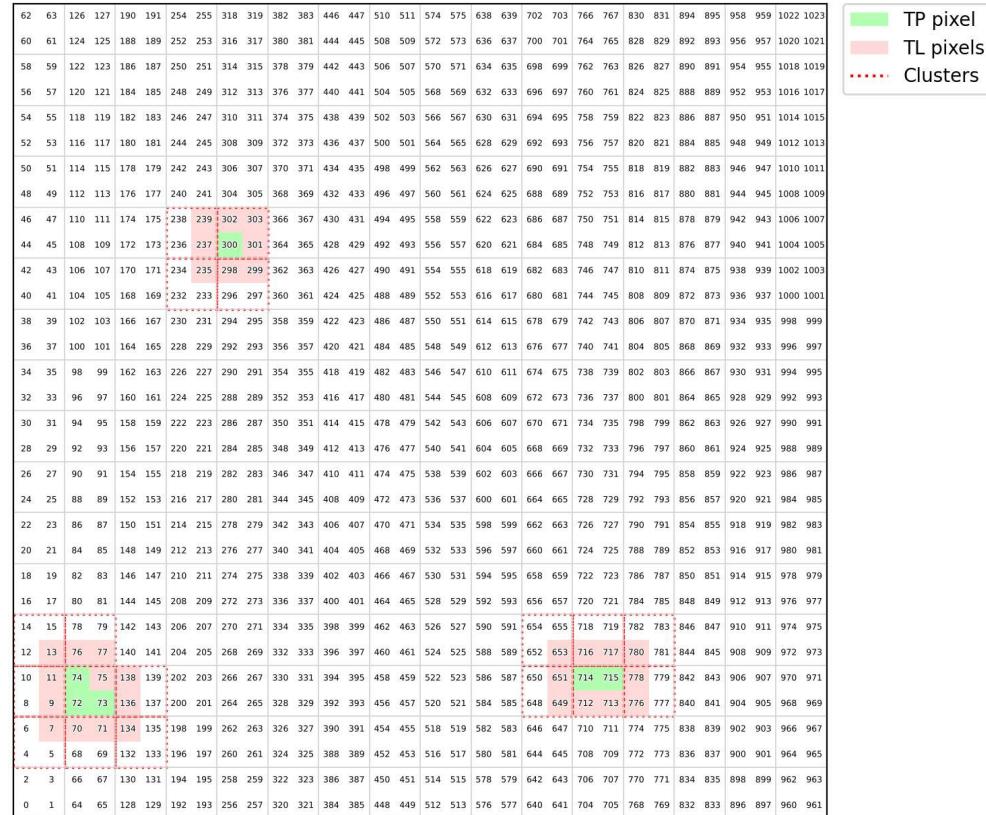


EICROC2 digital architecture

2 December 2025

Introduction

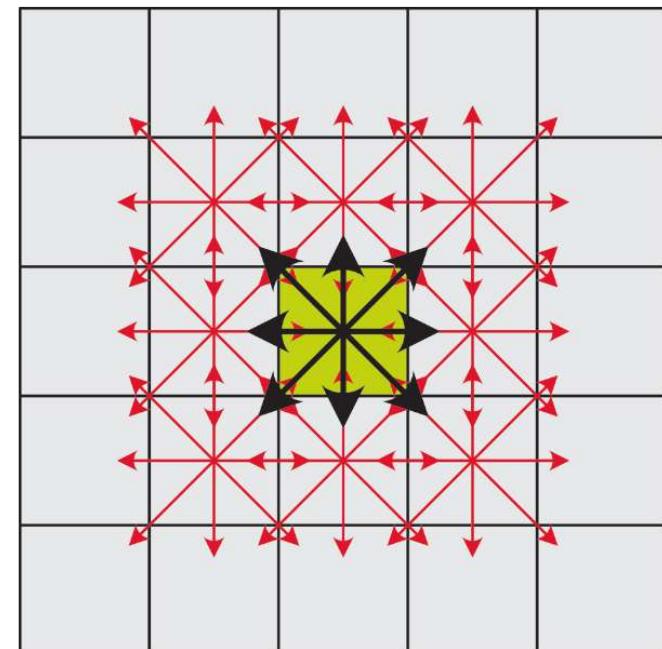
- AC LGAD sensors require to read pixel hits but also their neighbors due to charge sharing
- EICROC2 digital readout global specifications:
 - Must read neighboring pixels
 - Small area (can use 130nm techno if it is small enough)
 - Low power
 - Read fast enough to limit data loss due to dead time



62	63	126	127	190	191	254	255	318	319	382	383	446	447	510	511	574	575	638	639	702	703	766	767	830	831	894	895	958	959	1022	1023
60	61	124	125	188	189	252	253	316	317	380	381	444	445	508	509	572	573	636	637	700	701	764	765	828	829	892	893	956	957	1020	1021
58	59	122	123	186	187	250	251	314	315	378	379	442	443	506	507	570	571	634	635	698	699	762	763	826	827	890	891	954	955	1018	1019
56	57	120	121	184	185	248	249	312	313	376	377	440	441	504	505	568	569	632	633	696	697	760	761	824	825	888	889	952	953	1016	1017
54	55	118	119	182	183	246	247	310	311	374	375	438	439	502	503	566	567	630	631	694	695	758	759	822	823	886	887	950	951	1014	1015
52	53	116	117	180	181	244	245	308	309	372	373	436	437	500	501	564	565	628	629	692	693	756	757	820	821	884	885	948	949	1012	1013
50	51	114	115	178	179	242	243	306	307	370	371	434	435	498	499	562	563	626	627	690	691	754	755	818	819	882	883	946	947	1010	1011
48	49	112	113	176	177	240	241	304	305	368	369	432	433	496	497	560	561	624	625	688	689	752	753	816	817	880	881	944	945	1008	1009
46	47	110	111	174	175	238	239	302	303	366	367	430	431	494	495	558	559	622	623	688	687	750	751	814	815	878	879	942	943	1006	1007
44	45	108	109	172	173	236	237	300	301	364	365	428	429	492	493	556	557	620	621	684	685	748	749	812	813	876	877	940	941	1004	1005
42	43	106	107	170	171	234	235	298	299	362	363	426	427	490	491	554	555	618	619	682	683	746	747	810	811	874	875	938	939	1002	1003
40	41	104	105	168	169	232	233	296	297	360	361	424	425	488	489	552	553	616	617	680	681	744	745	808	809	872	873	936	937	1000	1001
38	39	102	103	166	167	230	231	294	295	358	359	422	423	486	487	550	551	614	615	678	679	742	743	806	807	870	871	934	935	998	999
36	37	100	101	164	165	228	229	292	293	356	357	420	421	484	485	548	549	612	613	676	677	740	741	804	805	868	869	932	933	996	997
34	35	98	99	162	163	226	227	290	291	354	355	418	419	482	483	546	547	610	611	674	675	738	739	802	803	866	867	930	931	994	995
32	33	96	97	160	161	224	225	288	289	352	353	416	417	480	481	544	545	608	609	672	673	736	737	800	801	864	865	928	929	992	993
30	31	94	95	158	159	222	223	286	287	350	351	414	415	478	479	542	543	606	607	670	671	734	735	799	800	862	863	926	927	990	991
28	29	92	93	156	157	220	221	284	285	348	349	412	413	476	477	540	541	604	605	668	669	732	733	796	797	860	861	924	925	998	999
26	27	90	91	154	155	218	219	282	283	346	347	410	411	474	475	538	539	602	603	666	667	730	731	794	795	858	859	922	923	996	997
24	25	88	89	152	153	216	217	280	281	344	345	408	409	472	473	536	537	600	601	664	665	728	729	792	793	856	857	920	921	984	985
22	23	86	87	150	151	214	215	278	279	342	343	406	407	470	471	534	535	598	599	662	663	726	727	790	791	854	855	918	919	982	983
20	21	84	85	148	149	212	213	276	277	340	341	404	405	468	469	532	533	596	597	660	661	724	725	788	789	852	853	916	917	980	981
18	19	82	83	146	147	210	211	274	275	338	339	402	403	466	467	530	531	594	595	658	659	722	723	788	787	850	851	914	915	978	979
16	17	80	81	144	145	208	209	272	273	336	337	400	401	464	465	528	529	592	593	656	657	720	721	784	785	848	849	912	913	976	977
14	15	78	79	142	143	206	207	270	271	334	335	398	399	462	463	526	527	590	591	654	655	718	719	782	783	846	847	910	911	974	975
12	13	76	77	140	141	204	205	268	269	332	333	396	397	460	461	524	525	588	589	652	653	716	717	786	787	844	845	908	909	972	973
10	11	74	75	138	139	202	203	266	267	330	331	394	395	458	459	522	523	586	587	650	651	714	715	778	779	842	843	906	907	970	971
8	9	72	73	136	137	200	201	264	265	328	329	392	393	456	457	520	521	584	585	646	649	712	713	776	777	840	841	904	905	968	969
6	7	70	71	134	135	198	199	262	263	326	327	390	391	454	455	518	519	582	583	646	647	710	711	774	775	838	839	902	903	966	967
4	5	68	69	132	133	196	197	260	261	324	325	388	389	452	453	516	517	580	581	644	645	708	709	772	773	836	837	900	901	964	965
2	3	66	67	130	131	194	195	258	259	322	323	386	387	450	451	515	517	578	579	642	643	706	707	770	771	834	835	898	899	962	963
0	1	64	65	128	129	192	193	256	257	320	321	384	385	444	449	512	513	576	577	640	641	704	705	766	769	832	833	896	897	960	961

Triggers for neighboring pixels

- **TP** : pixel receiving a hit = discriminator trigger, provide TDC and ADC data
- **TL1** : pixel receiving a trigger order from a TP, to read ADC data
- **TL2** : pixel receiving a trigger order from a TL1, to read ADC data
- Implementation :
 - Only TL1 is implemented for now
 - ➔ Readout only the close neighbors
- Complexity of this solution will be when routing these signals at matrix level :
Each of the 1024 pixel has one output to its 8 neighbors, and 8 inputs from them



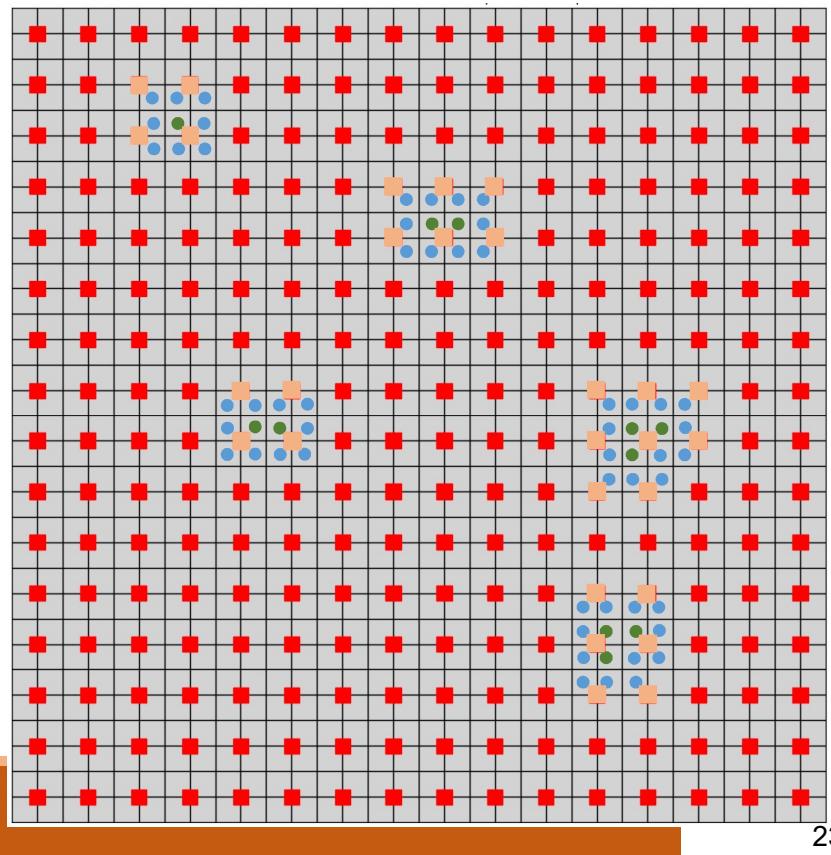
Architecture proposal

- Goals
 - Less digital logic possible inside pixel/matrix
 - Less signals possible between matrix and periphery
 - Triplication of sensitive circuits (configuration registers for example)
 - No triplication on data path
 - Complexity on periphery side, simple logic inside pixel
- Proposal : **Based on clusters of 4 pixels, controlled by the periphery**
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First iteration of this architecture is ready at RTL level, some debug in progress

➔ Physical implementation can reveal new constraints, architecture may change

- Triggered Pixel (TP)
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- Busy cluster
- Cluster waiting for hit



Dead time

What is the deadtime?



Dead time corresponds to the time a pixel is **blocked** and will not acquire new hits : pixel is **blind** during that time

- Analog dead time corresponds to the **ADC conversion time**
- Digital dead time is the time to get the **data from the pixel to the periphery**
- With the following hypothesis :
 - Event randomly distributed
 - Asynchronous system

→ Efficiency can be defined as $R = \frac{1}{\lambda\delta + 1}$

Where λ is the event rate and δ the dead time

- From Alex Jentsch : « Event rate of 100Hz for the 10% pixels closest to the beam (beam halo), 10Hz for other pixels »
 - Event rate used for analyses is 20Hz per pixel as default, and 200Hz as worst case (considering double pixels hit)
- Dead time comes from simulation results of our architecture

Dead time

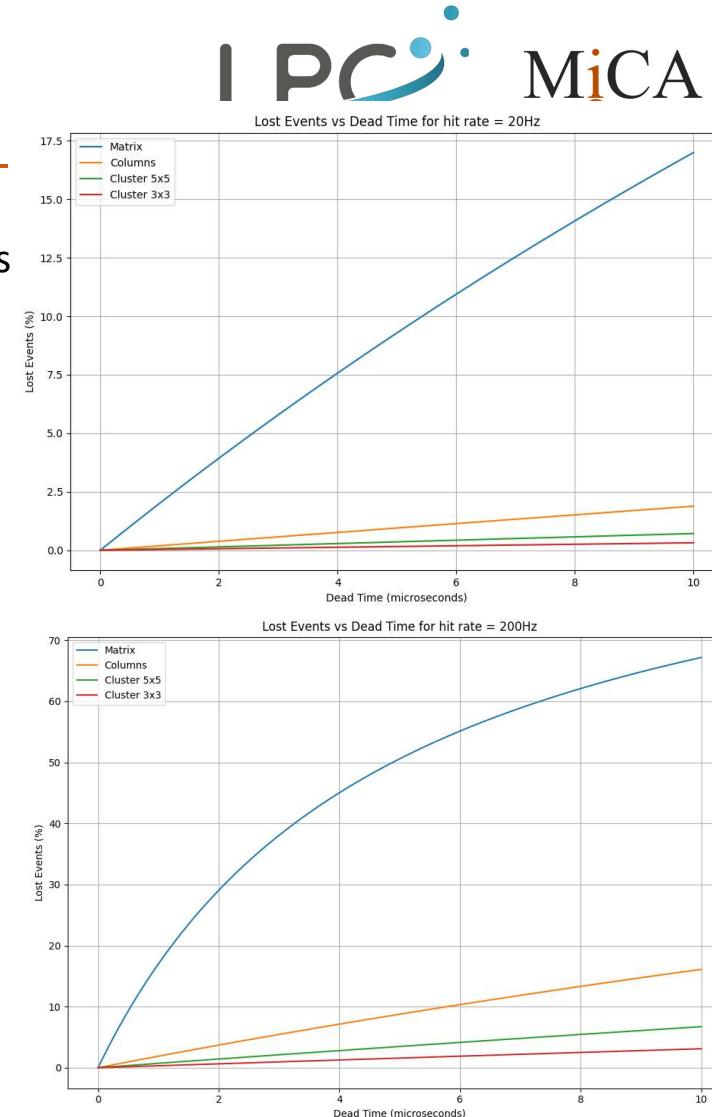
- Dead time also highly depends on the number of pixels blocked when a hit occurs
- Plots show how dead time impacts data loss for different blocking cases
- **Specifications :**
- ➔ Data loss due to dead time : **0.001% / 0.05%** (99.999 % / 99.95 % efficiency)
- **First estimation of data loss with such readout :**

Considering an average analog dead time (ADC conversion time) of 400ns

Data loss for Clusters, 3x3 readout	Rate = 20Hz	Rate = 200Hz
	Default (1 hit = 1 TP, 8 TL1)	0.028%
Multiple (1 hit = 2 TP, 10 TL1)	0.032%	0.32%
Worst case (1 hit = 4 TP, 12 TL1)	0.040%	0.40%

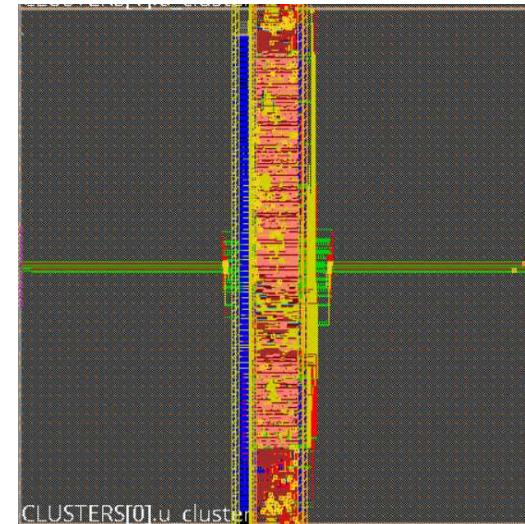
<0.05% data loss is achievable

0.001% data loss not possible for ADC with 800ns conversion time

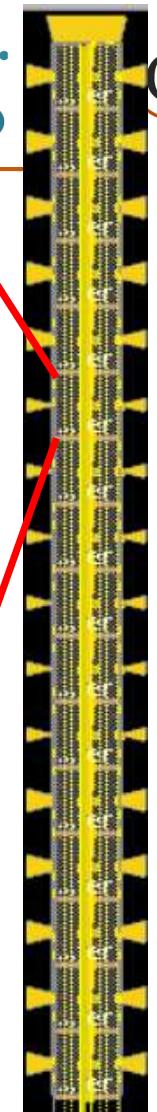


Physical implementation

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- **Need more time to validate that this architecture can fit using 130nm technology**



Cluster of 4 pixels



Double column

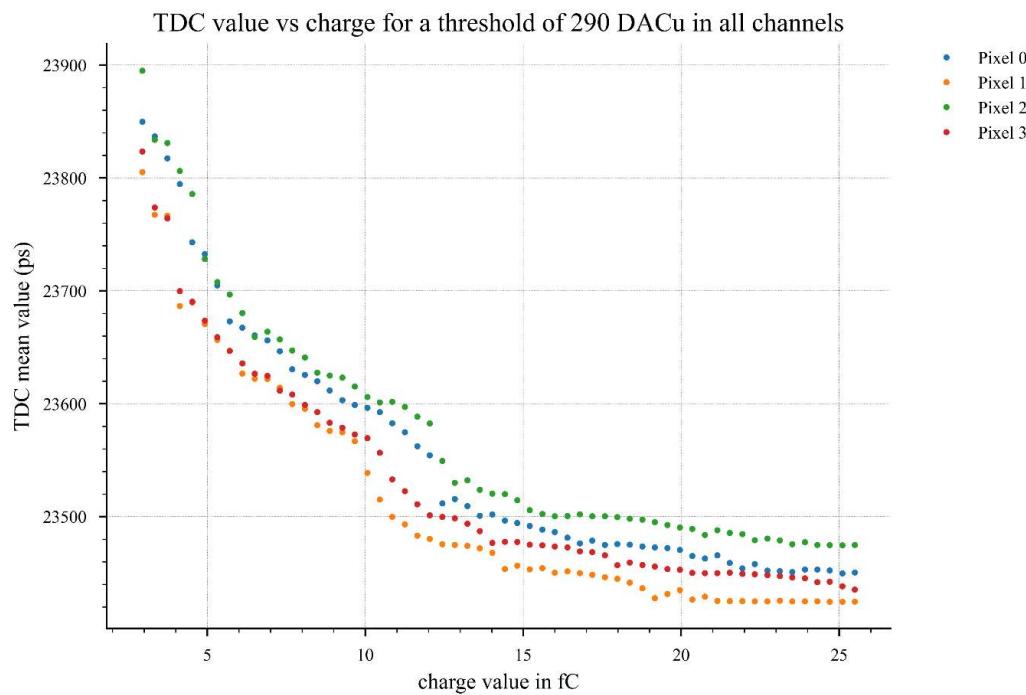
Organisation and schedule



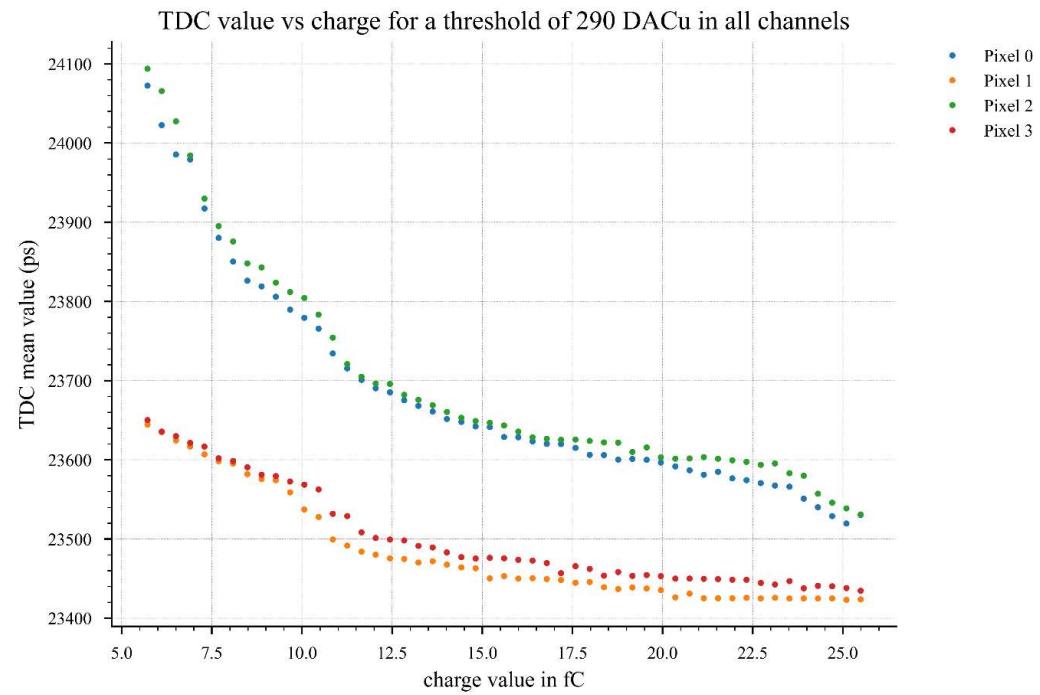
- LPCA team for EICROC :
 - 2 digital engineers (N. Kachkachi, A. Soulier)
 - 3 experts helping for specific points (H.Chanal for architecture, L.Royer for mixed-signal/system, N.Arveuf for UVM)
- Code and scripts shared on IN2P3 git
- Documentations shared on box IN2P3
 - EICROC spec : document gathering global specification related to the digital readout of the chip
 - Implementation spec : Detailed architecture explanation
- SOS server planned to be setup at Clermont : Centralized database for IP sharing
- Schedule planned:
 - First iteration of full digital RTL architecture including all blocks : Summer 2026
 - Techonology choice : Early 2026
 - First iteration of full chip implementation : Autumn 2026

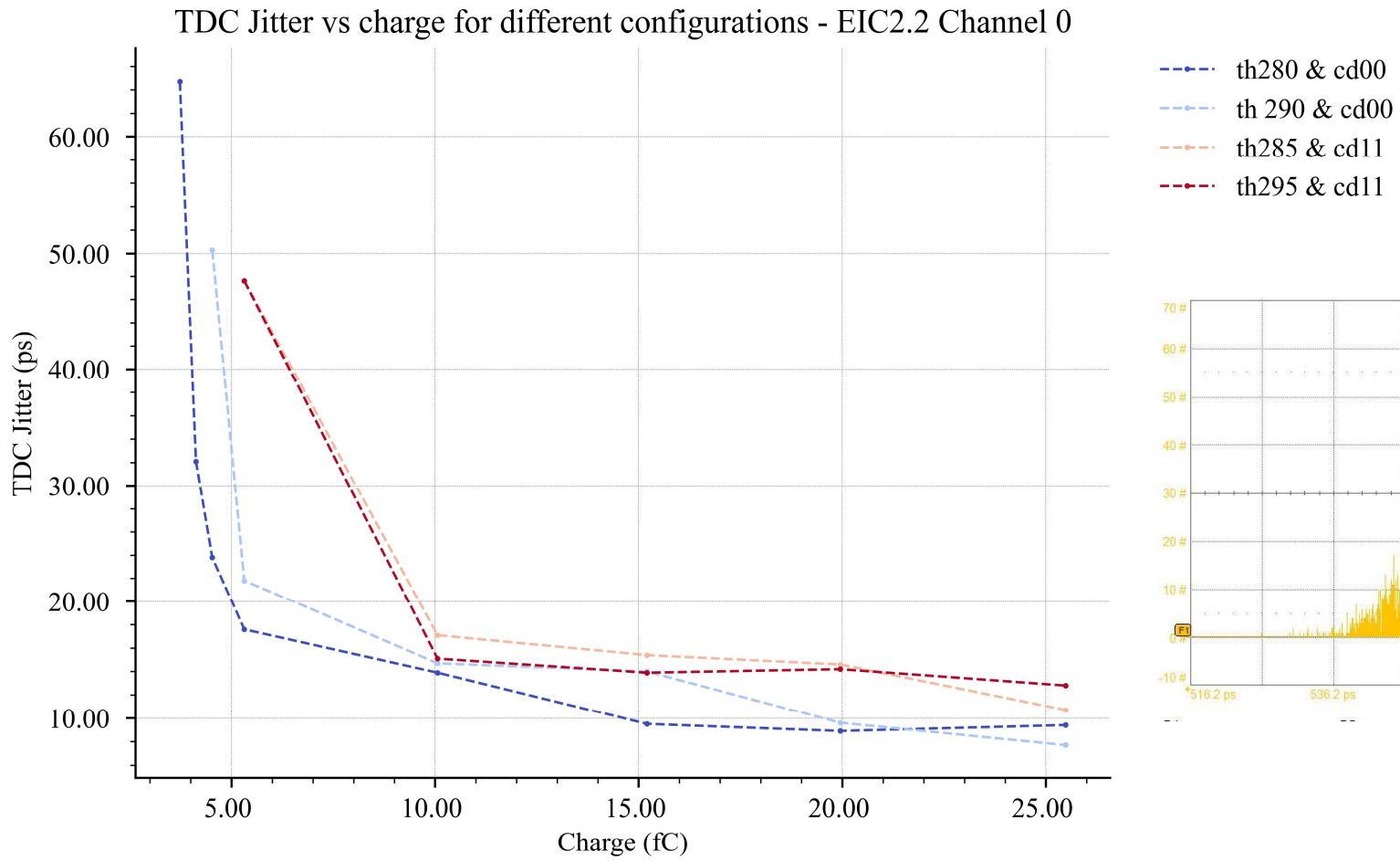
TDC ToA for $c_D = 00$ and $c_D = 11$

$c_D = 00$

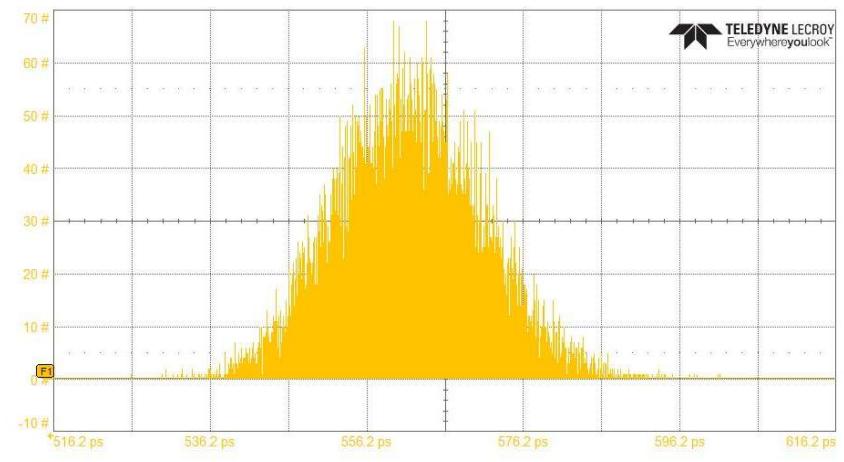


$c_D = 11$
Pixels 0 & 2





Measurements done with the oscilloscope



EICROC0 variants

- EICROC0A : same as EICROC0 with more testability
 - Each pixel can be by-passed by SC (clock is then turned off)
 - Buffers in SC to allow extension to 4x32
 - Larger dynamic range in pulse injection
- EICROC0B [Adrien]
 - Same preamp/discri/TDC/integrator
 - ADC and driver replaced by **peak sensing and Wilkinson ADC**
 - Currently ADC path ~1 mW/ch becomes 200 uW/ch
- Fabricated with EICROC1 below

