EICROC status and plans
ePIC collaboration meeting
BNL 21 jan 2026

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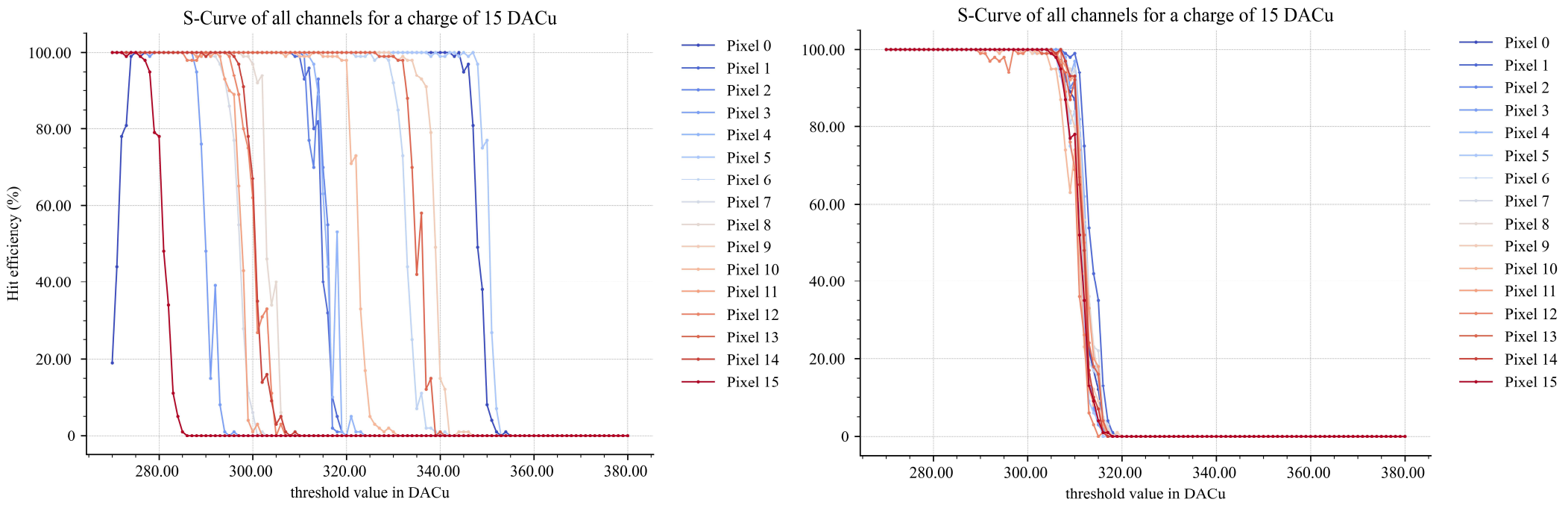
Organization for Micro-Electronics desiGn and Applications

EICROC0 update on measurements : S-Curves [A. Verplancke]

- 6-bit DAC for channel-wise threshold alignement

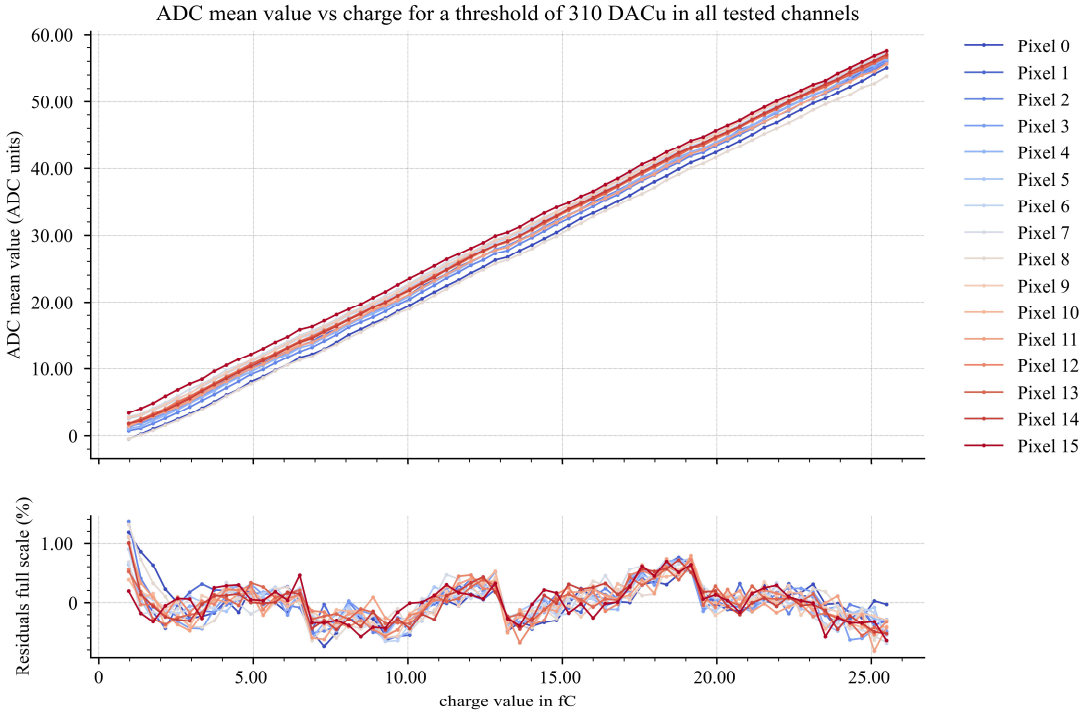
Correction of channels for a charge of 5 fC



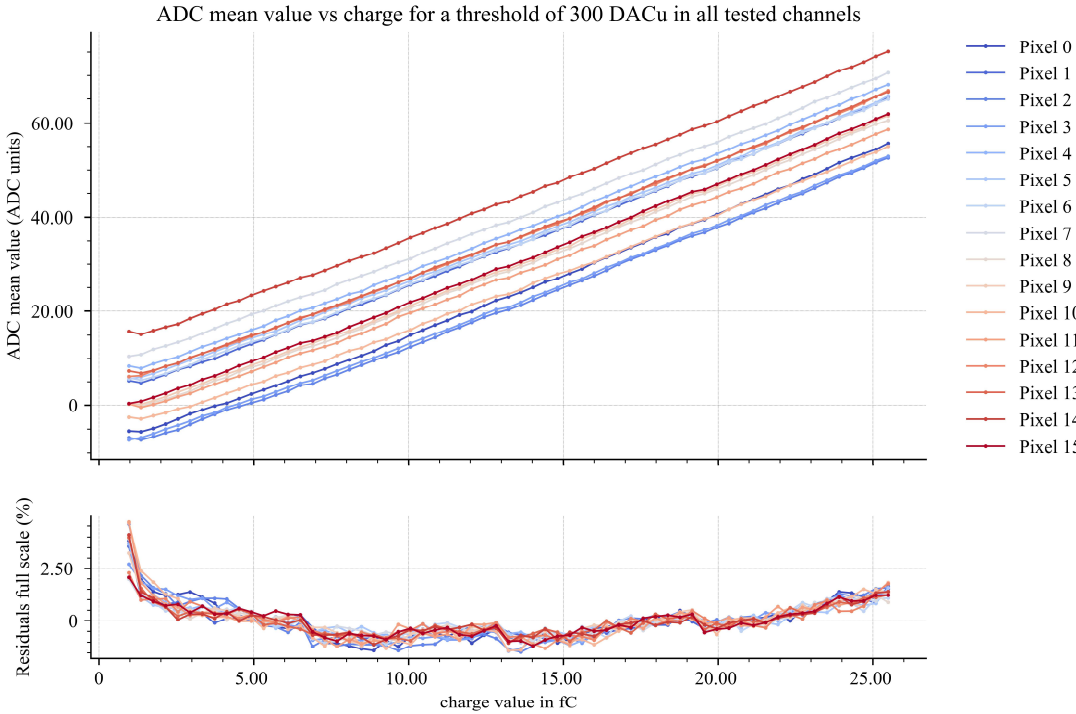
EICROC0 measurements : ADC linearity

- 8 bit 40 MHz SAR ADC [Krakow]
  - Noise ~1 UADC but large common mode noise
  - Signal 50 UADC ~500 um => 1 UADC ~10 um

ADC mean & residuals – no sensor



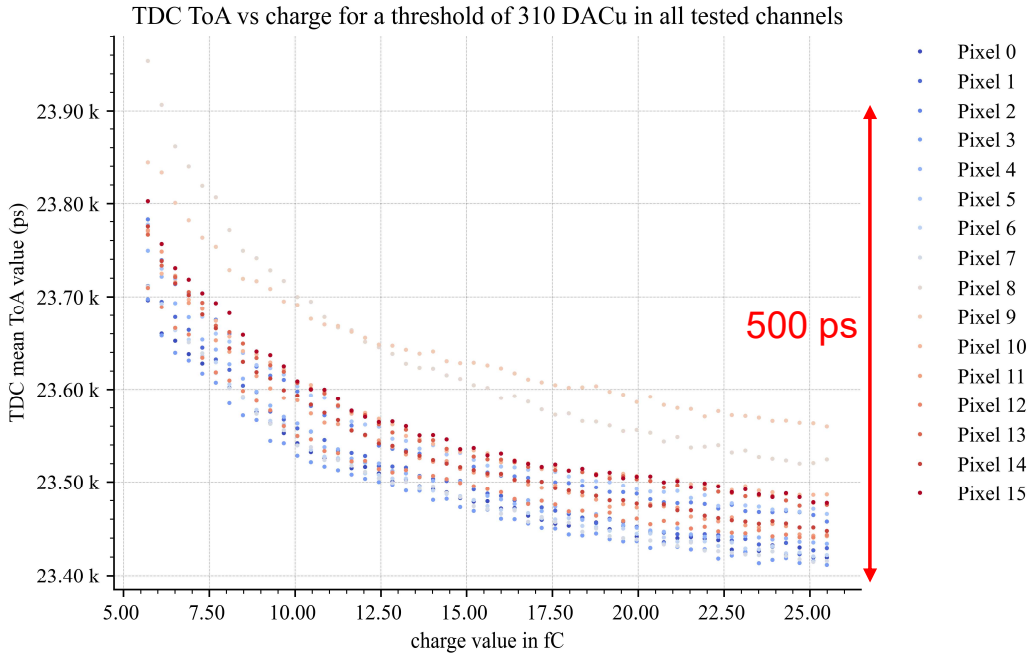
ADC mean & residuals – BNL Flipchip sensor



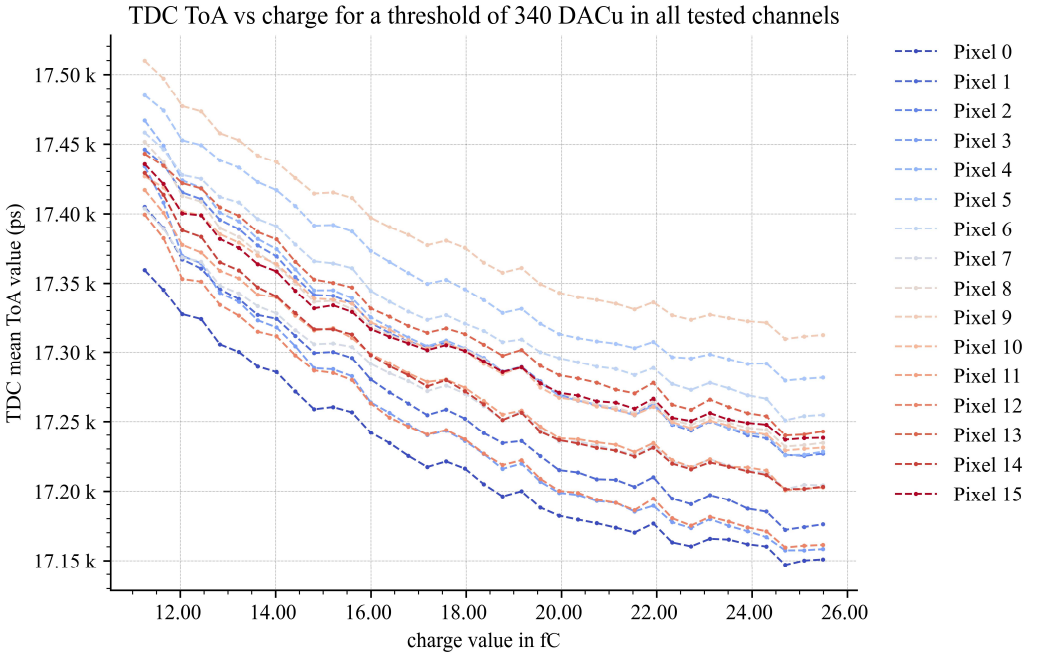
EICROC0 measurements : TDC ToA

- Time walk measurement :~400 ps

TDC ToA – no sensor

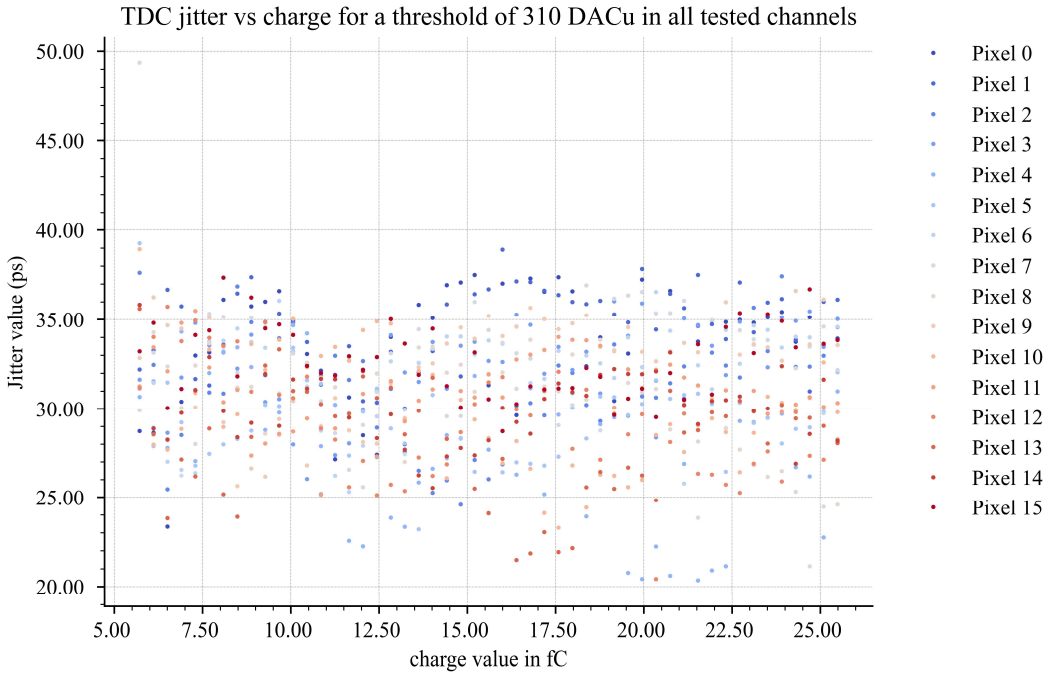


TDC ToA – BNL Flipchip sensor

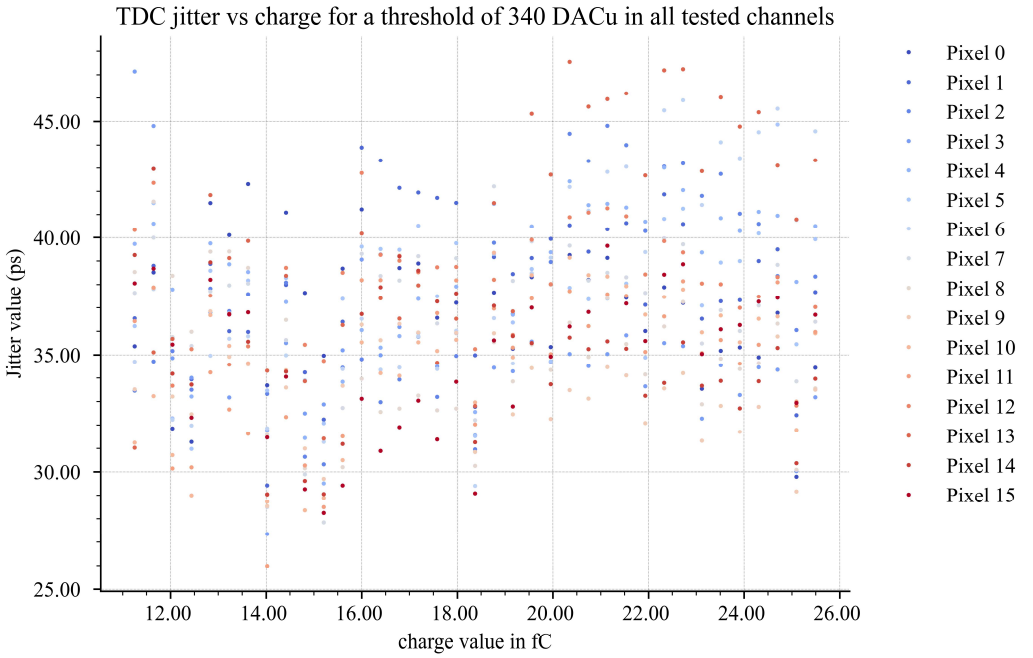


EICROC0 measurements : TDC jitter

TDC jitter – no sensor



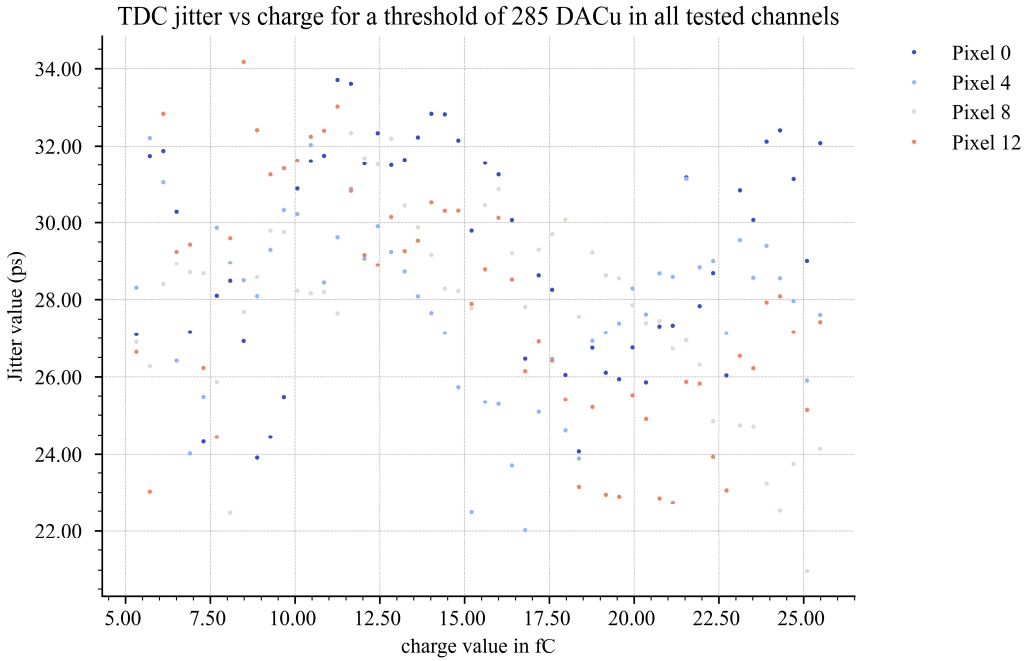
TDC jitter – BNL Flipchip sensor

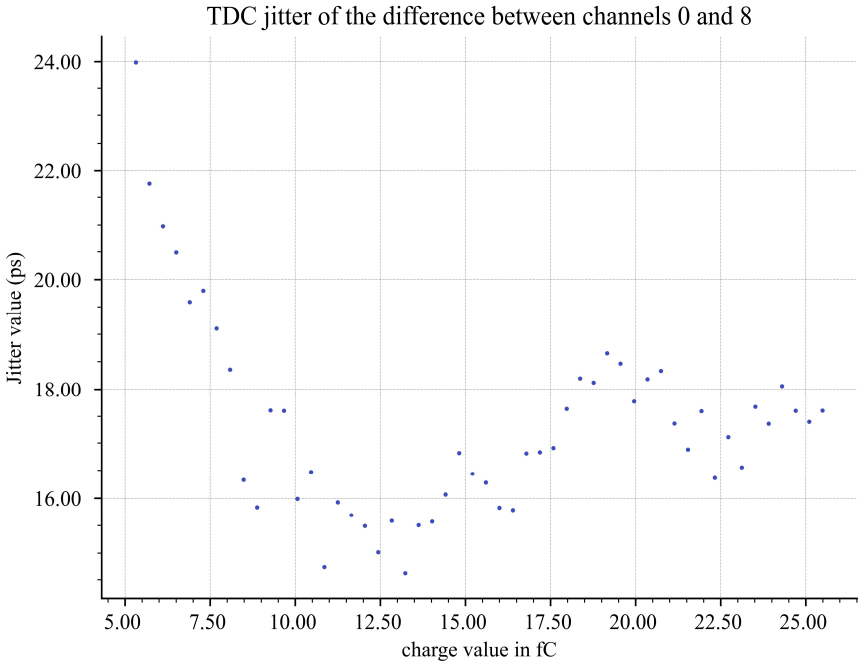


Charge range degraded with sensor, still need to properly calibrate the TDC for each channel and remove correlated noise

EICROC0 measurements : TDC jitter

TDC jitter results for a simultaneous injection in pixels of line 0 (0, 4, 8, 12)



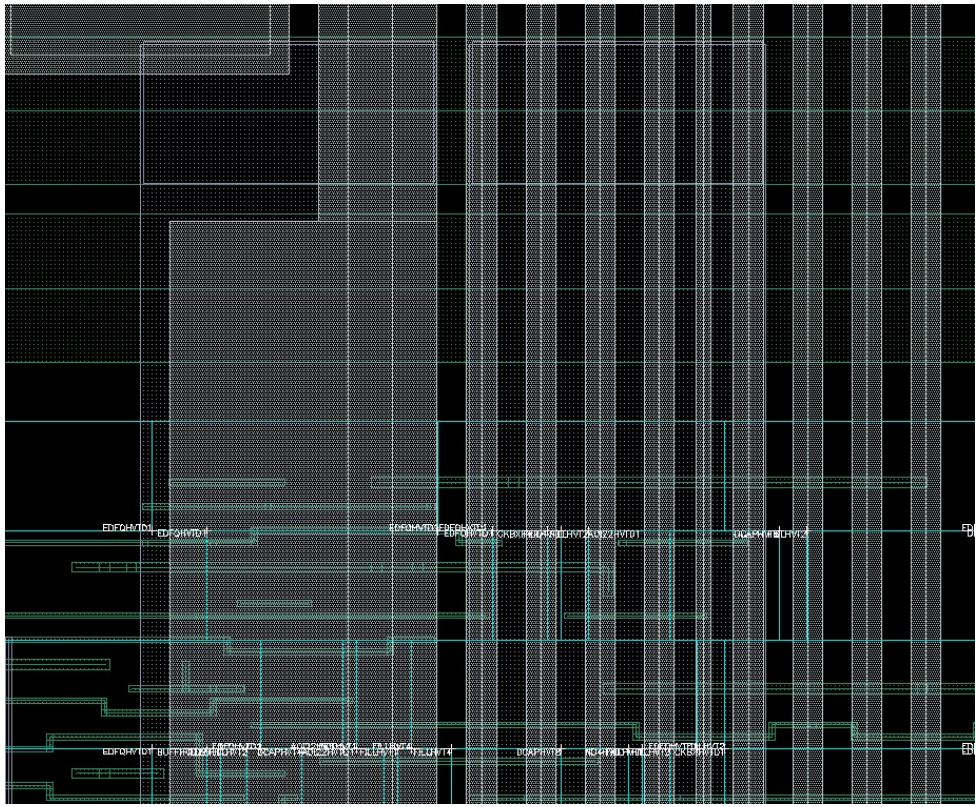


- We can also inject in channels simultaneously with the test pulse to then remove the correlated noise from the TDC measurements
- The plot represents the TDC jitter for the difference of two channels that we injected in simultaneously
- Performance approaching what is measured with the oscilloscope

EICROC0 Coupling investigation

- Large coupling seen on the ADC data which was completely hiding the signal up to 20 fC
- Large coupling capacitance between local (pixel) digital block and preamp / shaper bias lines
- Layout improved by adding exclusion zones and a shield between bias lines and digital

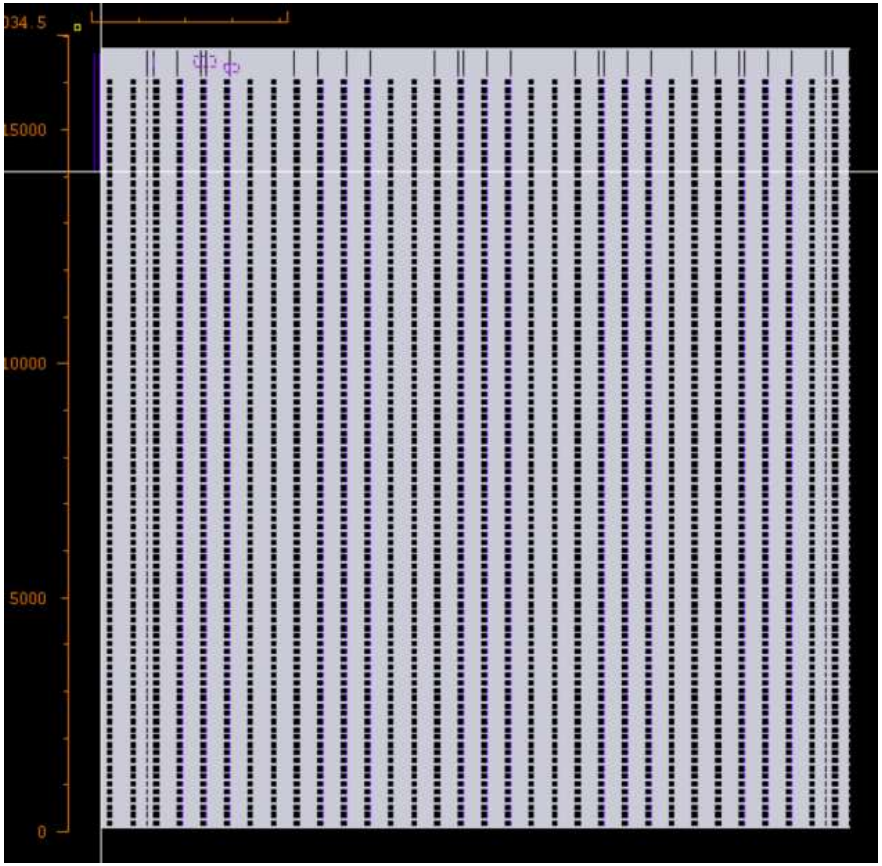
- Done in EICROC0A



Bias / digital block layout in new EICROC ASICs

EICROC1

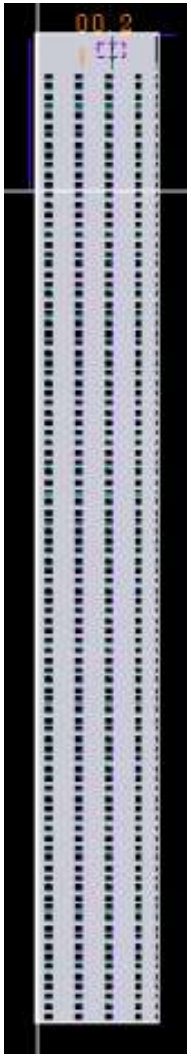
- 32x32 chip : final dimensions
- Goal :
  - test full-scale chip analog performance (IR drops)
  - Allow final sensor characterization
  - Test interface with DAQ : fast commands and 320 Mb/s data output
  - Progress on module/front-end boards
- Caveats :
  - Not (yet) zero-suppressed data
  - Still 2mW/ch
  - Still analog-on-top



EICROC1 description

- Designed as 8 blocks of 4x32
  - Read out sequentially, like EICROC0
  - Pixel similar to EICROC0A
  - 8 CLPS outputs at 40 MHz
  - Clock tree for isochronous calib_pulse distribution

- Common balcony (End of column)
  - Biases and slow control
  - New : fast command decoder (clock, calib_pulse, enable_acquisition, start_readout)
  - Backup clock and cmd_pulse inputs available
  - New : 320 MHz serializer for 1 CLPS output



EICROC1 I/Os

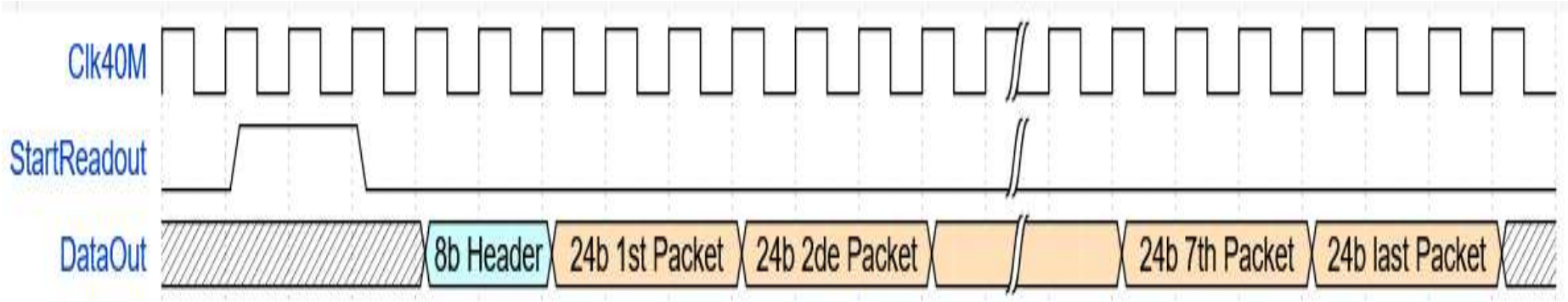
- Digital inputs
  - CLK_320 and FCMD (clock and fast commands) : CLPS
  - RSTb and RSTb_I2C : 1.2 V CMOS active low
  - SDA, SCL and 4b address : I2C slow control 1.2V CMOS
  - SEL_FCMD : 1.2V CMOS to select the backup inputs (below) (default fcmd)
  - Backup inputs : like EICROC0 (clk_160, cmd_pulse, en_acq, start_ro)
  - All unused inputs can be left floating (internal pull-ups/pull-downs)

- Digital outputs
  - 8 x 40 MHz data output (CLPS) by block of 4x32
  - one 320 MHz serialized data output (CLPS)
  - one trigger output (OR of all internal triggers) (CLPS)
  - One digital probe (1.2V CMOS) for debugging

- Analog outputs : for debugging (2 preamp outputs, analog probe, bias probe)

Data format

- Same as EICROC0 :
  - Data format : the 8 packets of 24 bits represent 8 successive samples of the data. One packet of 24 formats is ordered as followed : packet[23]=0, packet[22:12]=TDC[10:0], packet[11:9]=0, packet[8:1]=ADC[7:0], packet[0]=hit



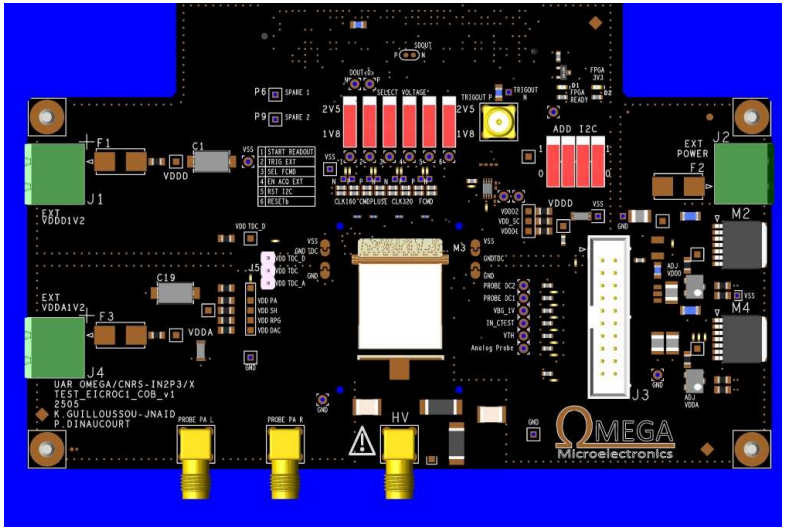
EICROC1 max rate

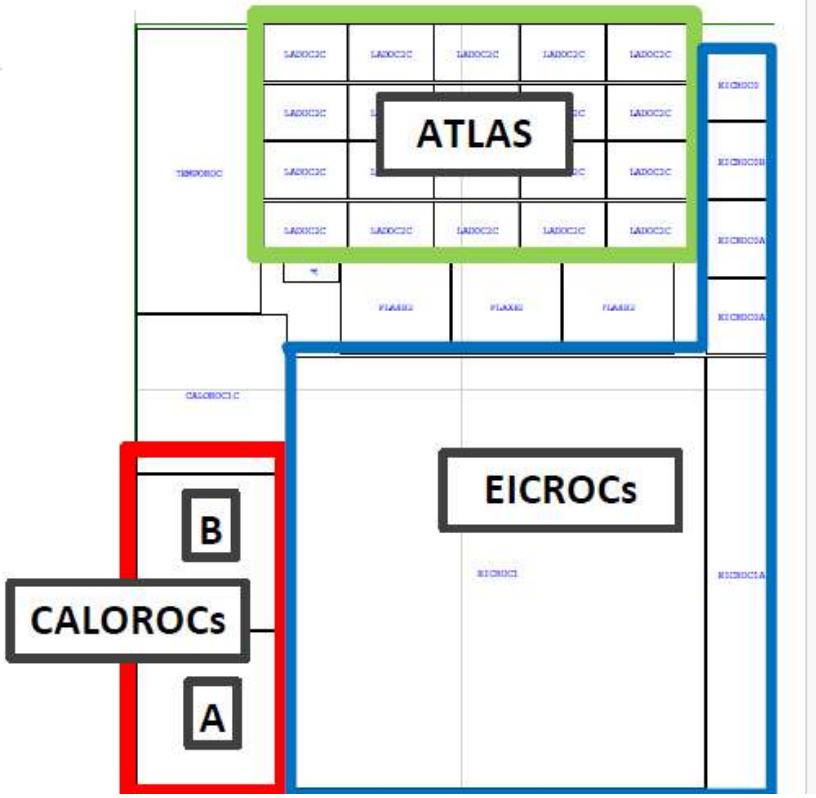
- Payload and readout speed
  - Each pixels provides 8 samples of 24 bits (12b TDC 12b ADC) at 40 MHz + header
  - 200 bits * 25 ns = 5 us/pixel
  - 128 pixels * 5 us = 640 us => ~1.5 kHz maximum rate per block of 4x32 ~10 Hz/pixel
  - Same rate for full chip with serialized 320 MHz output
  - Spec for RPs is 15 Hz/pixel (max 28 Hz)

- Future improvements
  - Payload reduction to 12b TD C + 5 samples of 8b ADC = 64 bits => ~30 Hz/pixel max rate
  - Zero-suppression : read only channels with hits and their (4-8) neighbours (for barycenters)
  - With 1 hit/column gives ~10 improvement => ~300 Hz/pixel max rate
  - A derandomizer would also be needed

EICROC1 status

- Wafers received mid december and sent to dicing company (NCAP China)
- Complex dicing as multiple chips
- Expect first chips in february
- Testboard fabricated : 10 boards received just before Xmas
- Now at assembly in Clermont





Future EICROC2

- What is missing in EICROC1 ?
  - Larger rate compatibility ?
  - Derandomizer for successive events (how many ?)
  - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
  - Auto-trigger and zero_suppressed data
  - Power reduction if possible down to ~1 mW/ch

- Clermont Ferrand lab has joined to take responsibility for the DoT
  - Already participated in ATLAS ALTIROC
  - The design and verification should take ~1 year from now

- Technology choice ?
  - Depends mostly on rate estimates and complexity of digital

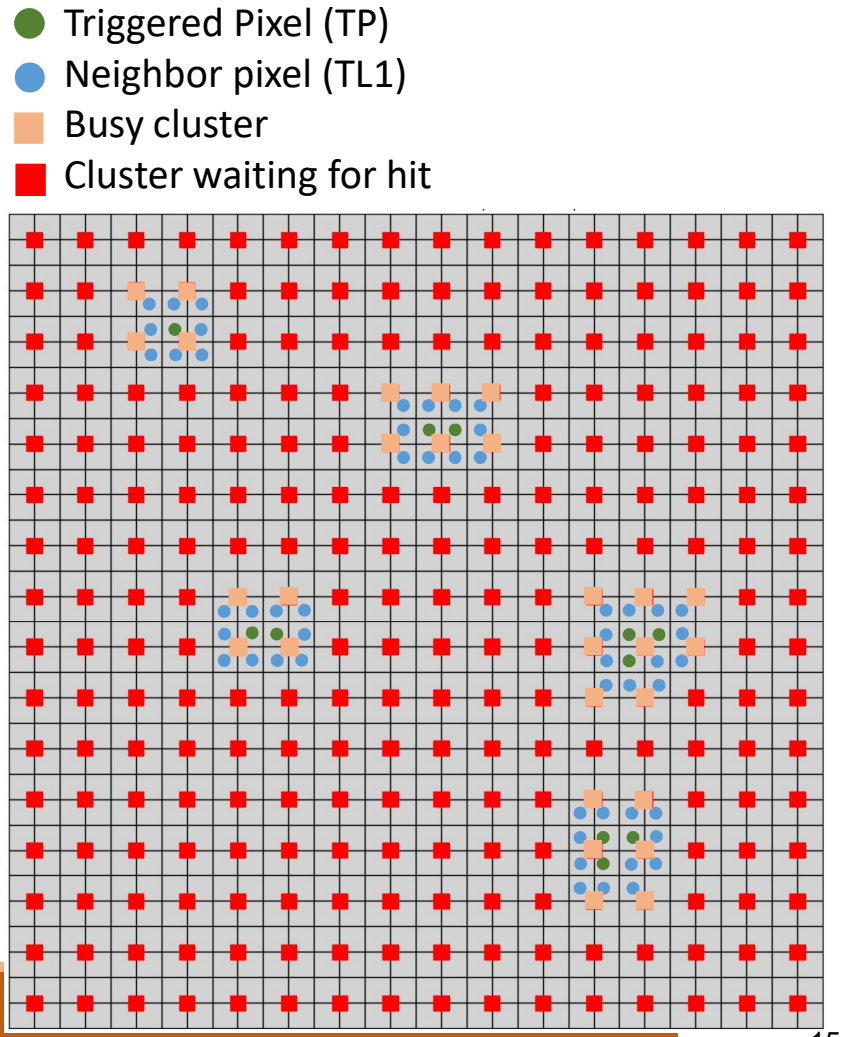
Architecture proposal [A. Soulier et al.]

- Goals
  - Less digital logic possible inside pixel/matrix
  - Less signals possible between matrix and periphery
  - Triplication of sensitive circuits (configuration registers for example)
    - No triplication on data path
  - Complexity on periphery side, simple logic inside pixel

- Proposal : **Based on clusters of 4 pixels, controlled by the periphery**
  - Some logic shared at cluster level
  - Shared data bus between 2 columns

First iteration of this architecture is ready at RTL level, some debug in progress

➔ Physical implementation can reveal new constraints, architecture may change



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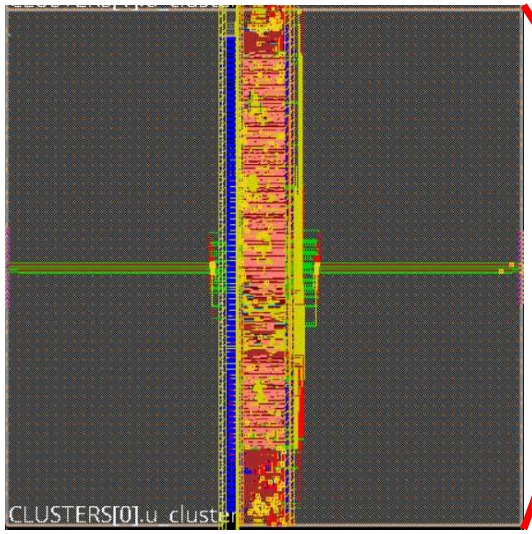
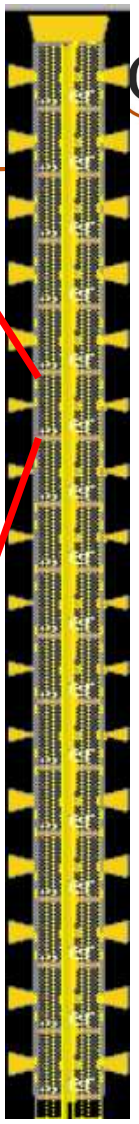
Physical implementation

- First physical implementation done in **130nm**
  - Check if we manage to fit digital readout inside pixel
- Preliminary layout of the cluster of 4 pixels and the column
- Triplication of cluster (probably need some refinement)
- Using a pixel_analog_dummy macro, not the real analog front-end
- **Need more time to validate that this architecture can fit using 130nm technology**



Cluster of 4 pixels



Double column

summary

- EICROC now reached full scale 32x32 with EICROC1
  - Important for analog performance and sensor test
  - Also allows to progress on system design

- Small scale EICROCs 4x4 still under test to improve performance and reduce power
  - Foresee also version in 65n in case digital does not fit in 130n

- EICROC2 now needs its digital design : ~1 year design time from now
  - With the most welcome help from Clermont Ferrand lab
  - Main driving specification is the hit rate : 50 Hz/pixel OK ?

- System tests are (as always) an important input for chip(s) finalization

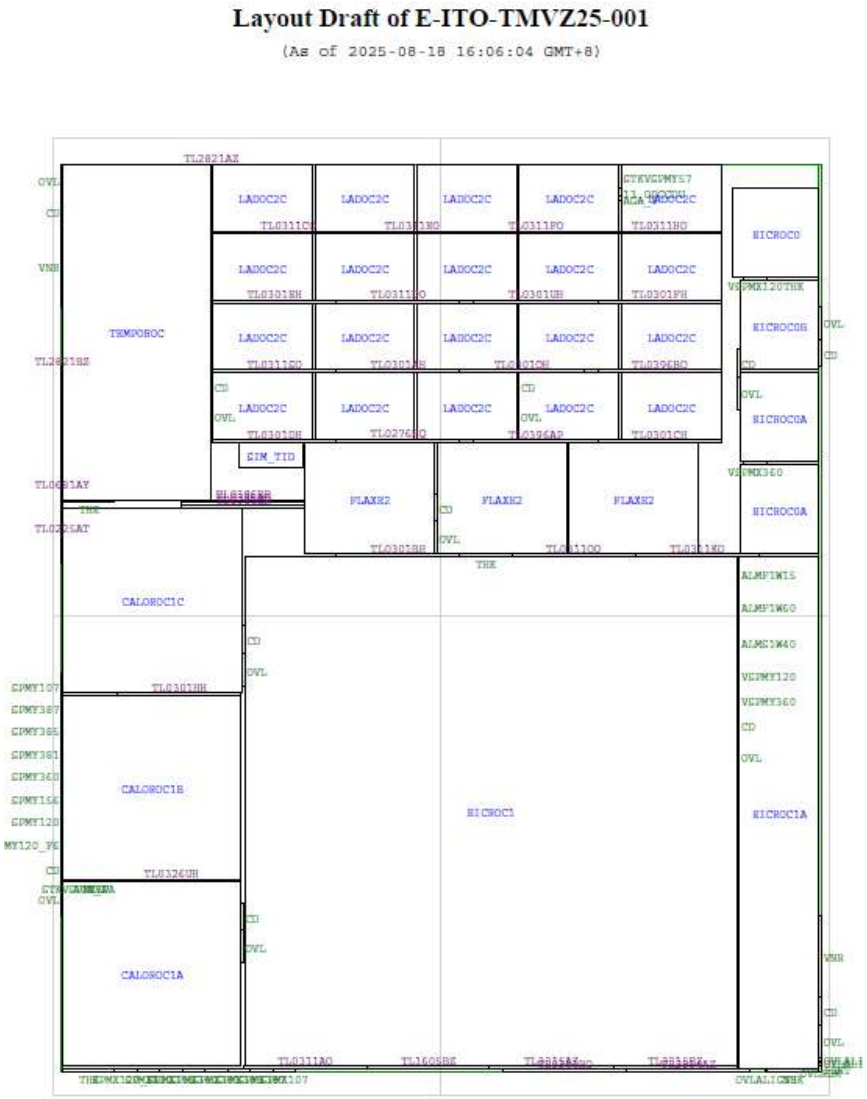
backup

EICROC reticle 2025

- TSMC now requires to fully populate the reticle of 24x32
  - Cost ~300 k€

- For EIC we have
  - 1 EICROC1 32x32
  - 1 EICROC1A 4x32
  - 3 EICROC0/A/B 4x4
  - 3 CALOROC1A/B/C
  - ~70% of reticle area
  - EICROC1 is 40% of reticle area
  - gds files loaded end of may

- administrative issues delayed run to september !

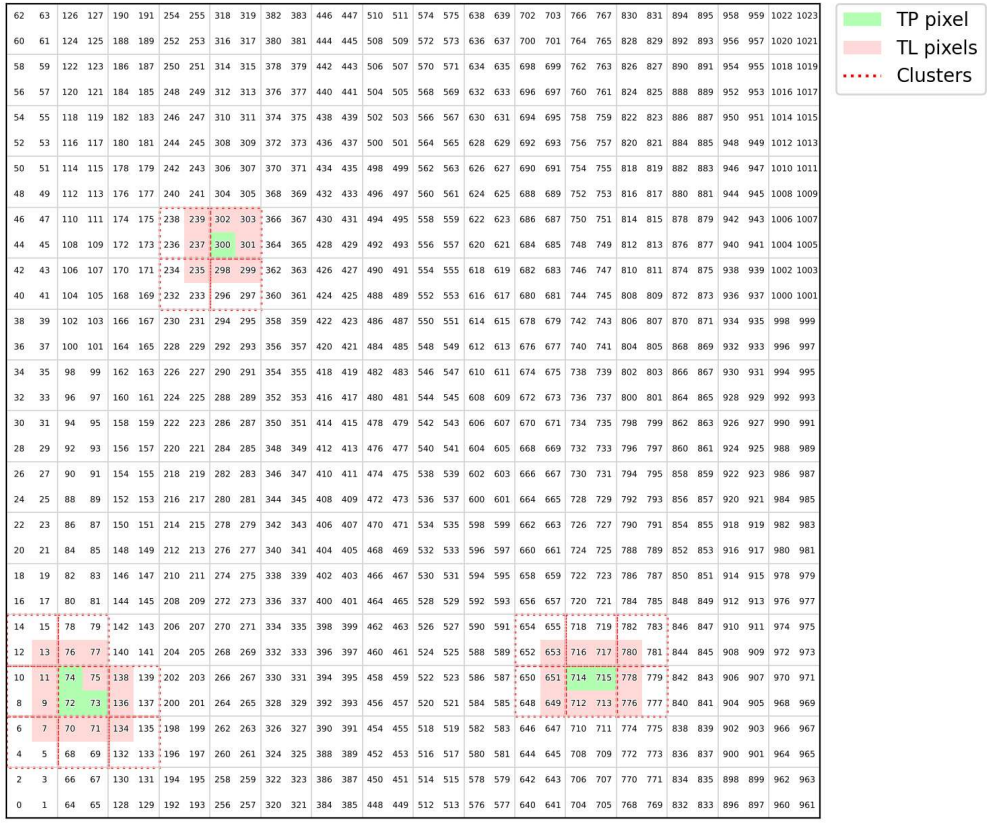


EICROC2 digital architecture

2 December 2025

Introduction

- AC LGAD sensors require to read pixel hits but also their neighbors due to charge sharing



- EICROC2 digital readout global specifications:
  - Must read neighboring pixels
  - Small area (can use 130nm techno if it is small enough)
  - Low power
  - Read fast enough to limit data loss due to dead time

Triggers for neighboring pixels

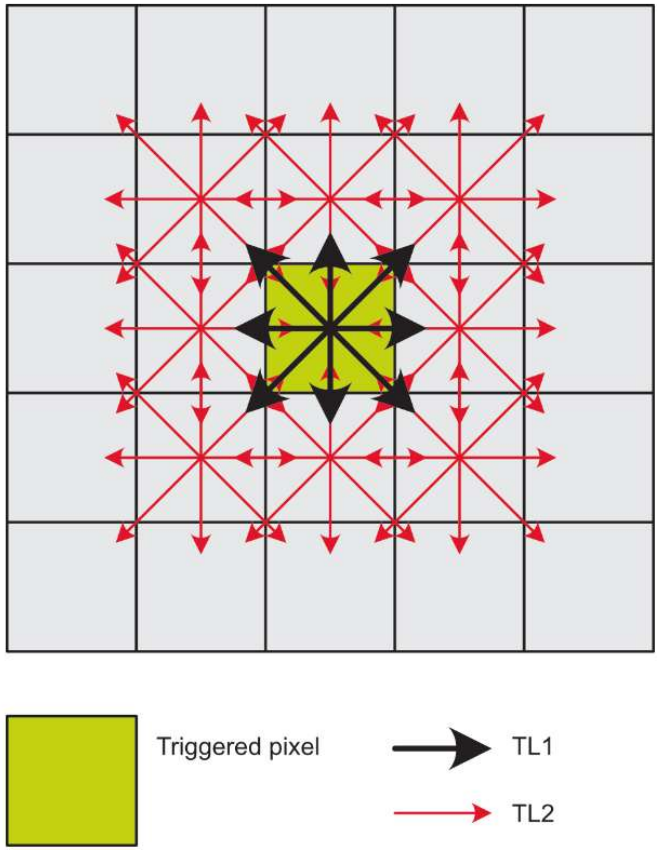
- **TP** : pixel receiving a hit = discriminator trigger, provide TDC and ADC data
- **TL1** : pixel receiving a trigger order from a TP, to read ADC data
- TL2 : pixel receiving a trigger order from a TL1, to read ADC data

- Implementation :
  - Only TL1 is implemented for now

  ➔ Readout only the close neighbors

- Complexity of this solution will be when routing these signals at matrix level :

Each of the 1024 pixel has one output to its 8 neighbors, and 8 inputs from them



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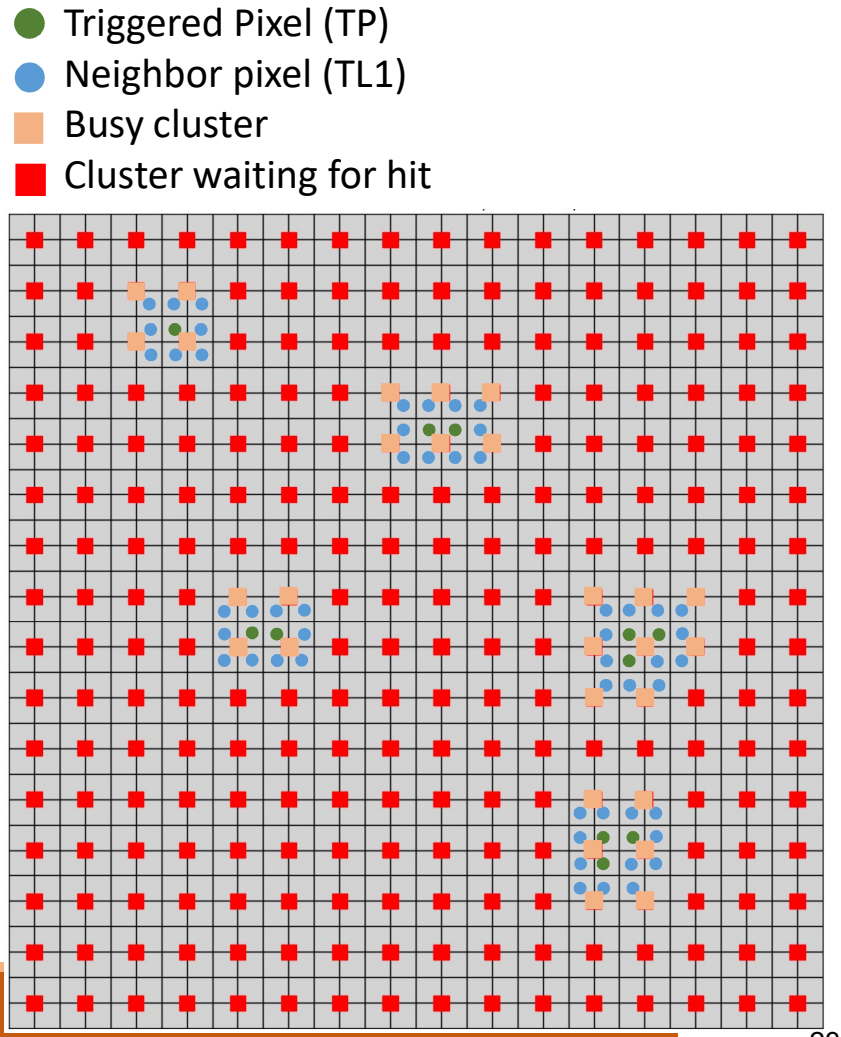

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Dead time

What is the deadtime?

Dead time corresponds to the time a pixel is **blocked** and will not acquire new hits : pixel is **blind** during that time

- Analog dead time corresponds to the **ADC conversion time**
- Digital dead time is the time to get the **data from the pixel to the periphery**

- With the following hypothesis :
  - Event randomly distributed
  - Asynchronous system
  - ➔ Efficiency can be defined as $R = \frac{1}{\lambda\delta + 1}$

  Where λ is the event rate and δ the dead time

- From Alex Jentsch : « Event rate of 100Hz for the 10% pixels closest to the beam (beam halo), 10Hz for other pixels »
  - Event rate used for analyses is 20Hz per pixel as default, and 200Hz as worst case (considering double pixels hit)
- Dead time comes from simulation results of our architecture

Dead time

- Dead time also highly depends on the number of pixels blocked when a hit occurs
- Plots show how dead time impacts data loss for different blocking cases
- **Specifications** :

➔ Data loss due to dead time : **0.001% / 0.05%** (99.999 % / 99.95 % efficiency)

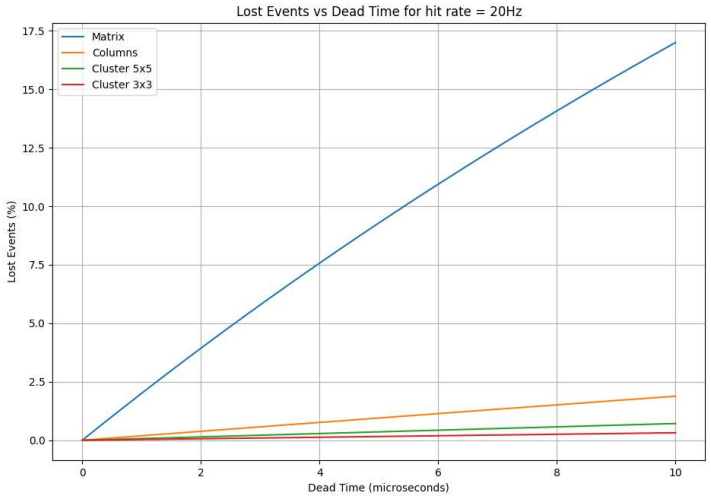
- **First estimation of data loss with such readout :**

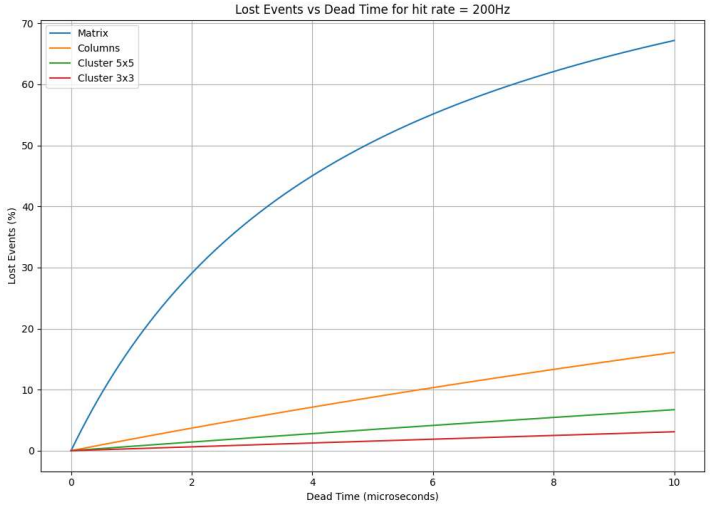
Considering an average analog dead time (ADC converstion time) of 400ns

Data loss for Clusters, 3x3 readout	Rate = 20Hz	Rate = 200Hz
Default (1 hit = 1 TP, 8 TL1)	0.028%	0.28%
Multiple (1 hit = 2 TP, 10 TL1)	0.032%	0.32%
Worst case (1 hit = 4 TP, 12 TL1)	0.040%	0.40%

<0.05% data loss is achievable

0.001% data loss not possible for ADC with 800ns conversion time





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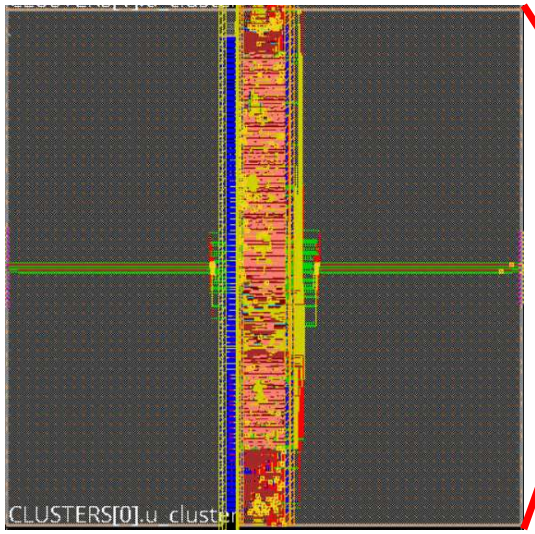
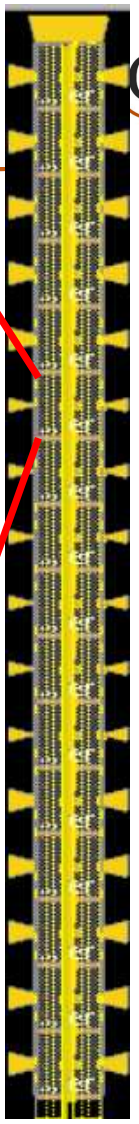


Cluster of 4 pixels



Double column

Organisation and schedule

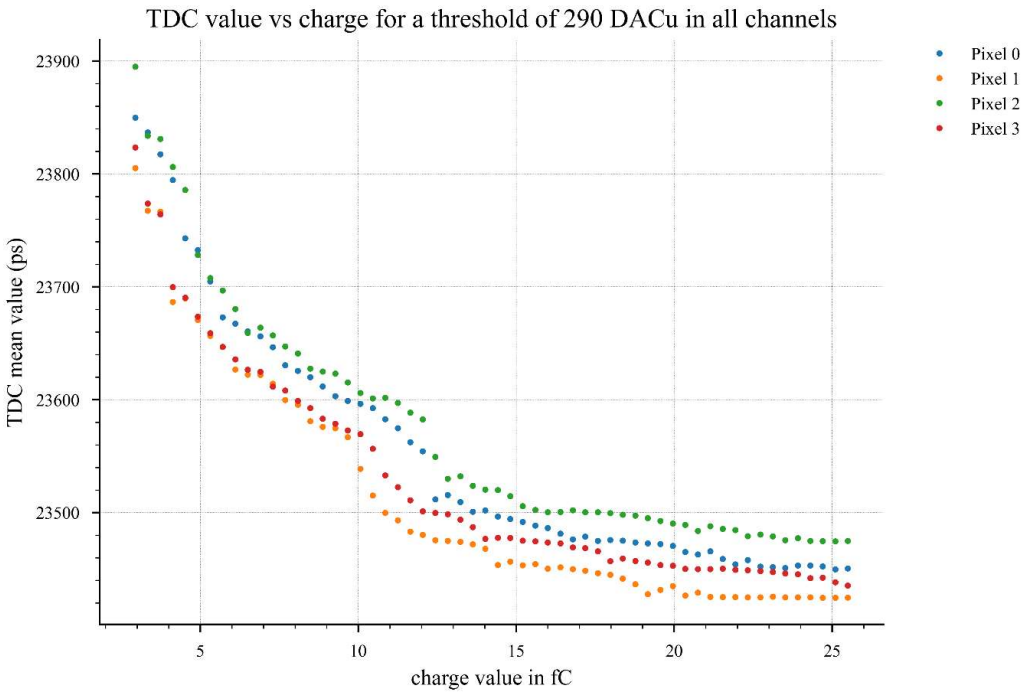
- LPCA team for EICROC :
  - 2 digital engineers (N. Kachkachi, A. Soulier)
  - 3 experts helping for specific points (H.Chanal for architecture, L.Royer for mixed-signal/system, N.Arveuf for UVM)
- Code and scripts shared on IN2P3 git
- Documentations shared on box IN2P3
  - EICROC spec : document gathering global specification related to the digital readout of the chip
  - Implementation spec : Detailed architecture explanation
- SOS server planned to be setup at Clermont : Centralized database for IP sharing

- Schedule planned:
  - First iteration of full digital RTL architecture including all blocks : Summer 2026
  - Techonology choice : Early 2026
  - First iteration of full chip implementation : Autumn 2026

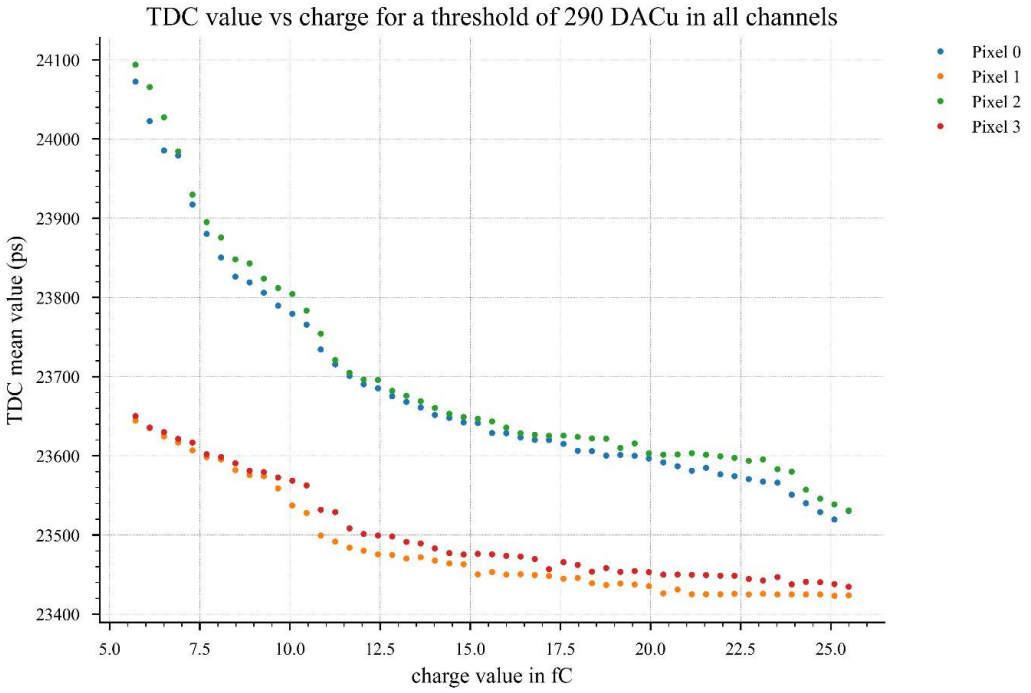
EICROC0 measurements : TDC ToA with no sensor

TDC ToA for c_D = 00 and c_D = 11

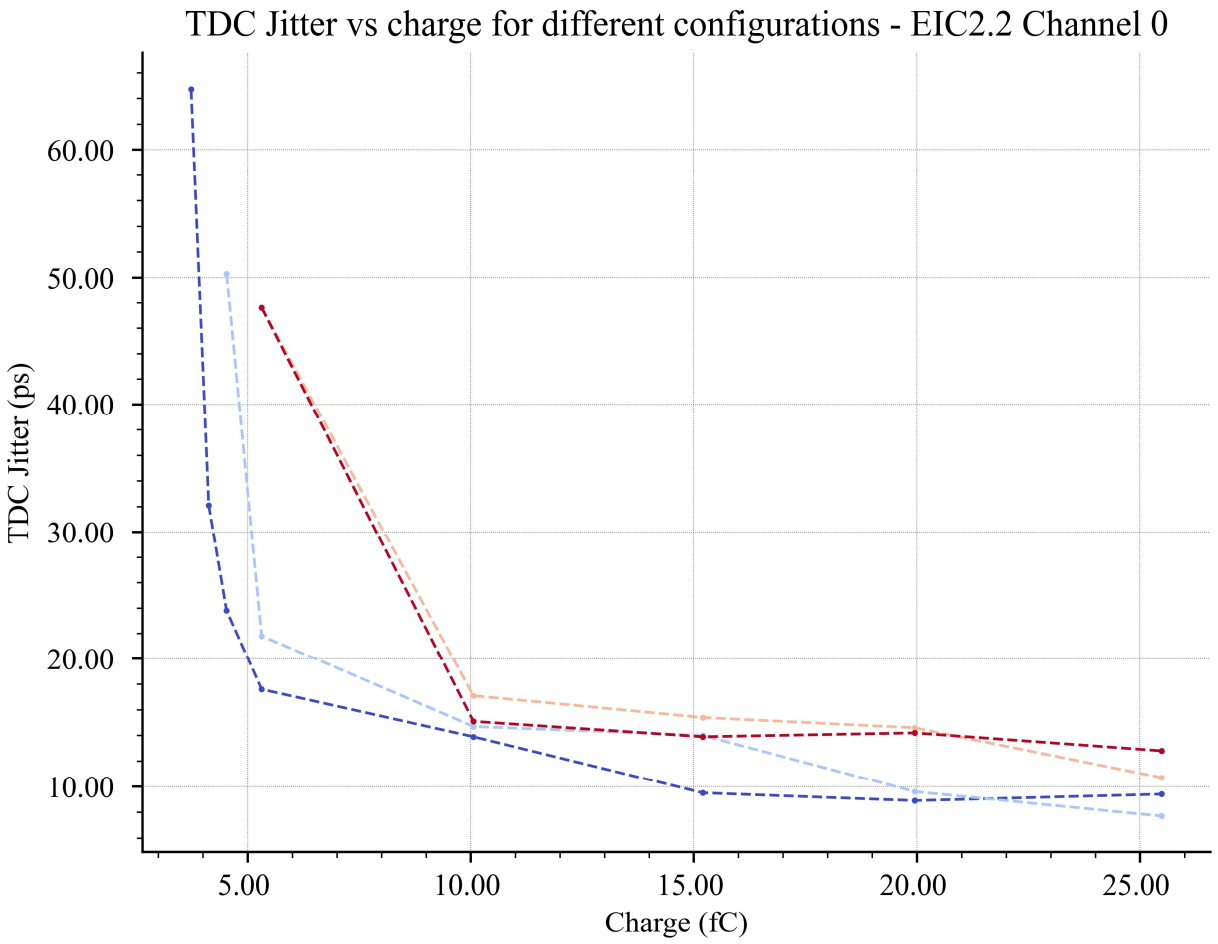
c_D = 00



C_D = 11
Pixels 0 & 2

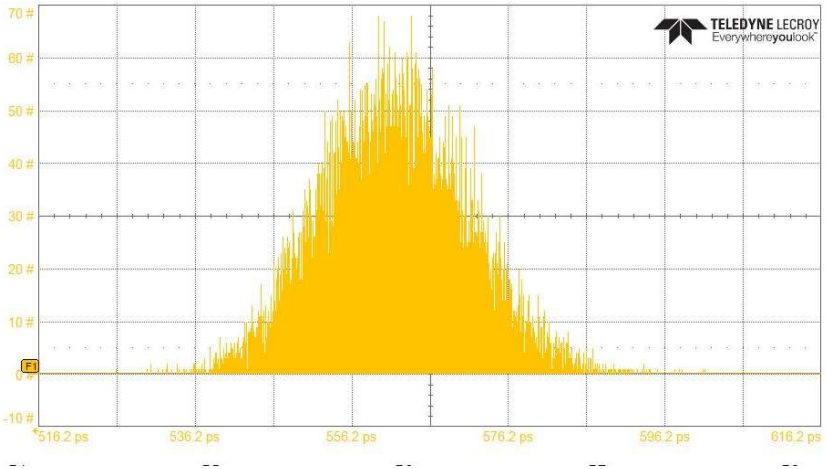


EICROC0 : discriminator jitter measured on probe



th280 & cd00
th 290 & cd00
th285 & cd11
th295 & cd11

Measurements done with the oscilloscope



EICROC0 variants

- EICROC0A : same as EICROC0 with more testability
  - Each pixel can be by-passed by SC (clock is then turned off)
  - Buffers in SC to allow extension to 4x32
  - Larger dynamic range in pulse injection

- EICROC0B [Adrien]
  - Same preamp/discri/TDC/integrator
  - ADC and driver replaced by peak sensing and Wilkinson ADC
  - Currently ADC path ~1 mW/ch becomes 200 uW/ch

- Fabricated with EICROC1 below