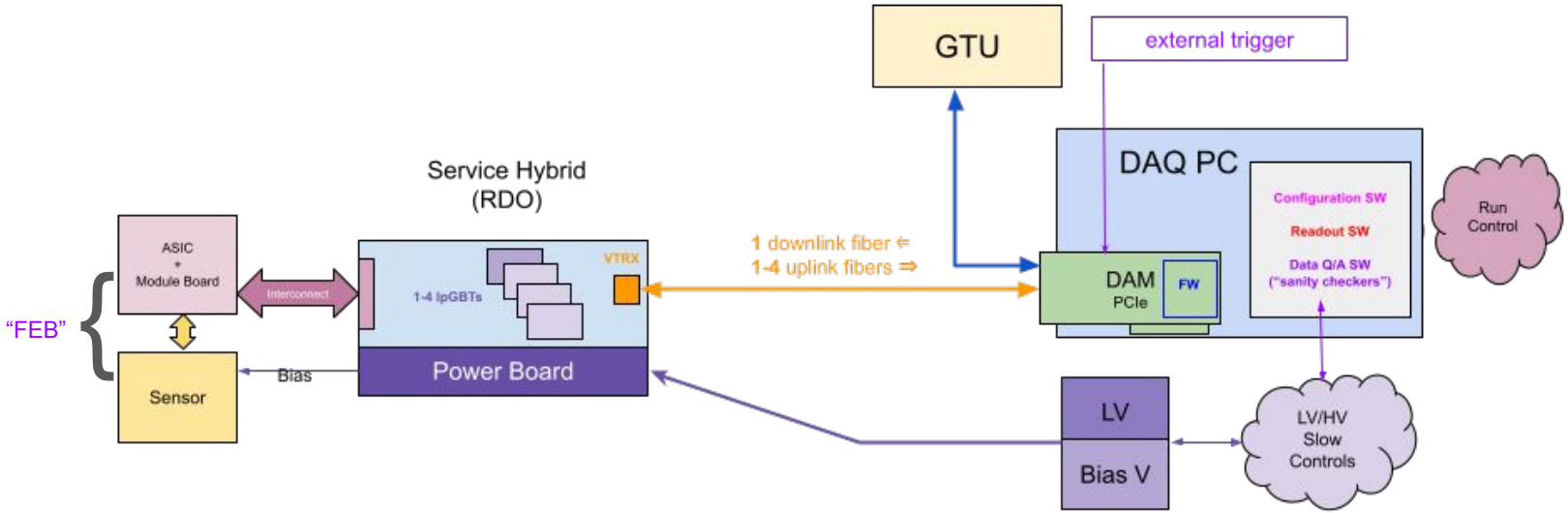
AC-LGAD Readout Chain Updates

T. Ljubicic, M. Matveev, W. Li (Rice University)
A. Jentsch, P. Tribedy, T. Camarda (BNL)

What is the AC-LGAD Readout Chain

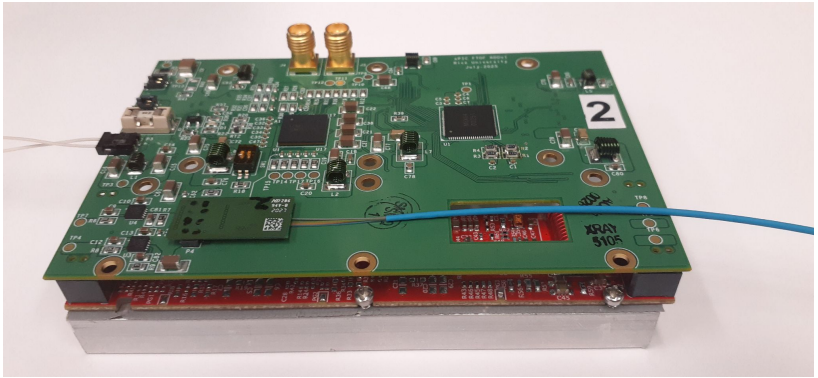


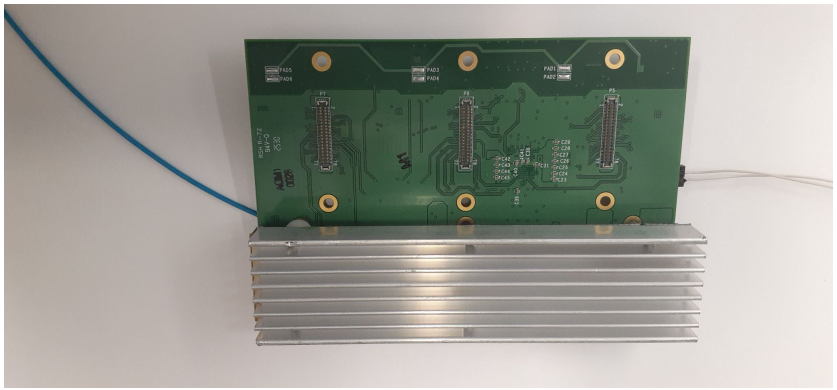
Components of the Readout Chain

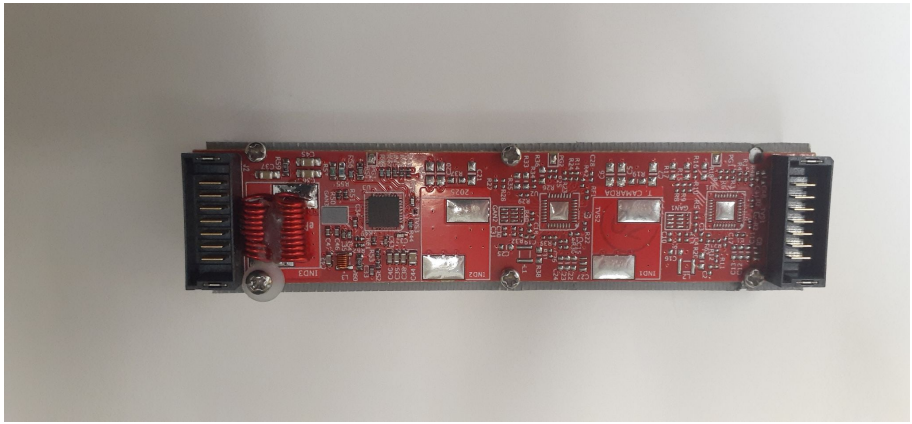
- AC-LGAD Readout Board RBv1 (Completed)
  - lpGBT & VTRX+ based
  - can interface to up to 12 ASICs
- Forward TOF Power Board PBv1 (Completed)
  - CERN bPOL48 as the main converter
  - designed for EICROC1 and FTOF but serves as a V0 prototype for other AC-LGAD detectors
- Full Streaming Readout Chain over PCIe into DAQ using the Alinx AXAU15 DAM (Completed)
  - equipped with an external trigger input, if required (completed)
  - can be used by any lpGBT-based detector
- Adapter cards to ASIC Testboards (in progress)
  - EICROC1 Testboard designed at OMEGA as well as its Adapter Board from Rice
    - due Feb/Mar
  - FCFD Testboard & Adapter Board under discussion with Fermilab
    - planned for ~Summer 2026

RBv1 and PBv1 Board

- we have these boards at Rice and at BNL







⇐ PBv1 is 103 x 22 mm

Cooling fins above act as the detector's "Cooling Manifold" (slide 2)

EICROC1 Readout Tests

- We have 2 full Readout Chains:
  - at Rice: assembled and tested
  - at BNL: assembled (just now!) and will be tested ~next week
    - BTW, we need to meet to see if the lab location is suitable for longer term (1 year)
- EICROC1 Testboard designed by OMEGA is expected ~1 Feb
  - after which an EICROC1 ASIC needs to be wire bound to it
    - BNL? (similar to EICROC0)
    - Strasbourg?
    - Both??
    - needs a bit more discussion to go over details…
  - wire-bound EICROC1 expected ~1 Mar at BNL (and Rice)
- Adaptor card is designed at Rice
  - schematics complete
  - layout in progress ⇒ production and assembly will follow (same company)
  - expected delivery ~1 Mar

EICROC1 Testing Schedule

- EICROC1 available at BNL ~1 Mar ⇒ starts our testing
  - can we talk to the ASIC via lpGBT – does I2C work? Do the EICROC1 register values make sense?
  - does the DAQ Interface work: do we see Idle Tokens on the link as expected, is the data format understood?
  - do the Fast Commands work? Does the ASIC react?
  - does the command to pulse the ASIC work? Does the pedestal/pulser data make sense?
- Once we understand the ASIC and confirm interfaces we can continue with mounting of the sensors and real AC-LGAD data
  - first with “nothing” (pedestal, noise) and then lasers & sources (at BNL)
- our target is to get this completed by **May 1st**
  - and potentially be ready for CERN test beams(?)
  - aggressive schedule but doable **iff** the ASIC works without insurmountable issues
    - good communication with ASIC designers will be key

FCFD

- Fermilab's **FCFD** ASIC supports strip AC-LGADs (e.g. BTOF)
- Development underway of FCFD v1.2
  - first version with readout backend compatible with lpGBT
  - supports streaming
  - 6 channels
  - tapeout targeted for Apr/May 2026
  - first Internal Design Review will be scheduled in <2 weeks (new)
    - will give us a better understanding of the interfaces and power needs
- Discussions regarding the ASIC's Testboard started
  - Testboard is expected to be designed in Fermilab as well as first basic tests
- Readout chain
  - will use RBv1 (w lpGBT & VTRx)
  - will likely need its own Adapter Board to be designed and produced (Rice, PED?)
  - and also a different Power Board from PBv1 due to different voltage needs (2.5V?)
    - perhaps we can adapt our PBv1?
    - need to understand FCFD's power needs ⇒ following the Design Review above

Other tests

- we (still) need to measure various sources of jitter (BNL)
- we can use the setup to evaluate the different cabling schemes (BNL?)
  - Roman Pots, B0 etc will need to have the ASIC signals carried via cables from the ASIC Modules to the RB (lpGBT) ⇐ very important for the design of these detectors!
  - which cables and which connectors?
  - what is the influence of the cable length?
    - especially on the clock jitter but also other signals
  - e.g. we can do this by connecting the Testboard ⇔ Adapter with assorted cables under test instead of having direct connectors

Summary

- EICROC1 Readout Chain is being prepared at BNL
  - expected ~1 March 2026
- FCFD Readout Chain is moving along nicely
  - expected to use the existing RBv1 but likely with a different (or adapted) Power Board
    - expectation ~Summer 2026
  - might need a FY26 PED?