CALOROC for SiPM readout at EIC

January 2026 ePIC Collaboration Meeting

January 20-23 2026

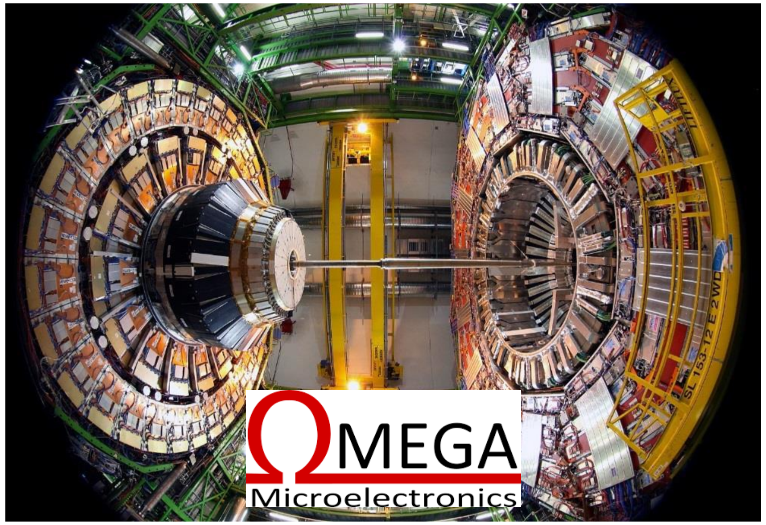
Frederic DULUCQ

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year



CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

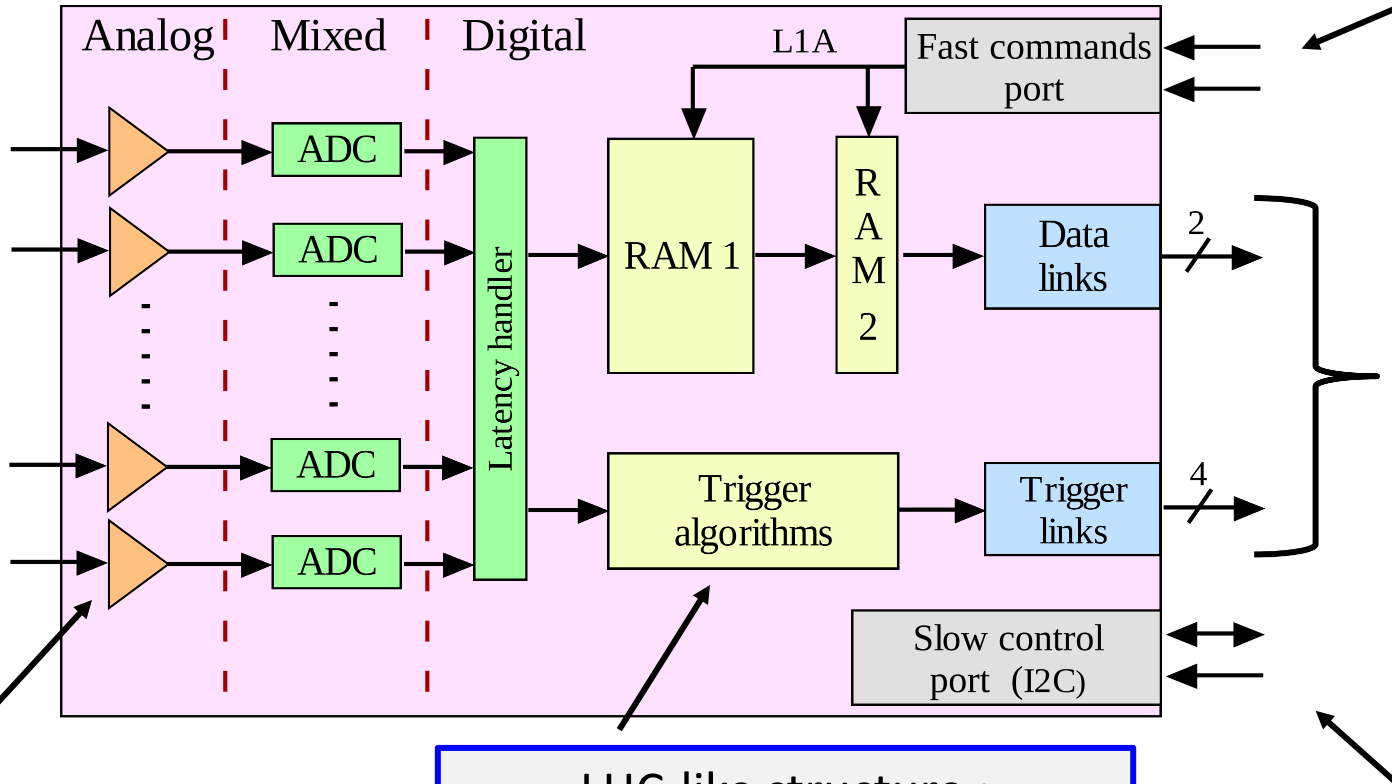
Common interfaces

HEP trend => imaging calorimetry
- High number of channels
- Charge and precise timing (<100 ps)
- Low power + System-On-Chip

Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

ROC chips standard structure

- H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (but interfaces for CALOROC will similar)



Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,26 Gbps)

I2C interface to load the ASIC parameters (slow control interface)

Analog front-end specific to sensor

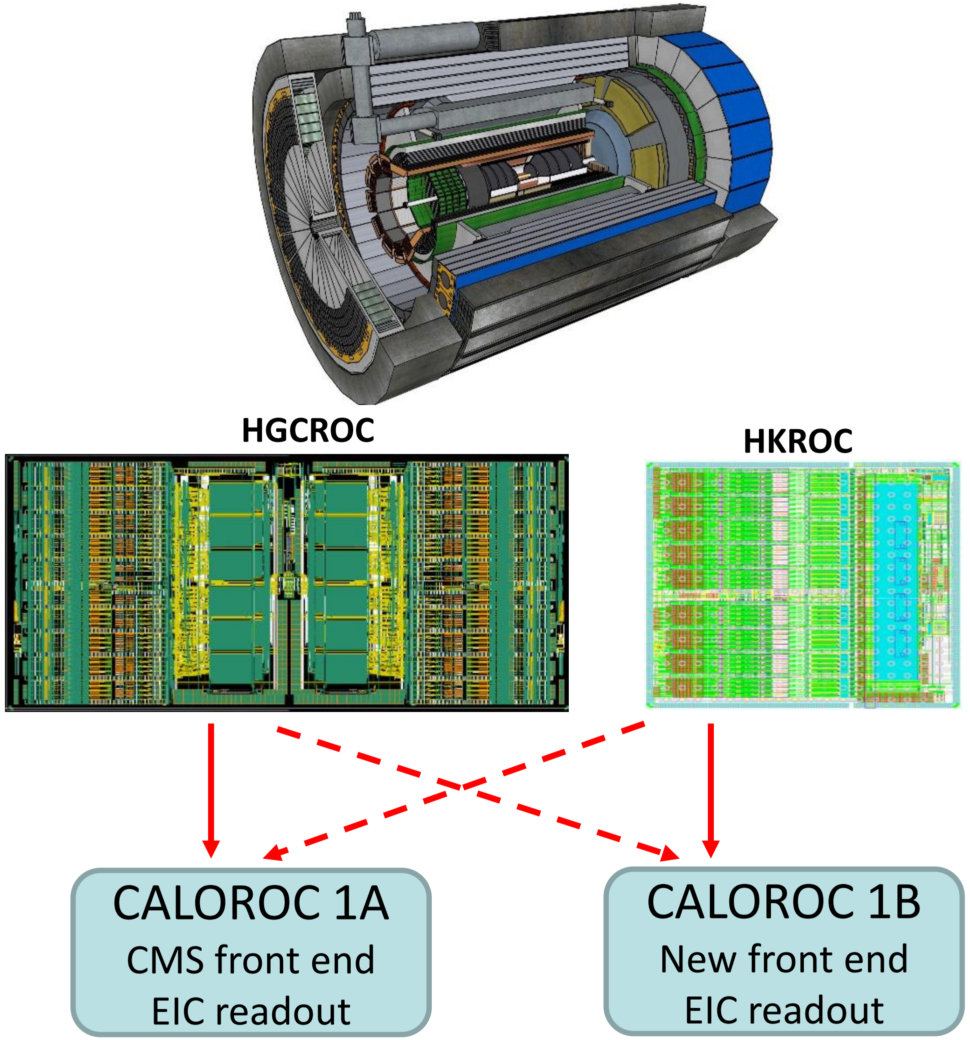
LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

What is CALOROC ?

- CALOROC will be available in 2 versions for SiPM readout:
  - SiPM range capacitance from 560 pF to 8.96 nF
  - ~ 10-15 mW / channel
  - Radiation hardening (HL-LHC levels)
    - 200 Mrad and 10^{16} n_{eq} / cm^2 (1 MeV equivalent neutrons)
    - SEE hardening on control logic
  - Charge and time measurement

- Streaming readout (no external trigger required)
- Conservative CALOROC1A based on CMS H2GCROC:
  - H2GCROC (ADC, TOT) analog/mixed reuse
  - Back-end compatible with EIC + zero-suppress

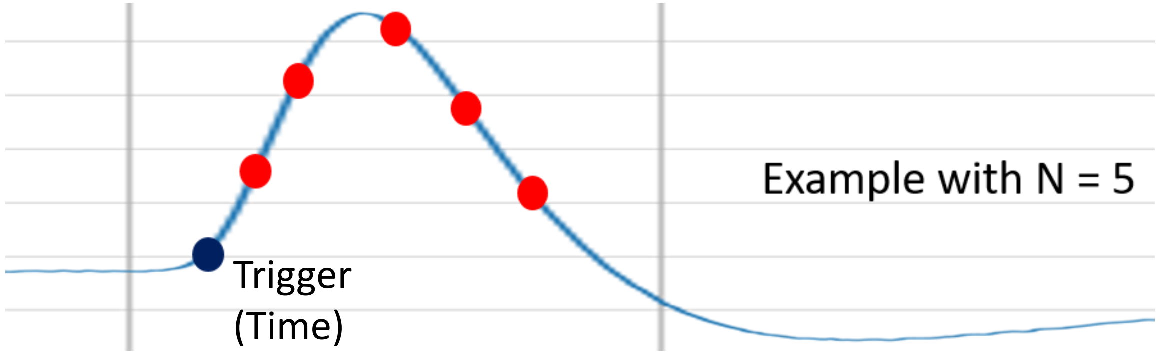
- New CALOROC1B based on gain switching:
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible



CALOROCs will share a common backend
+ pin-pin compatibility

CALOROC: Waveform Digitizer with Auto-Trigger [F. Dulucq]

- CALOROC is a waveform digitizer working @ 39.4 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)



CALOROC can accept ~ 50 kHz rate per channel (worst case)

Internal HKROC memory writing is without dead time

Hit-rate is only limited by serial link bandwidth (average values above)

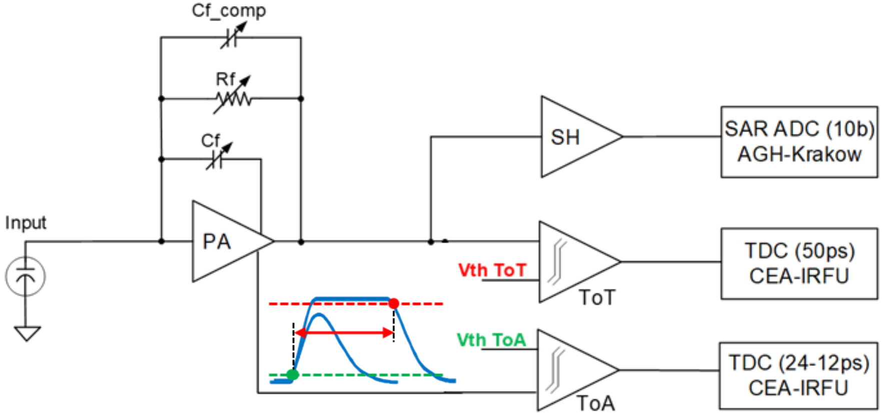
A zero-suppress feature can be activated

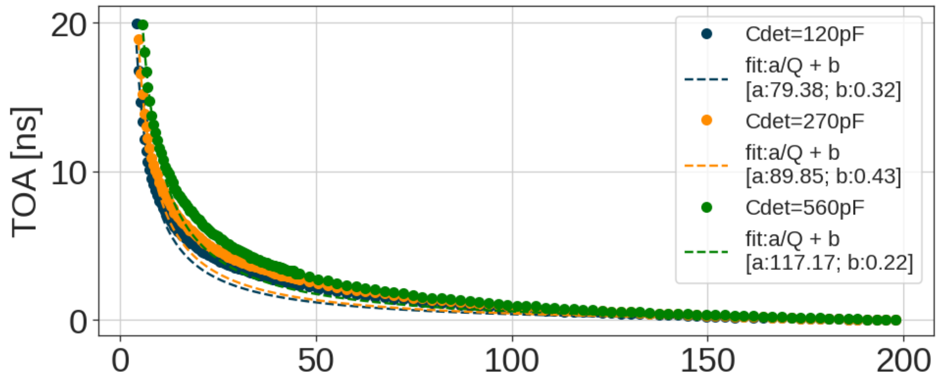
A fast command can trigger an ASIC snapshot

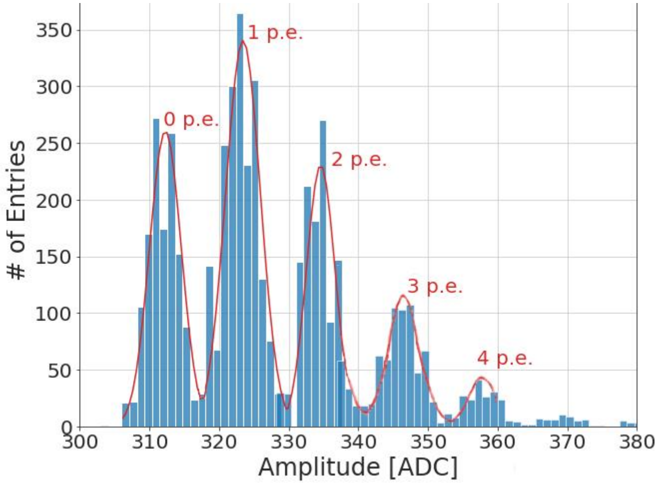
(monitoring, calibration, heartbeat)

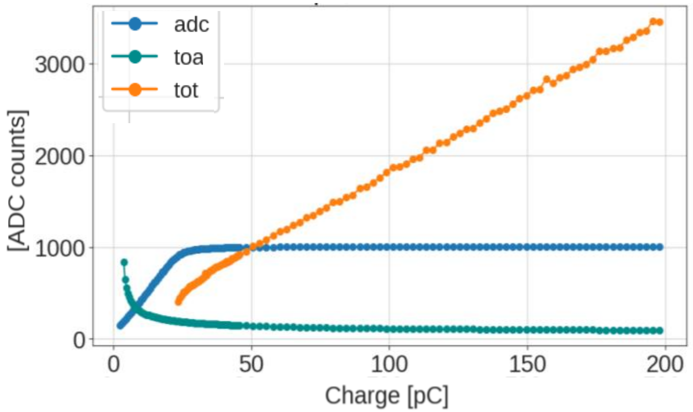
CALOROC1A (based on H2GCROC)

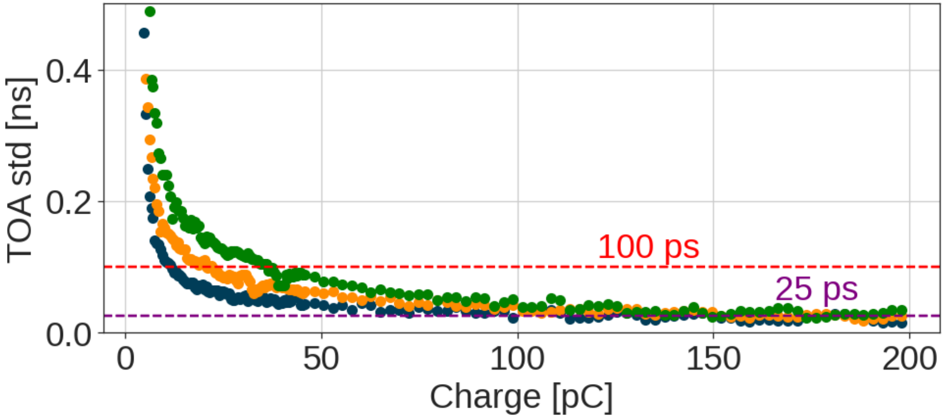
- ❑ Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - ❑ 15 mW per channel / Radiation performance / SiPM range 100-600 pF

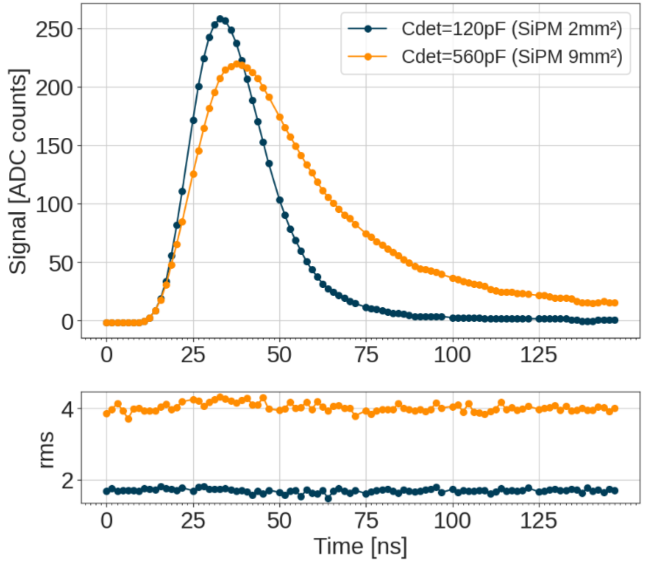










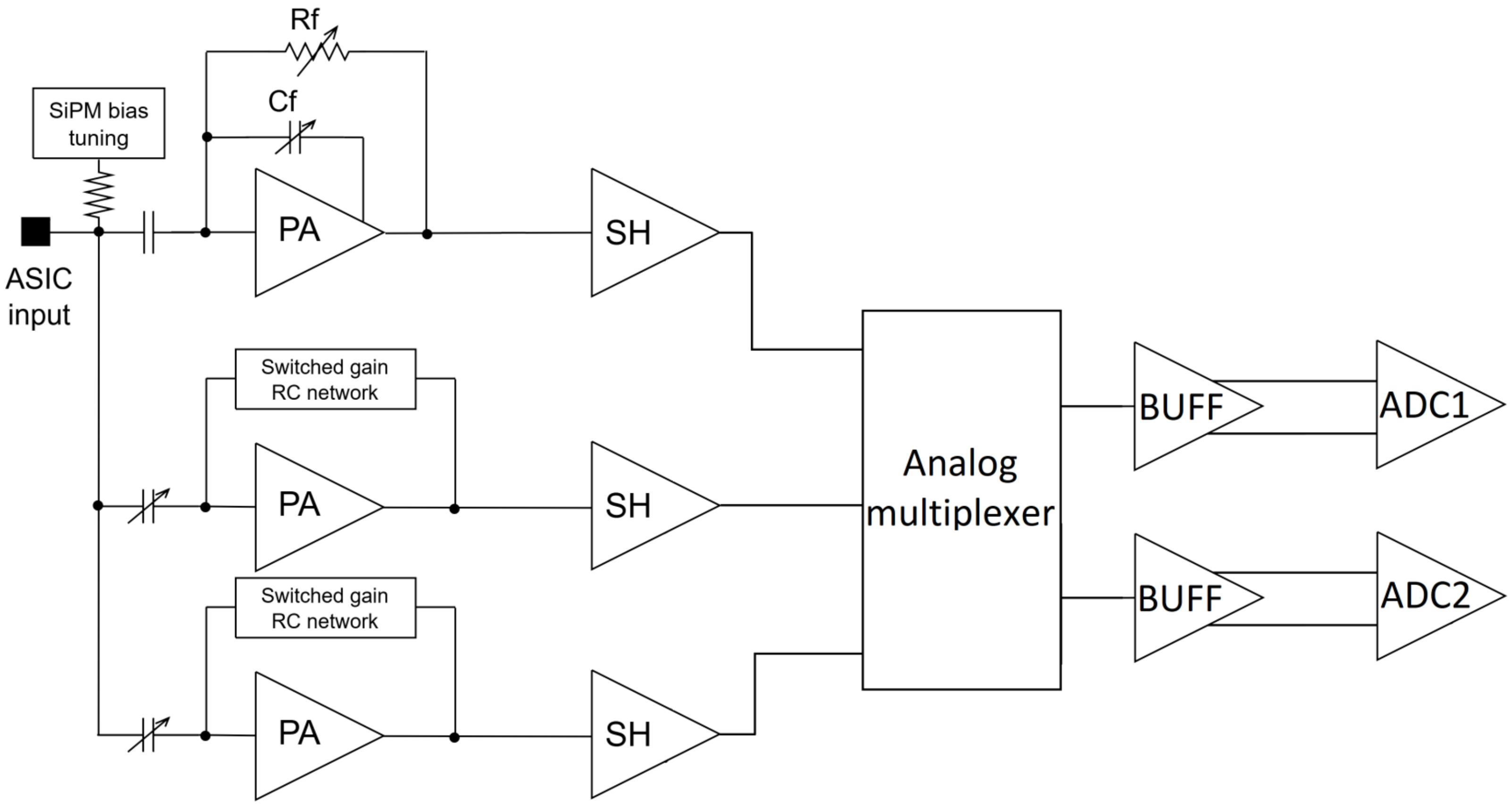


- ❑ CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 → https://doi.org/10.1088/1748-0221/19/04/C04005

CALOROC1B: Channel Architecture

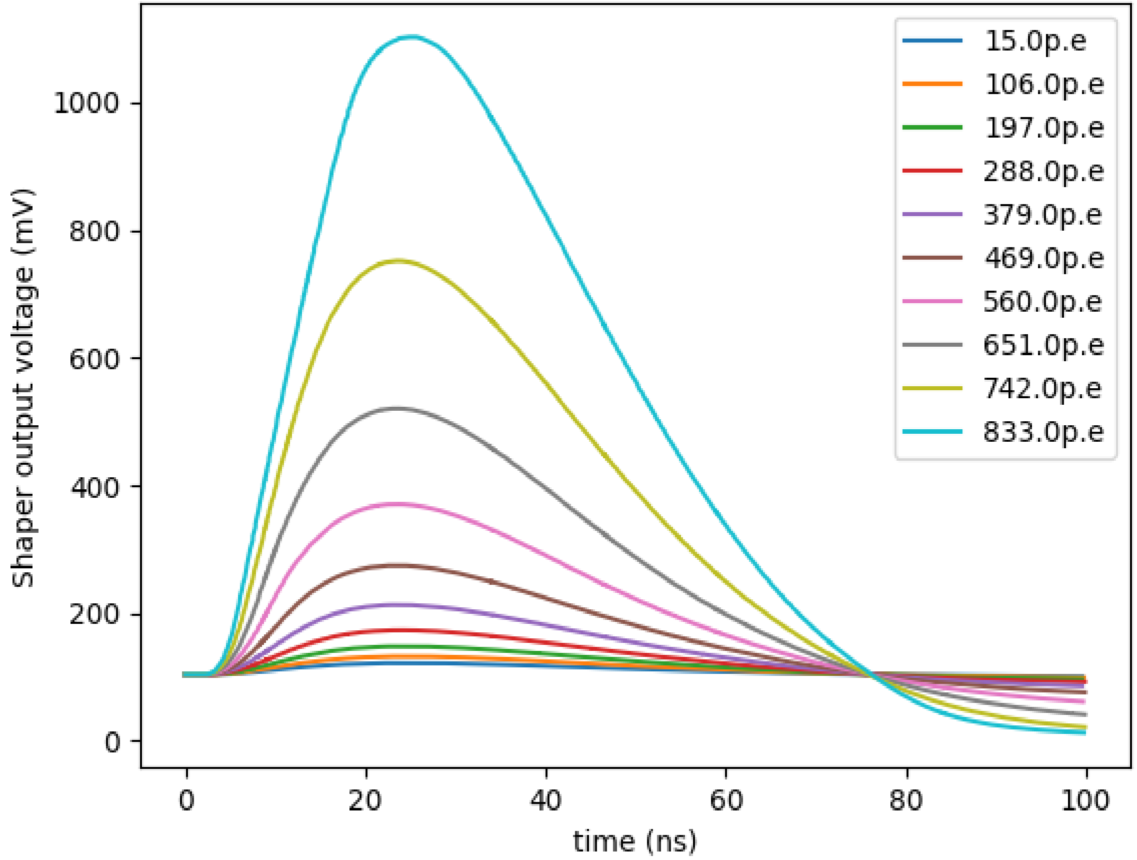
- New dynamic frontend with switched gain:
  - 1 high gain preamplifier
  - 2x low power preamplifier
  - 1 analog multiplexer
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 560 pF to 2.24 – 8.96 nF
  - ~ 10-15 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



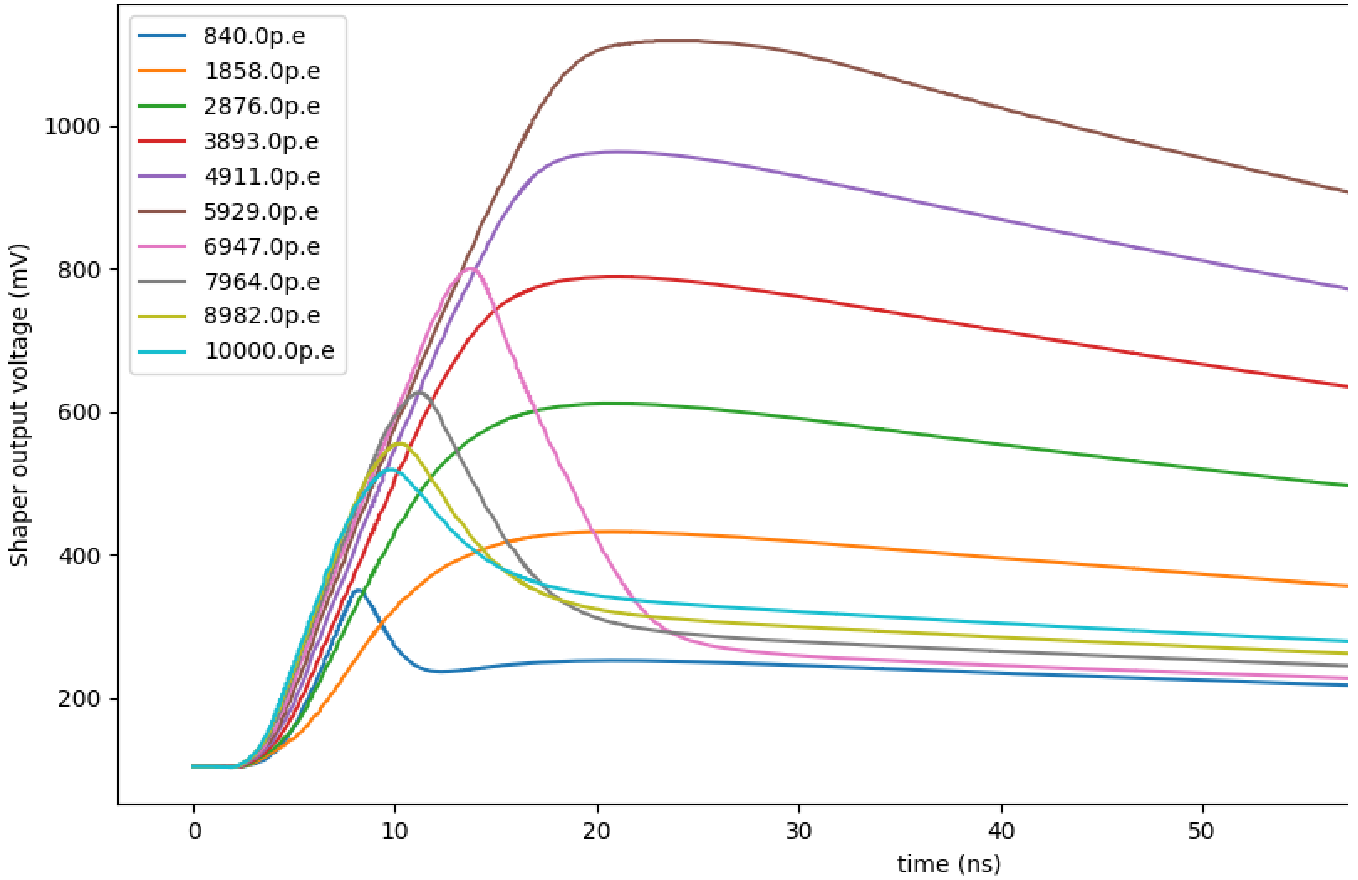
CALOROC1B: Charge and time simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 8.96 nF

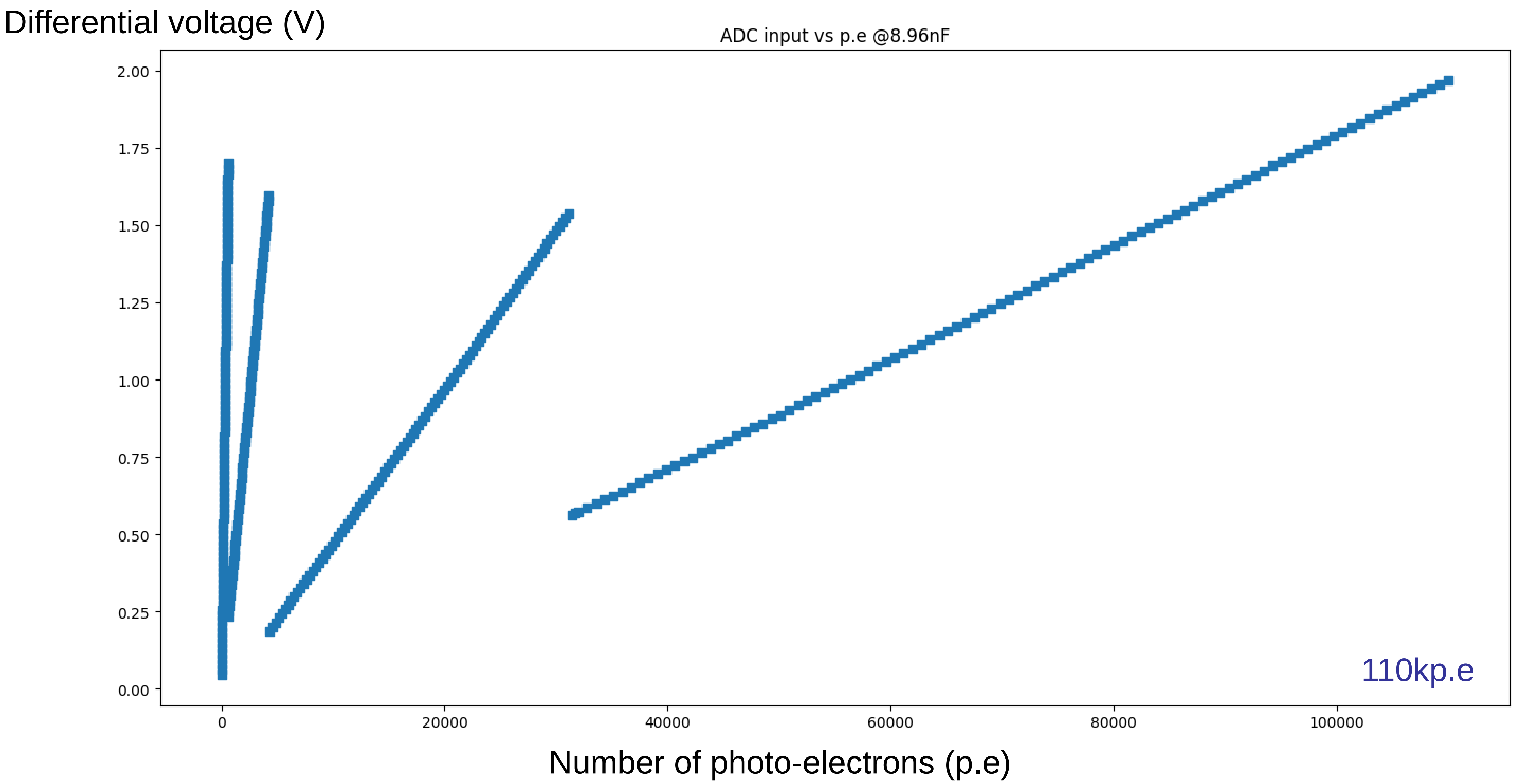
Waveform for high gain shaper @8.96nf configuration



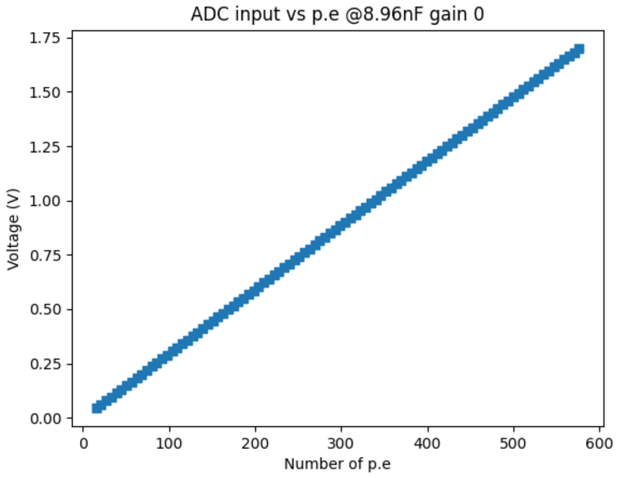
Waveform for medium gain shaper @8.96nf configuration

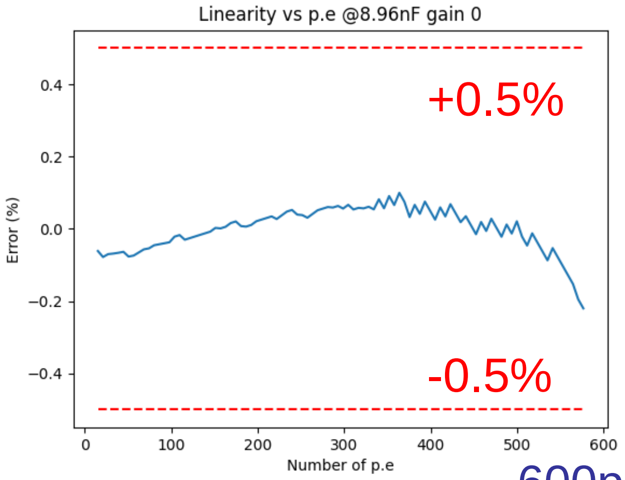


CALOROC1B: Linearity

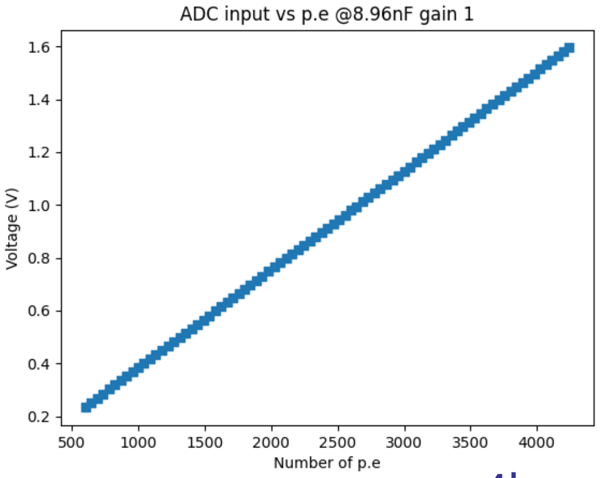


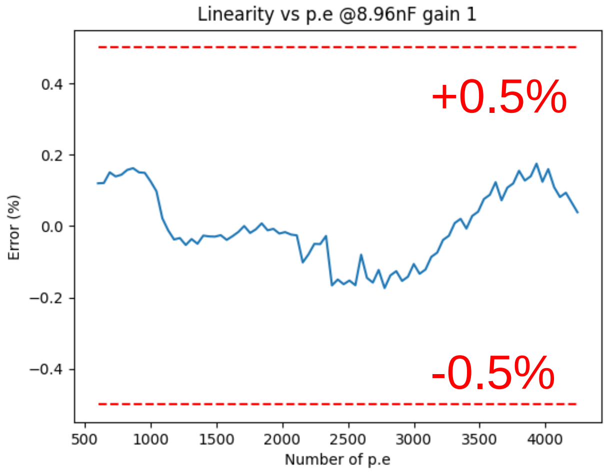
- Less than 1% linearity error



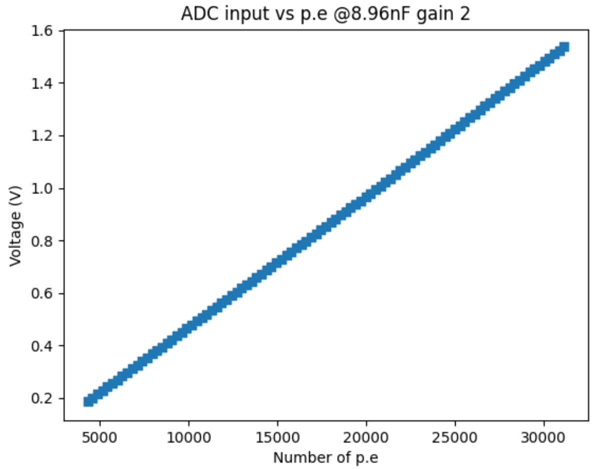


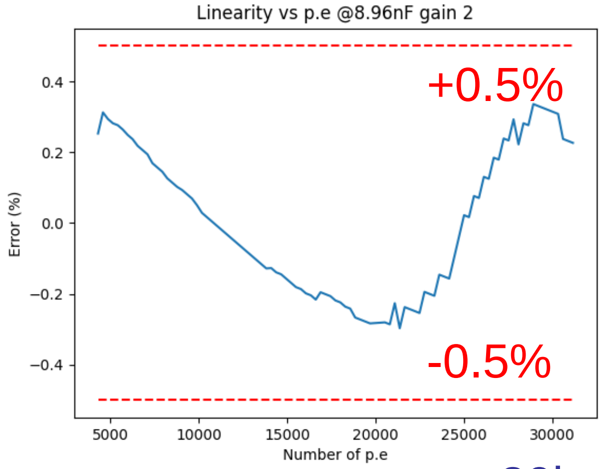
600p.e



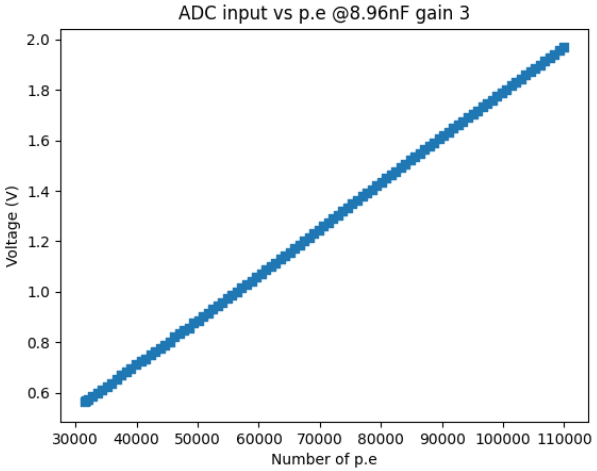


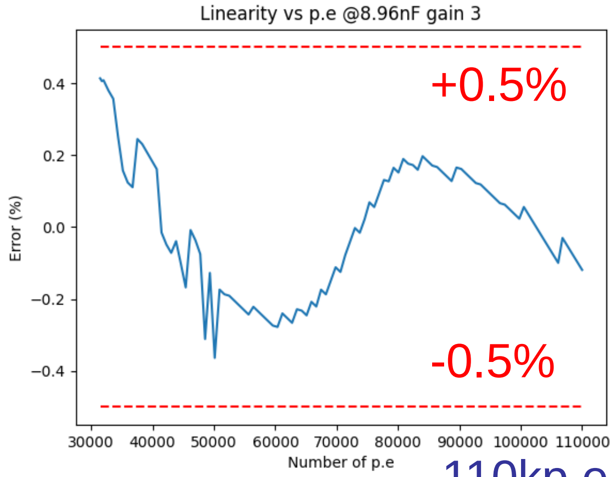
4kp.e





30kp.e

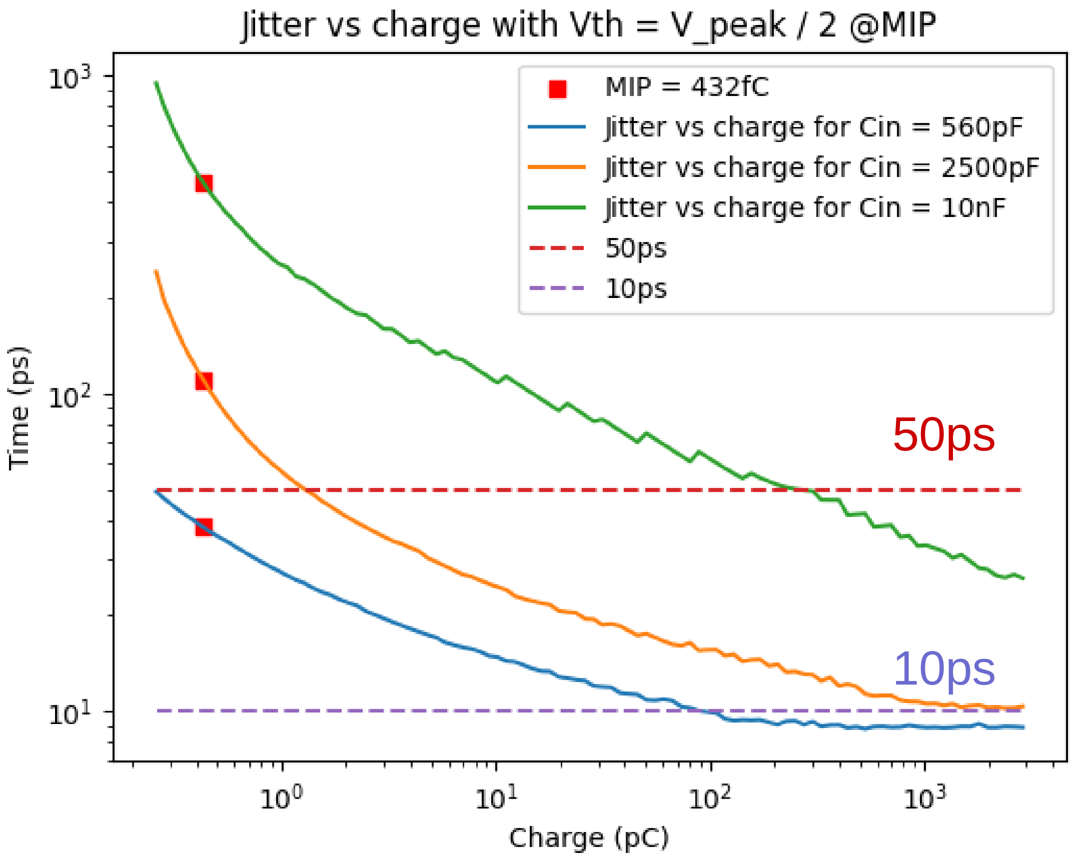


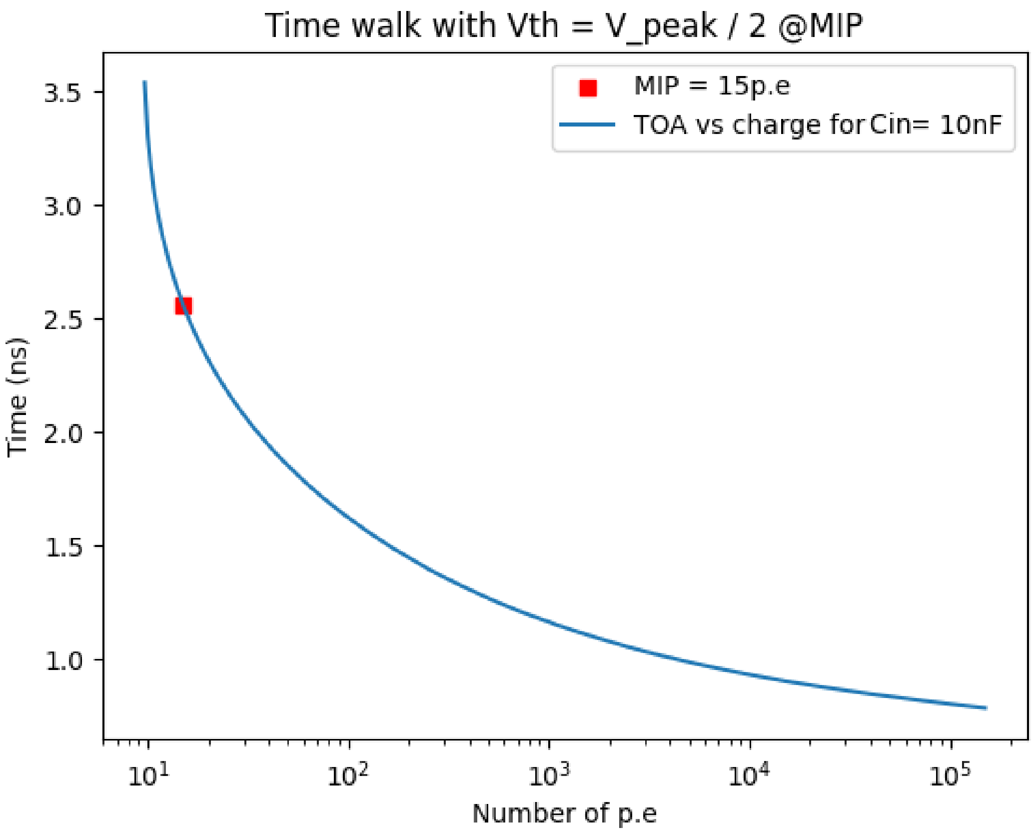


110kp.e

CALOROC1B: Timing precision

- Simulated time jitter goes down to 20 ps with < 500 ps for a MIP of 432fC @Cin=8.96nF
- Time walk is below ~2,5 ns





CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

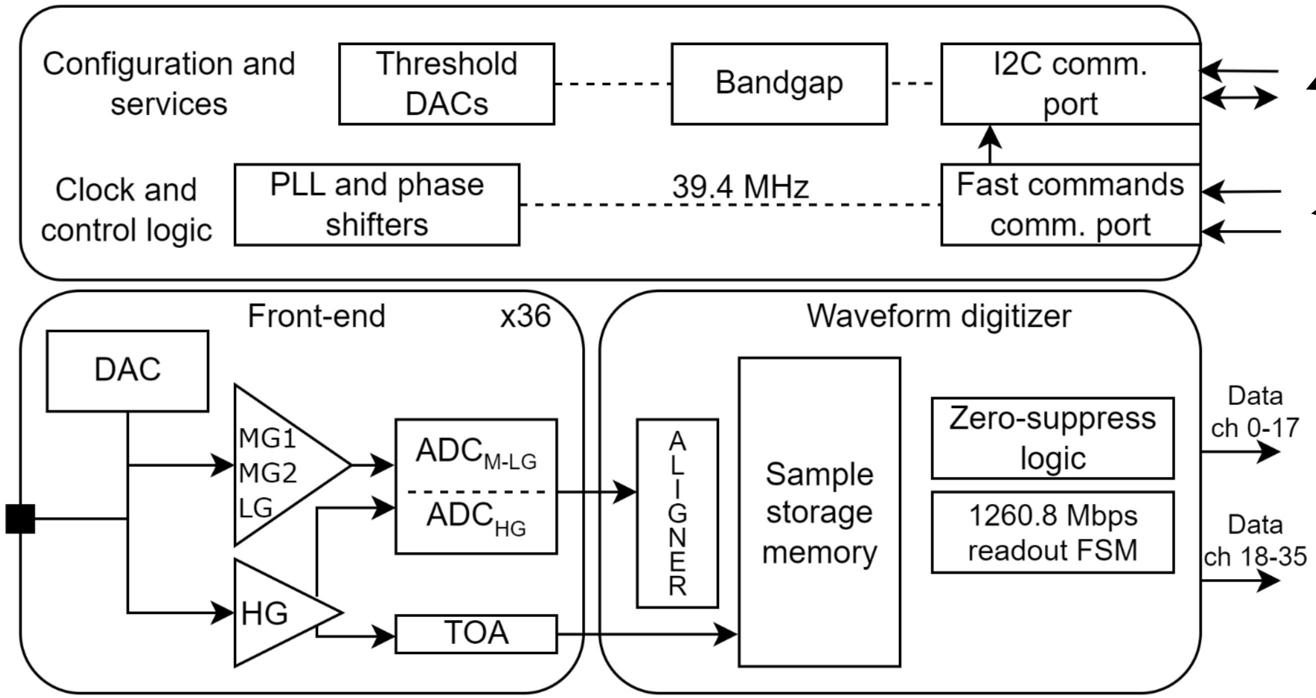
- CALOROC1b will be able to readout SiPM in the range ~ 560 pF to 8.96 nF
  - Timing measurements will focus on the MIP (~15pe)

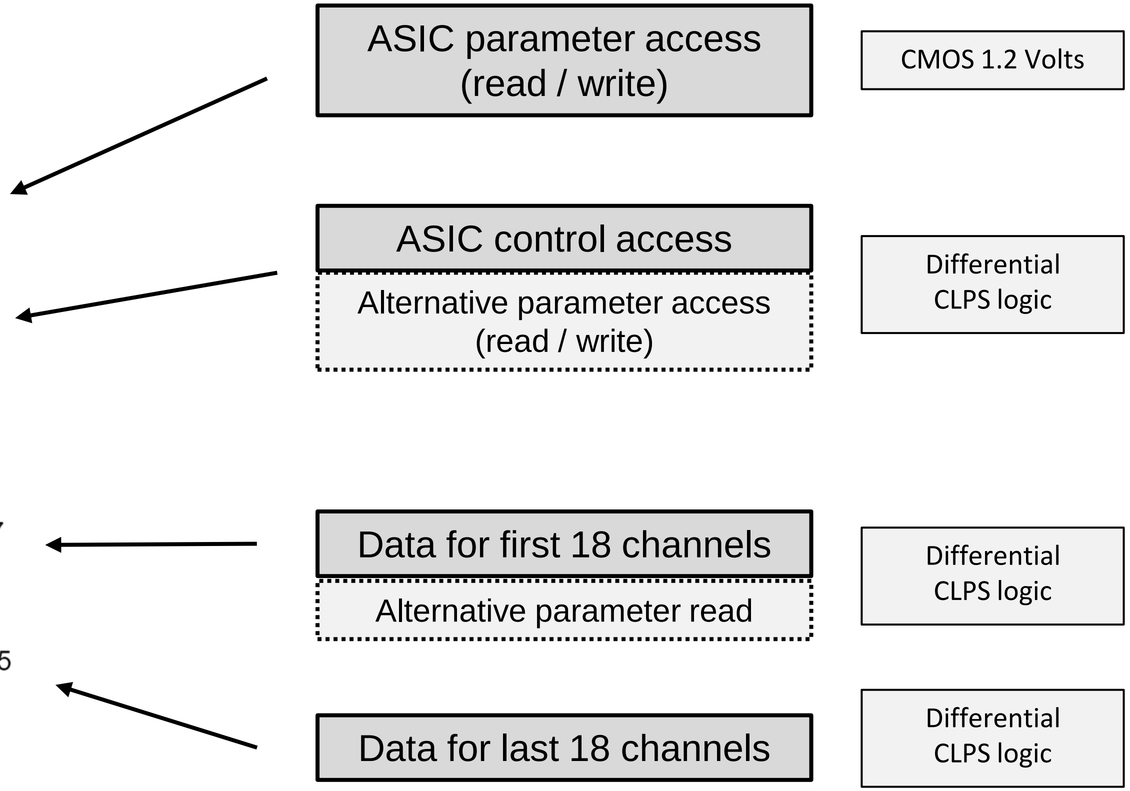
Operation modes	1 SiPM of 560pF Caloroc1B	4 SiPMs of 560pF Caloroc1B	16 SiPMs of 560pF Caloroc1B	1 SiPM of 560pF Caloroc1A
Cin	560pF	2.24nF	8.96nF	560pF
Dynamic range in charge (Noise - Max)	3.2fC-190pC	11fC-790pC	45fC-3.17nC	20fC-320pC
Input time constant (occupancy related)	112ns	450ns	450ns	10ns
Jitter @ MIP (≈400fC)	42ps	130ps	520ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	9	2.6	0.64	1.44

SiPM: S14160-3010PS 3x3mm (560pF)

CALOROC: Block Diagram – Interfaces [F. Dulucq]

- CALOROCs will have the same interfaces (comparable to CMS ones):
  - 1 clock @ 315.2 MHz + 2 resets (hard + soft)
  - Fast command to dynamically control the ASIC (differential)
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)





CALOROC: Fast Commands

- Commands to interact dynamically with the ASIC
  - 8 bits commands synchronized with incoming 315.2 MHz clock – MSB first
  - Only idle needed – others have a known latency
  - Detailed in the datasheet

Fast commands	Value	Description
Idle	00110110	Default command inside
ChipSync	11010010	Reset FSM, buffers and counters
BCR	00011101	Reset timestamp counter to a default value
EBR	11010001	Empty readout buffers
PING	10011001	Ping status and counters
LinkResetROCD	10011010	Transmission of synchronization patterns
ROC-Serializer-Reset	10011100	Reset serializer link module only
L1A	01001011	External trigger (all channels)
CalPulseInt	00101101	800 ns internal calibration pulse
CalPulseExt	01111000	100 ns external calibration pulse
SC_0	01011010	I2C over fast command - send '0'
SC_1	01011100	I2C over fast command - send '1'
SC_Valid_Reset	10001011	Valid or reset (2 consecutives) current transaction

Default command (Idle)

Resets and synchronization (ChipSync, BCR, EBR, PING)

Serial links recovery (LinkResetROCD, ROC-Serializer-Reset)

Calibration and pseudo-heartbeat (L1A, CalPulseInt, CalPulseExt)

Slow control (I2C) over fast commands (SC_0, SC_1, SC_Valid_Reset)

CALOROC: Readout Frames

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

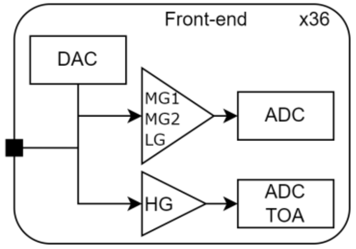
CALOROC A (CMS-like)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1	
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map	
Tc	Tp	10b ADC-1	10b ADC or TOT (Tc = 1)	10b TOA	
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA	
⋮					
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA	
CRC					
Idle/Sync Header	28b default IDLE Pattern				

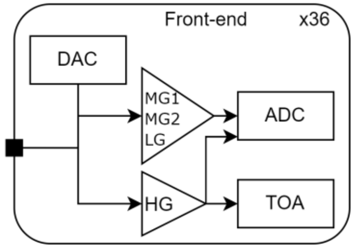
CALOROC B – 2 ADCs or 1 ADC (4 gains)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1	
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map	
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA		
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA		
⋮					
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA		
CRC					
Idle/Sync Header	28b default IDLE Pattern				

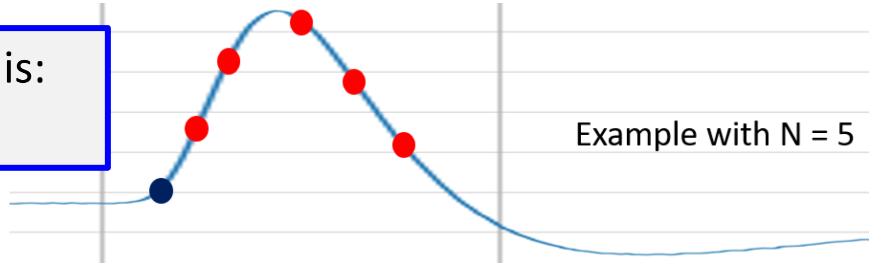
CALOROCB (2 ADCs)



CALOROCB (1 ADCs)



In ZS mode, for **X** (1-18) hit channels and **N** samples, number of 32-bit words is:
N x (2Headers + **X** + 2Trailers)



In characterization mode, forced TcTp, ADC, TOT, TOA for all channels

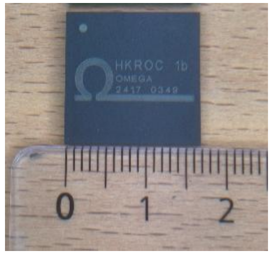
Test System for Characterization

- CALOROC characterization motherboard under design at OMEGA:
  - Originally developed for HGCROC and the HKROC
  - Well-known at OMEGA and LLR (firmware based only)
  - Compatible with KRIA motherboard (CERN) but software + firmware needed

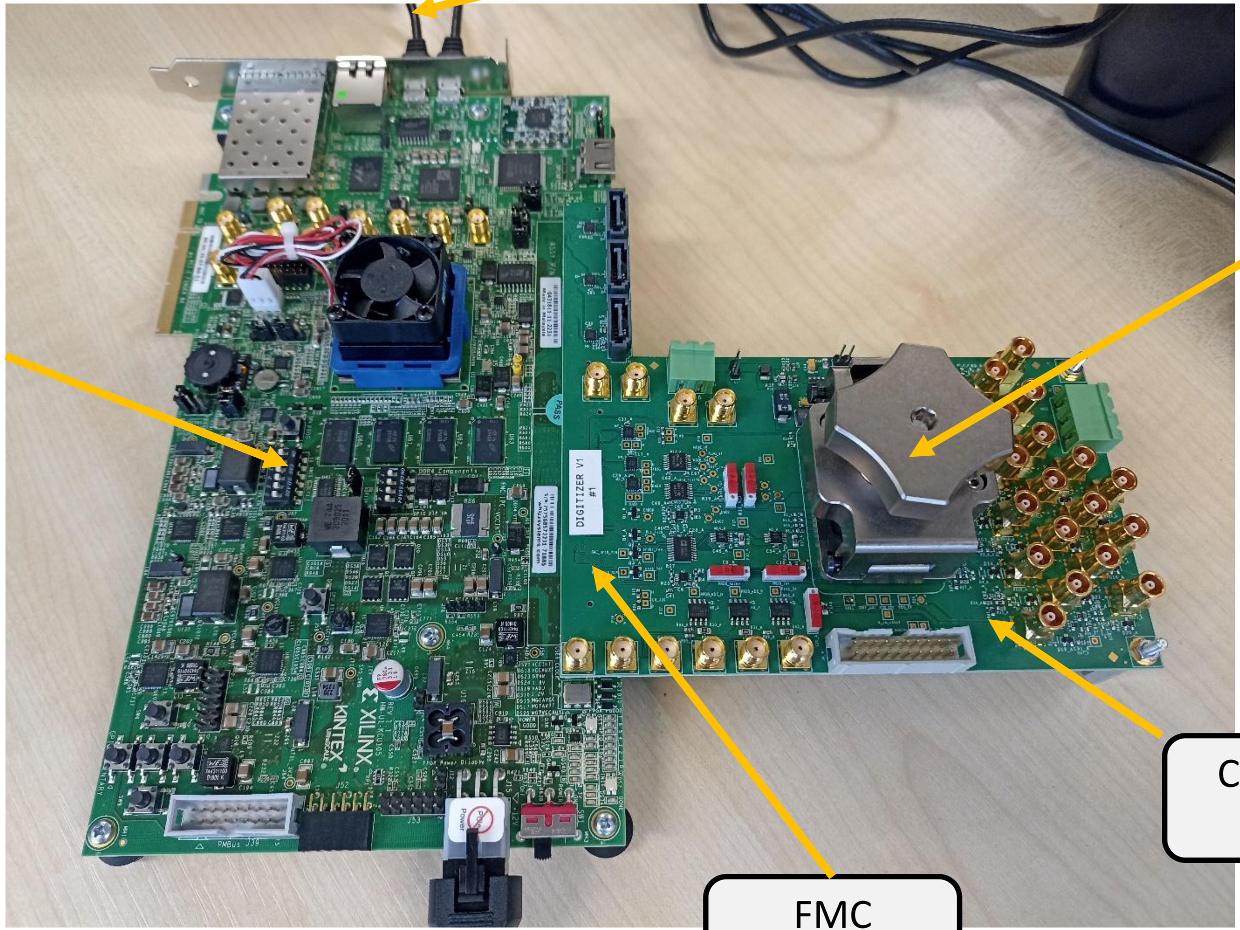
Python scripts

Monitor Program Test

CALOROC BGA socket

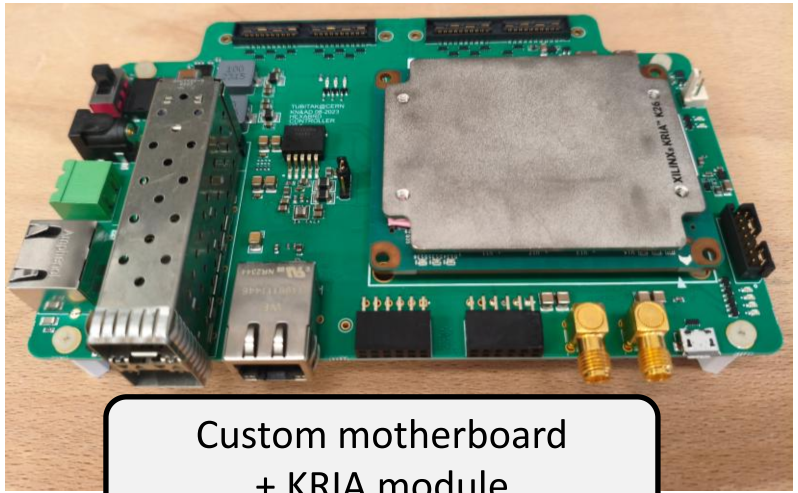


Commercial KCU105 board



Custom CALOROC motherboard

FMC connector



Custom motherboard + KRIA module

First Measurements Plan

- ASIC sanity checks
  - Power consumption of each part
  - Bias value versus simulation

- Validating interfaces (could be done in parallel)
  - Accessing the parameters (I2C only)
  - Reading ASIC output (high speed serial links)

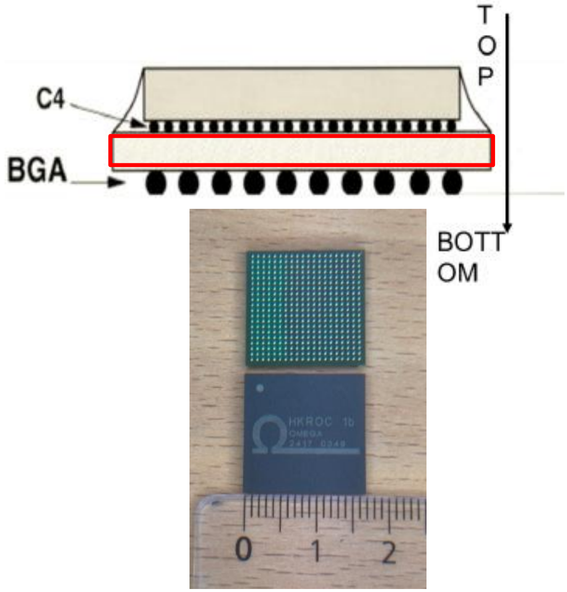
At this stage, more in-depth characterization tests could be performed

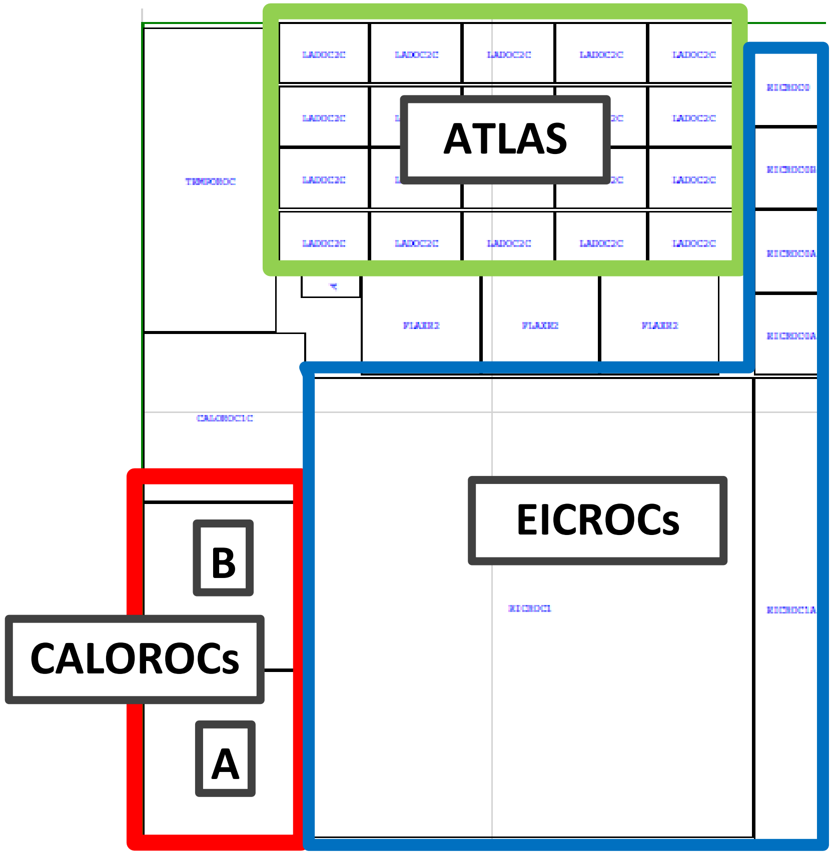
- ASIC front-end characterization
  - Linearity / Noise
  - Analog to digital conversion
  - CALO-A: Reproduce H2GCROC performances
  - CALO-B: Validation of switch-gain mechanism

Results will drive CALOROC2 design → Q1 2027
Possibly room for improvements (Hit rates ?)

Summary and Status

- **CALOROCs** are in the wafer dicing process
  - Prior to packaging (die + substrate)
  - Expected in March at the lab
- About 150 chips will be available
  - Same amount for both CALOROCs
  - 10-20 in the first batch in March
- ASICs characterization testboards
  - 1x CALOROC-compatible testboard available at OMEGA
  - 3x CALOROC-compatible-v2 available end of February
  - 5x CALOROC with full functionalities available in April
- +2 types of Front-End Boards





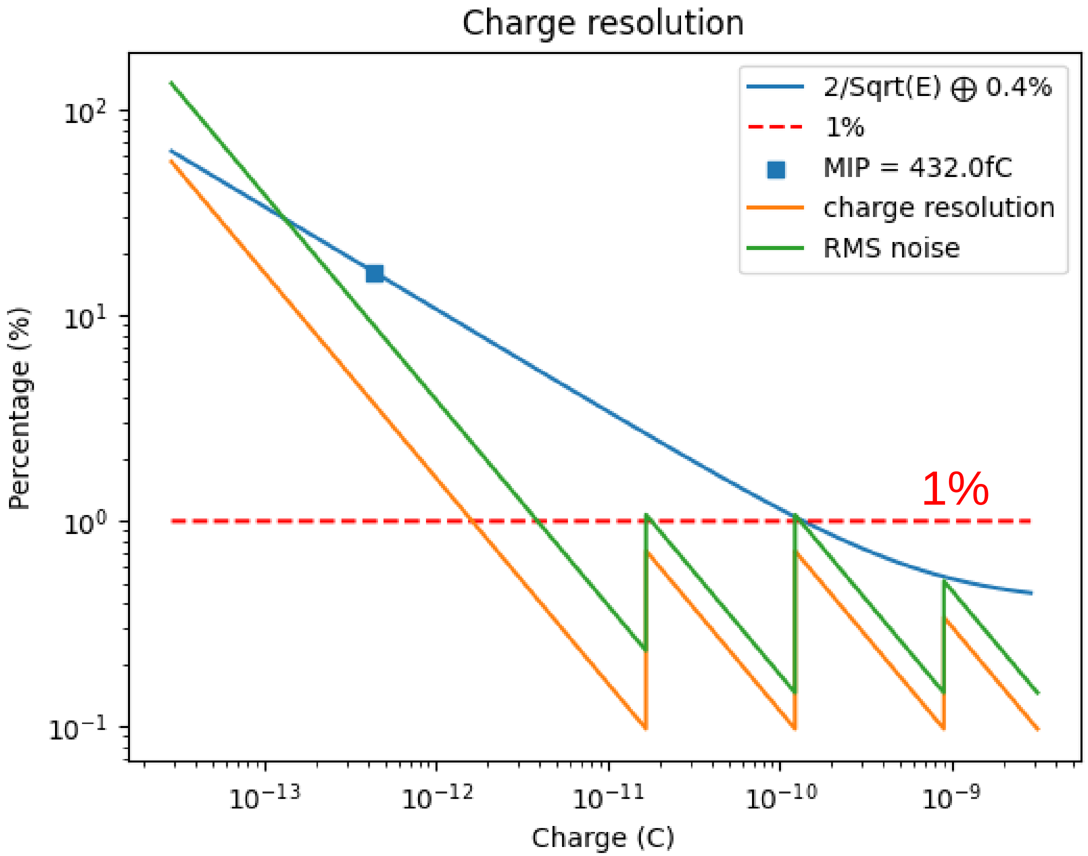
CALOROCs are targeted to include all features + radiation hardness on the first submission

Backups

CALOROC1B: Dynamic range and resolution

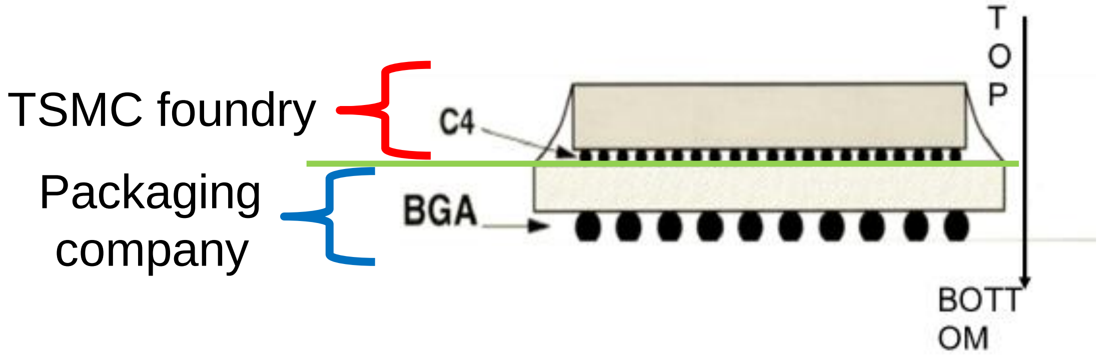
- The SiPM configuration has a direct impact on the dynamic range
  - The highest measurable charge is determined by the SiPM input capacitance.
  - The ratio between the highest and the lowest measurable charge is constant (dynamic range ratio).

- 10b resolution and 17b dynamic range
  - With a 10b ADC and 4 gains (2b) we have a resolution of 17b
  - The measured charge is in the format of $10b * GainRatio^{2b}$
  - The gain ratio can be adjusted to increase the dynamic range in exchange for a lower resolution.
  - Using the highest resolution the dynamic range ratio is 70k
  - Supposing 1MeV = 1p.e for the 8.96nF setup this should give us a dynamic range of 1.5MeV (noise floor) to 110GeV



CALOROC Packaging

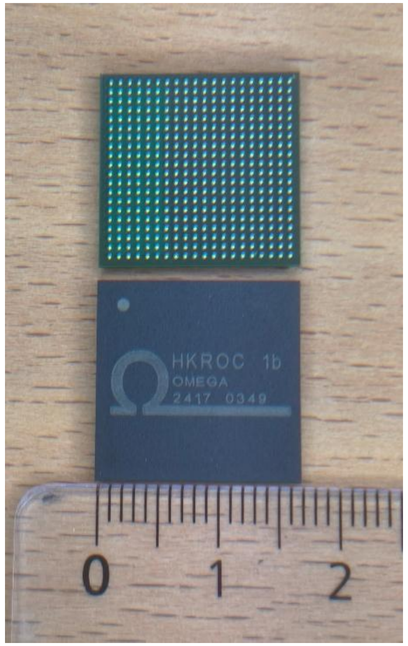
- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0.8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3



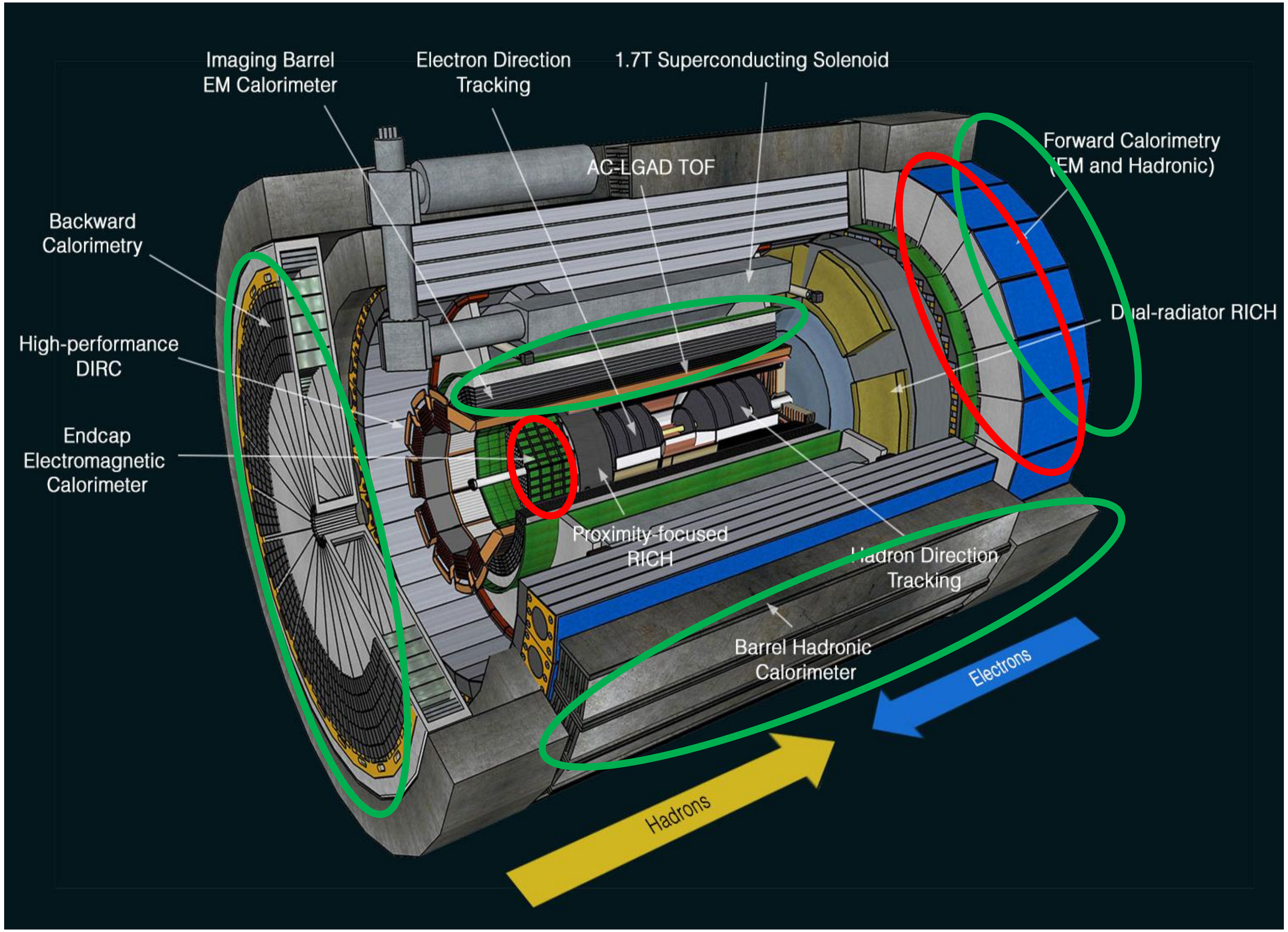
JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216

TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2



Calorimetry at ePIC



13 Calorimeters:

- 7 x SiPM – CALOROC
- 5 x SiPM – Discrete
- 1 x SiPM – Commercial fADC250

From J. Landgraf

(IDR review)