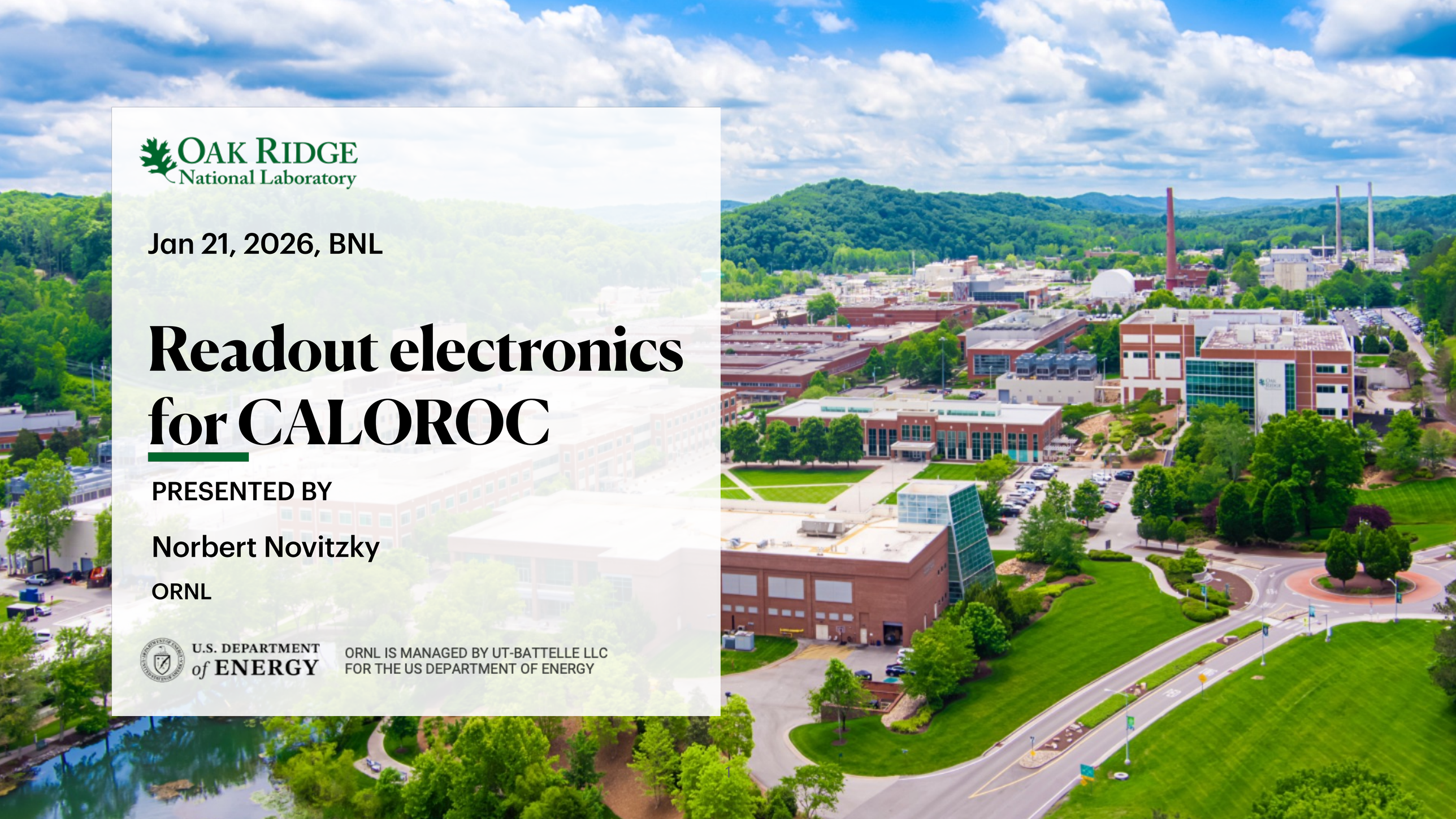

OAK RIDGE National Laboratory

Jan 21, 2026, BNL

Readout electronics for CALOROC

PRESENTED BY

Norbert Novitzky

ORNL

U.S. DEPARTMENT of ENERGY

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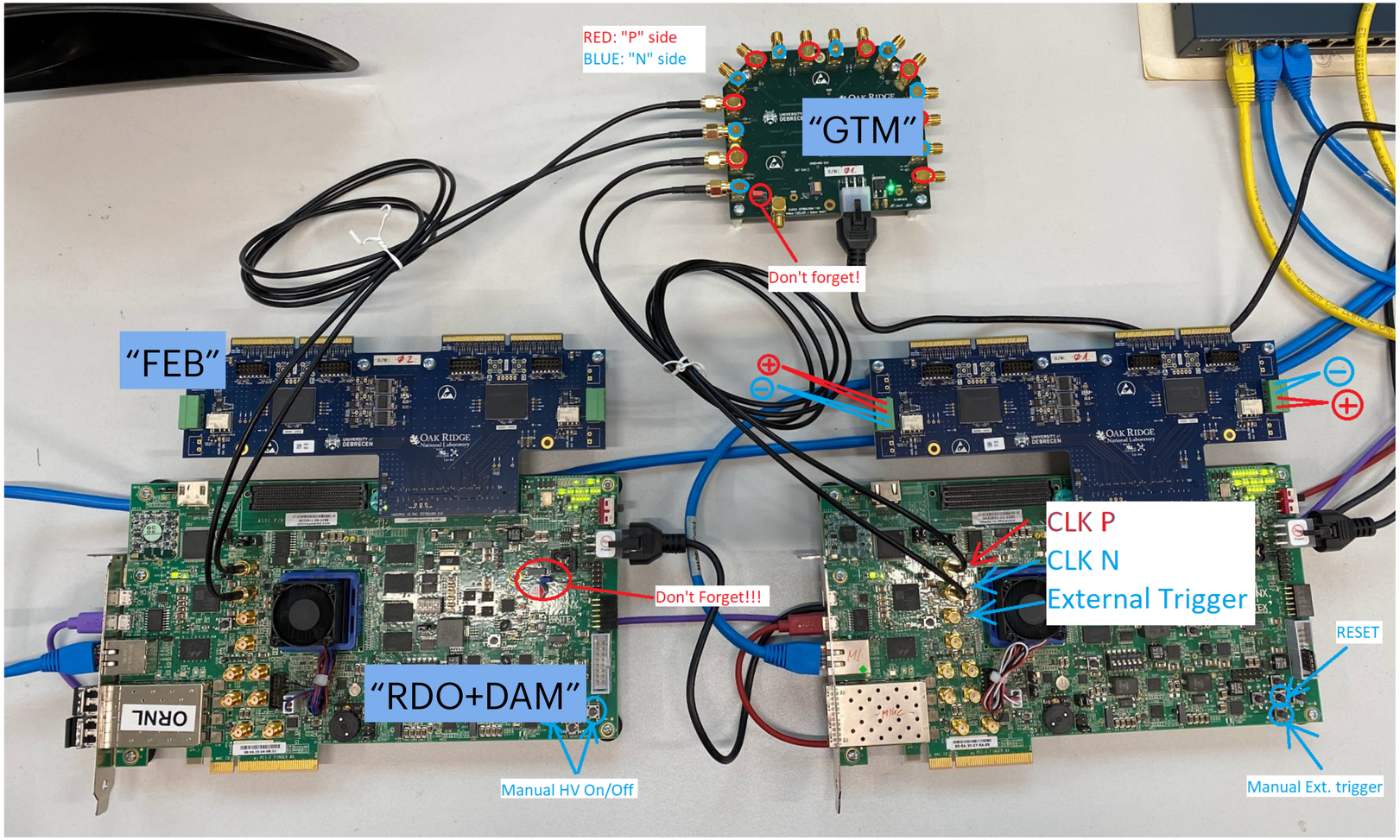
FOR THE US DEPARTMENT OF ENERGY

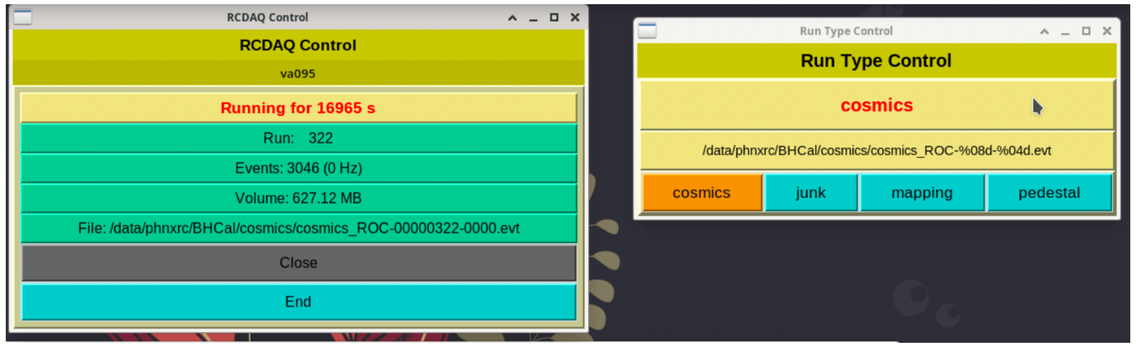
Where are we at



We have a protoboard2.0 supported from the eRD109:

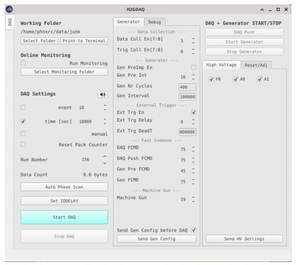
- Containing 2 H2GCROCs
- KCU firmware for readout
  - Now upgraded to 10Gbps readout
  - 2 protoboard per KCU is supported
- We produced ~20 protoboards, all calorimeters have a board
- Clock board, interface boards, trigger boards, cables, etc
  - These are supporting the readout, but it is also 'work and money'

Software



After the upgrade for 10Gbps, the python3 GUI is not really great (unless you limit the trigger rate)

Moved to RCDAQ

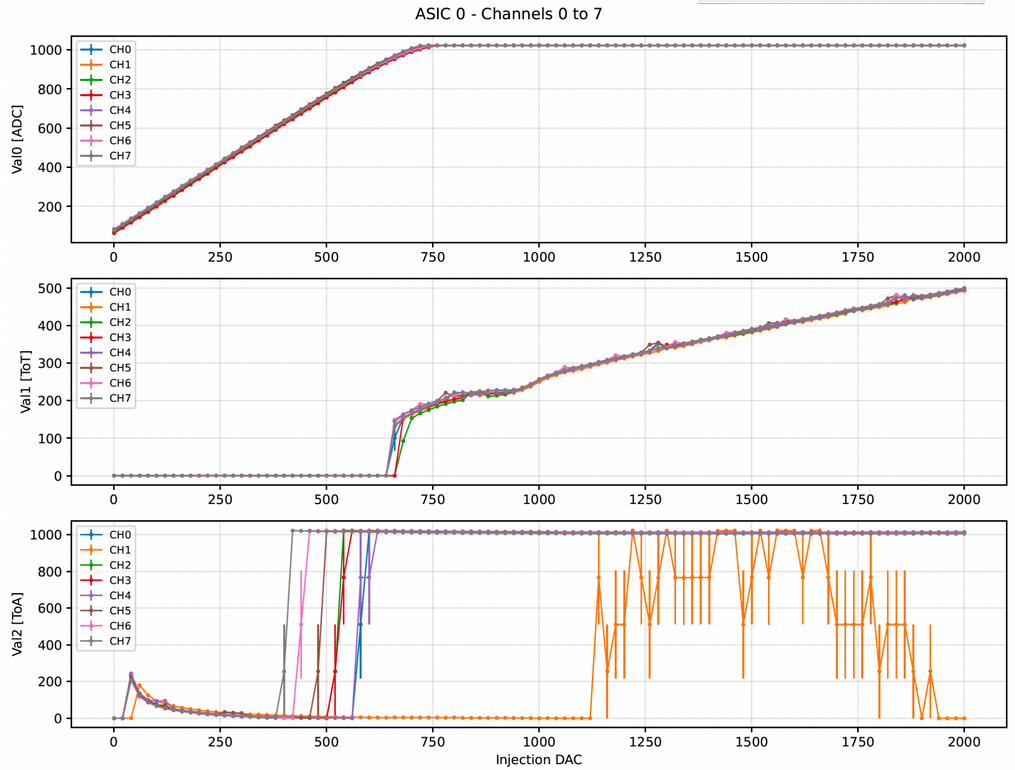


We keep the slow control

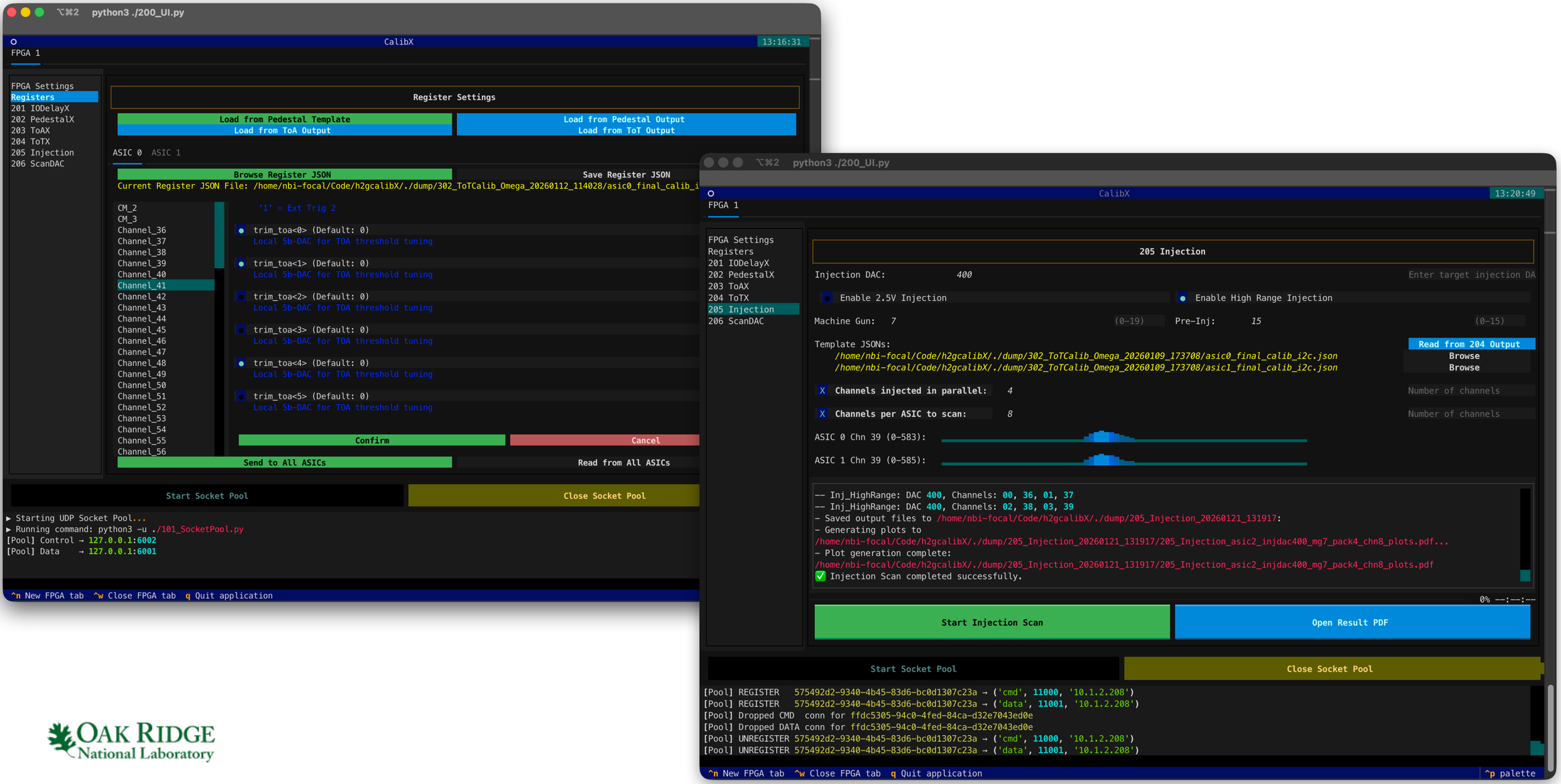
- I2C settings for the chip

and calibration in a python script:

- ADC calibration
- TOA and TOT calibration
- Injection tests
- Dac scan (for checking the full range)



Software 2


⌥⌘2 python3 ./200_UI.py
CalibX
13:16:31
FPGA 1
FPGA Settings
Registers
201 IODelayX
202 PedestalX
203 ToAX
204 ToTX
205 Injection
206 ScanDAC
Register Settings
Load from Pedestal Template
Load from Pedestal Output
Load from ToA Output
Load from ToT Output
ASIC 0 ASIC 1
Browse Register JSON
Save Register JSON
Current Register JSON File: /home/nbi-focal/Code/h2gcalibX/./dump/302_ToTCalib_Omega_20260112_114028/asic0_final_calib_i
CM_2
CM_3
Channel_36
Channel_37
Channel_38
Channel_39
Channel_40
Channel_41
Channel_42
Channel_43
Channel_44
Channel_45
Channel_46
Channel_47
Channel_48
Channel_49
Channel_50
Channel_51
Channel_52
Channel_53
Channel_54
Channel_55
Channel_56
'1' = Ext Trig 2
trim_toa<0> (Default: 0)
Local 5b-DAC for TOA threshold tuning
trim_toa<1> (Default: 0)
Local 5b-DAC for TOA threshold tuning
trim_toa<2> (Default: 0)
Local 5b-DAC for TOA threshold tuning
trim_toa<3> (Default: 0)
Local 5b-DAC for TOA threshold tuning
trim_toa<4> (Default: 0)
Local 5b-DAC for TOA threshold tuning
trim_toa<5> (Default: 0)
Local 5b-DAC for TOA threshold tuning
Confirm
Cancel
Send to All ASICs
Read from All ASICs
Start Socket Pool
Close Socket Pool
▶ Starting UDP Socket Pool...
▶ Running command: python3 -u ./101_SocketPool.py
[Pool] Control → 127.0.0.1:6002
[Pool] Data → 127.0.0.1:6001
^n New FPGA tab ^w Close FPGA tab q Quit application
⌥⌘2 python3 ./200_UI.py
CalibX
13:20:49
FPGA 1
FPGA Settings
Registers
201 IODelayX
202 PedestalX
203 ToAX
204 ToTX
205 Injection
206 ScanDAC
205 Injection
Injection DAC: 400
Enter target injection DA
Enable 2.5V Injection
Enable High Range Injection
Machine Gun: 7 (0-19)
Pre-Inj: 15 (0-15)
Template JSONs:
/home/nbi-focal/Code/h2gcalibX/./dump/302_ToTCalib_Omega_20260109_173708/asic0_final_calib_i2c.json
/home/nbi-focal/Code/h2gcalibX/./dump/302_ToTCalib_Omega_20260109_173708/asic1_final_calib_i2c.json
Read from 204 Output
Browse
Browse
X Channels injected in parallel: 4
Number of channels
X Channels per ASIC to scan: 8
Number of channels
ASIC 0 Chn 39 (0-583):
ASIC 1 Chn 39 (0-585):
-- Inj_HighRange: DAC 400, Channels: 00, 36, 01, 37
-- Inj_HighRange: DAC 400, Channels: 02, 38, 03, 39
- Saved output files to /home/nbi-focal/Code/h2gcalibX/./dump/205_Injection_20260121_131917:
- Generating plots to
/home/nbi-focal/Code/h2gcalibX/./dump/205_Injection_20260121_131917/205_Injection_asic2_injdac400_mg7_pack4_chn8_plots.pdf...
- Plot generation complete:
/home/nbi-focal/Code/h2gcalibX/./dump/205_Injection_20260121_131917/205_Injection_asic2_injdac400_mg7_pack4_chn8_plots.pdf
✅ Injection Scan completed successfully.
0% --:--:--
Start Injection Scan
Open Result PDF
Start Socket Pool
Close Socket Pool
[Pool] REGISTER 575492d2-9340-4b45-83d6-bc0d1307c23a → ('cmd', 11000, '10.1.2.208')
[Pool] REGISTER 575492d2-9340-4b45-83d6-bc0d1307c23a → ('data', 11001, '10.1.2.208')
[Pool] Dropped CMD conn for ffdc5305-94c0-4fed-84ca-d32e7043ed0e
[Pool] Dropped DATA conn for ffdc5305-94c0-4fed-84ca-d32e7043ed0e
[Pool] UNREGISTER 575492d2-9340-4b45-83d6-bc0d1307c23a → ('cmd', 11000, '10.1.2.208')
[Pool] UNREGISTER 575492d2-9340-4b45-83d6-bc0d1307c23a → ('data', 11001, '10.1.2.208')
^n New FPGA tab ^w Close FPGA tab q Quit application
^p palette

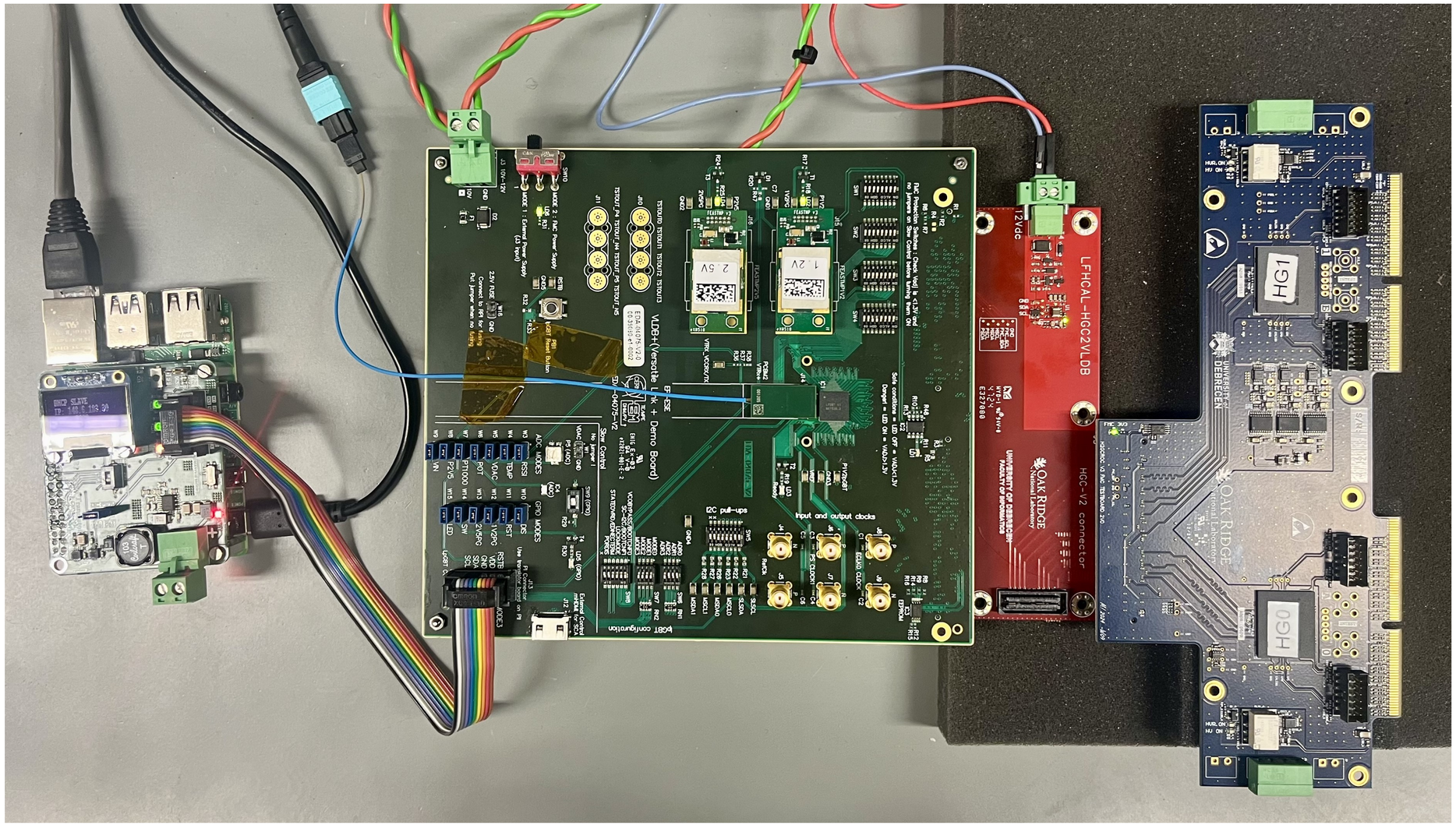
Some challenges of the readout

Protoboard was made to make the first tests with the existing H2GCROC:

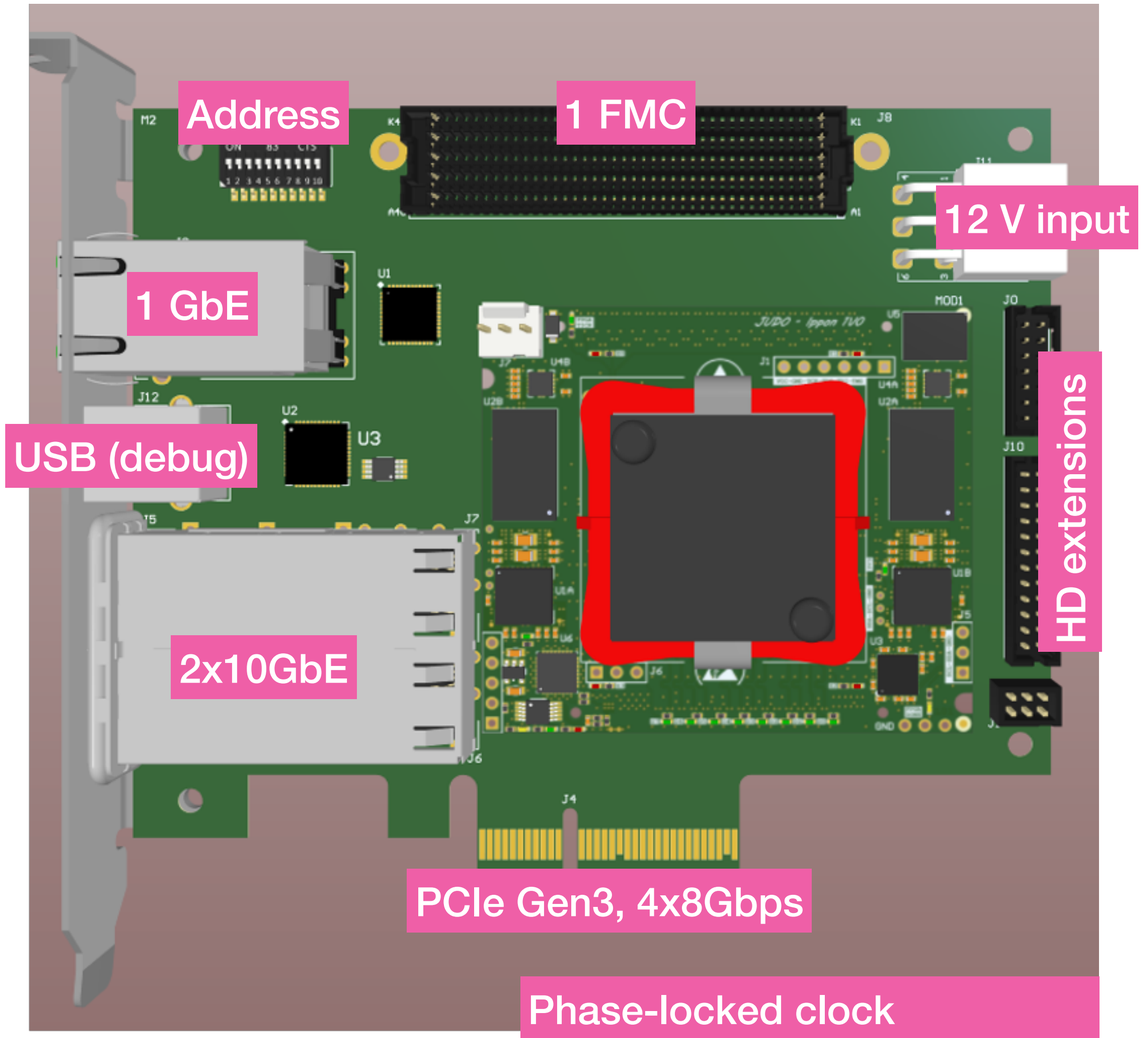
- Compatible with the CAEN backboards
  - Enable direct comparison of CAEN/H2GCROC readouts
- KCU for readout
  - We had it on hand
  - Now it is quite expensive, about 8000$
  - Only 4 chips/FPGA because of the space, not because of the FPGA

This is now obsolete, it will not work with the CALOROC chips

Test with the LpGBT



Generic RDO (gRDO)

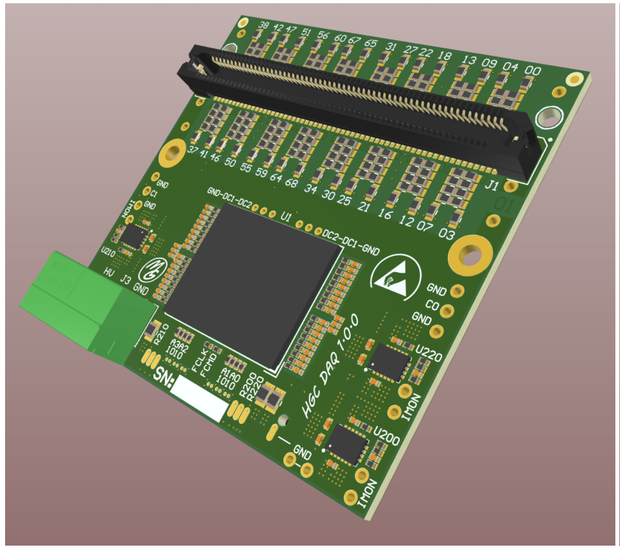


Generic RDO board:

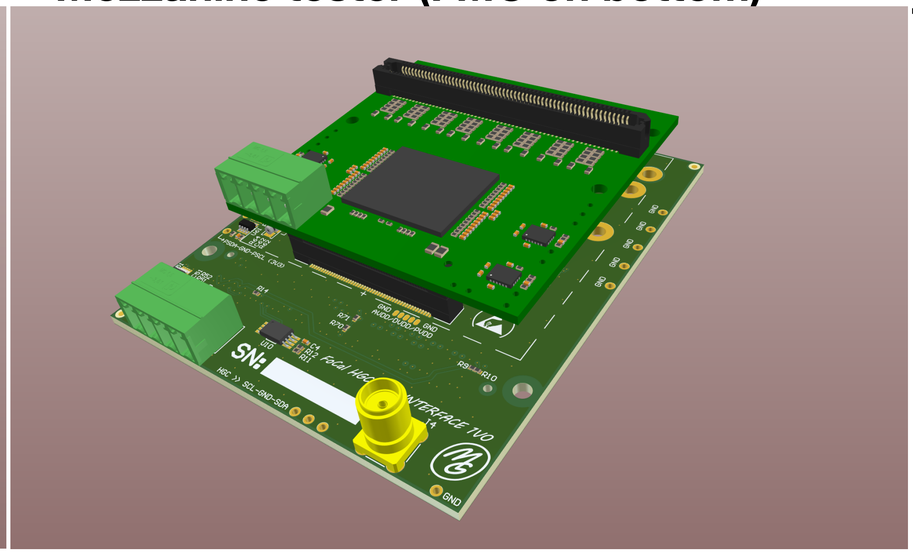
- Mezzanine for the FPGA is prepared. Only input is 12V power and the rest is on the board
  - Two types with different memory unit. Large memory might be needed for the aggregation work
- Baseboard needs some extra work
  - This is for basic testing, can be changed further
- In-limbo since last year, but it could be produced in 2 weeks

New H2GCROC/CALOROC readout board

H2GCROC mezzanine



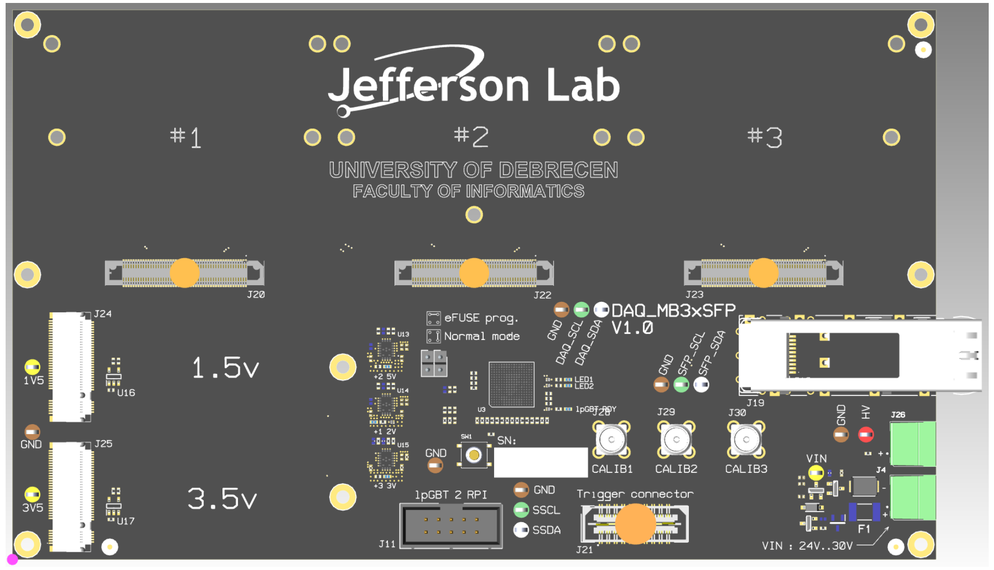
Mezzanine tester (FMC on bottom)



The mezzanine:

- 10 H2GCROC3D mezzanines will be produced
- One mezzanine == 64 channels
- Once CALOROC is available:
  - Make mezzanines with CALOROC
- Mezzanine Tester:
  - Connect to an FPGA FMC connector (e.g. KCU105, RDO, etc)
  - Individually testable setup
  - Can be used for small setup as is
    - LED tester for example

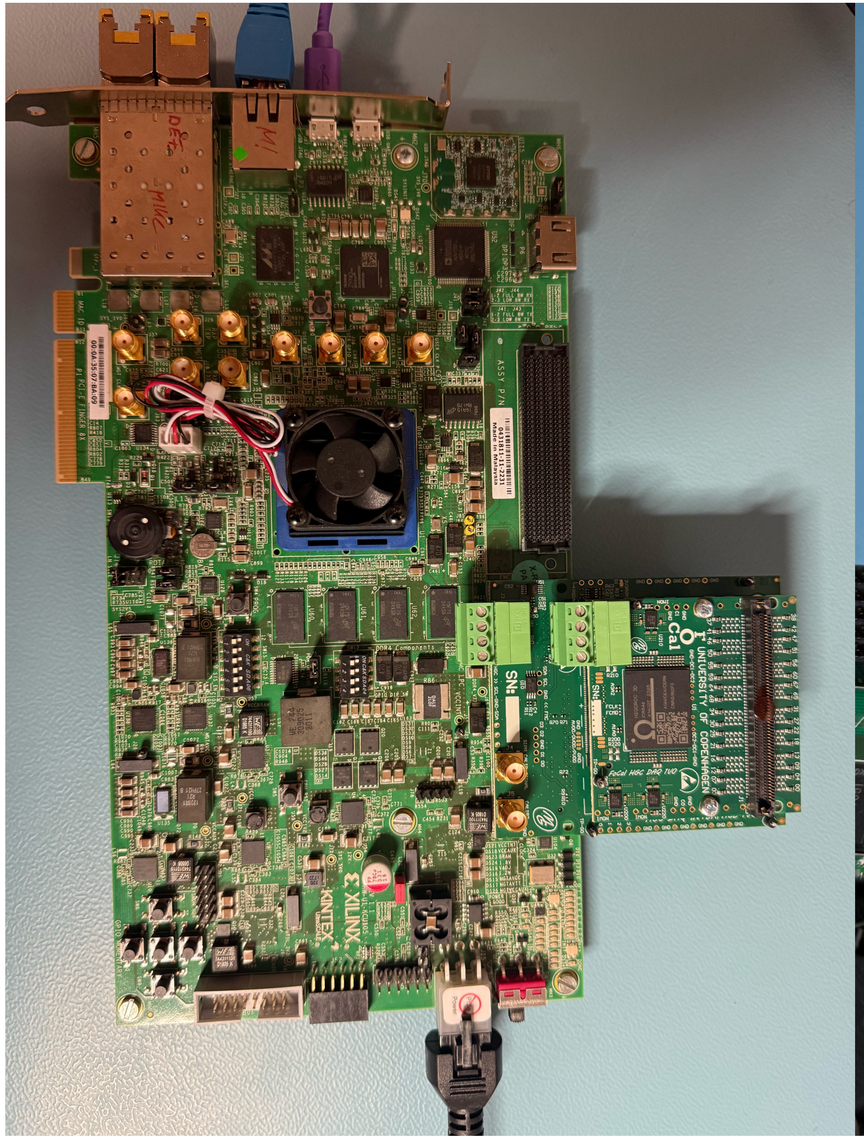
Baseboard for 3 mezzanines



Step forward:

- Can take 3 mezzanines:
  - Does not matter H2GCROC or CALOROC mezzanine
  - Both has 2x1.28 Gbps data lines
- First test article for all FEB
  - 1 LpGBT can take 3 ROCs
  - 1 SFP+ —> 10 Gbps output
  - 2 DC/DC bPOL48 converters
  - All radiation tolerant (SPF+?)

It is here


XILINX
KINTEX

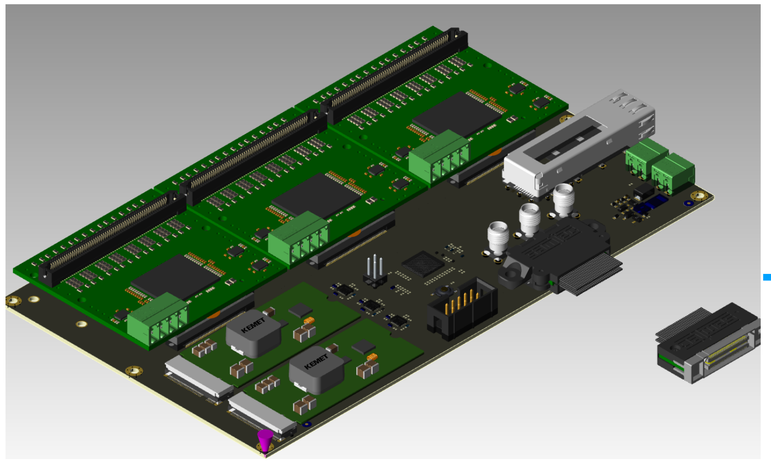

UNIVERSITY OF COPENHAGEN
HGC DAQ INTERFACE TVD
SN:
0431811-11-2231
Made in Malaysia
HGC >> SCL-GND-SDA
FMC LPC
VCCINT

Integration to the full readout chain

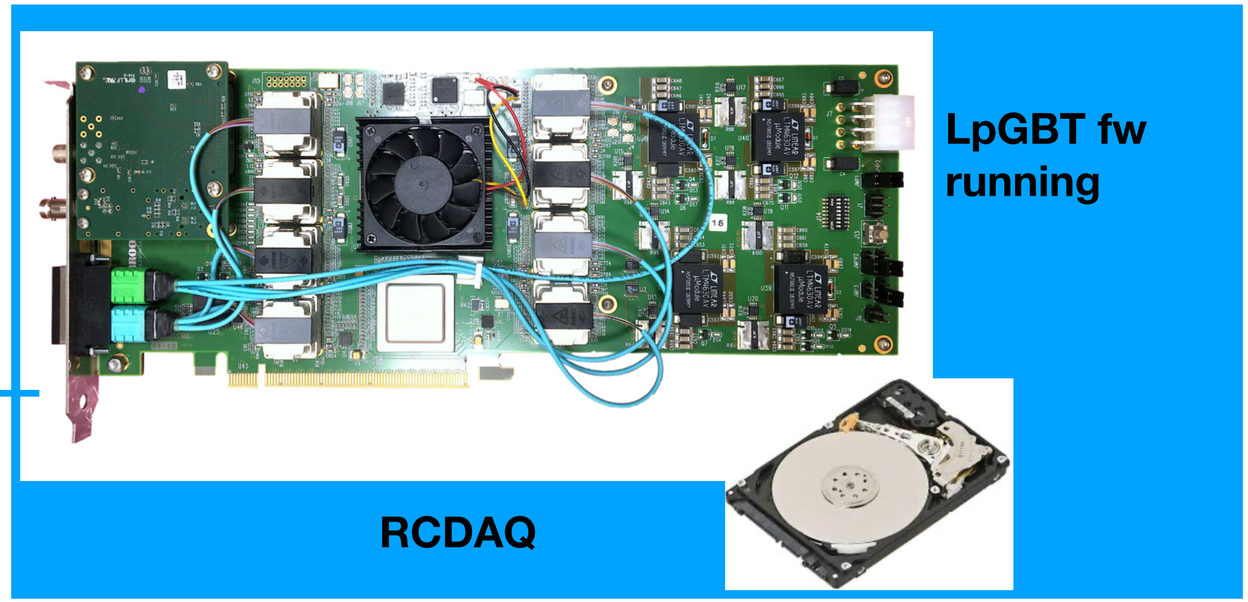
Setup a full readout chain:

- FEB's —> gRDO —> DAM boards
  - Here we can use the existing FELIX-712
  - H2GCROC board is in production - easy to change to CALOROC once the chip is available
  - Large scale tests and firmware development is needed

Step 1 - direct connection



10Gbps fiber



Integration to the full readout chain

Setup a full readout chain:

- FEB's —> gRDO —> DAM boards
  - Here we can use the existing FELIX-712
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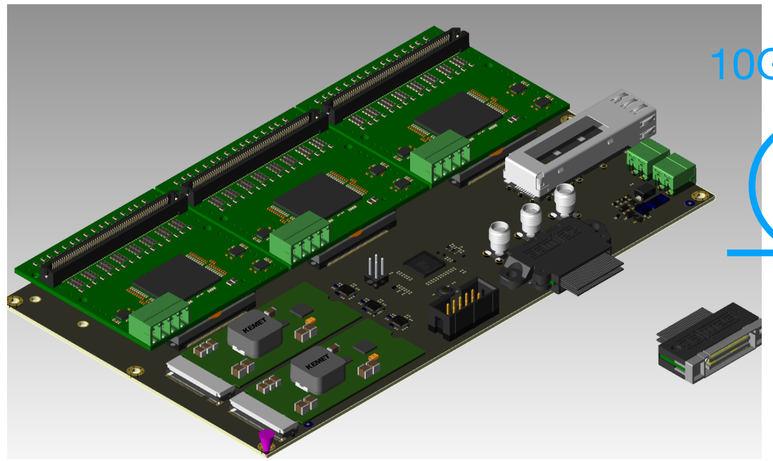
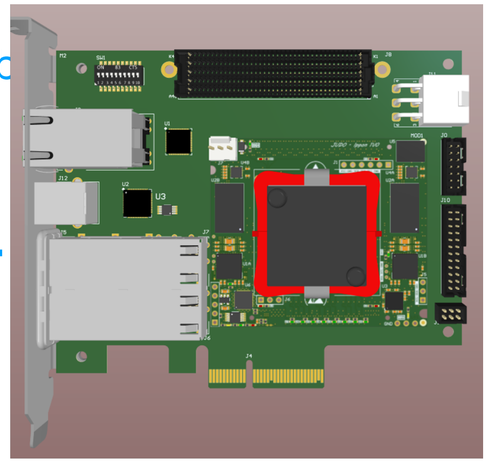
  - Large scale tests and firmware development is needed

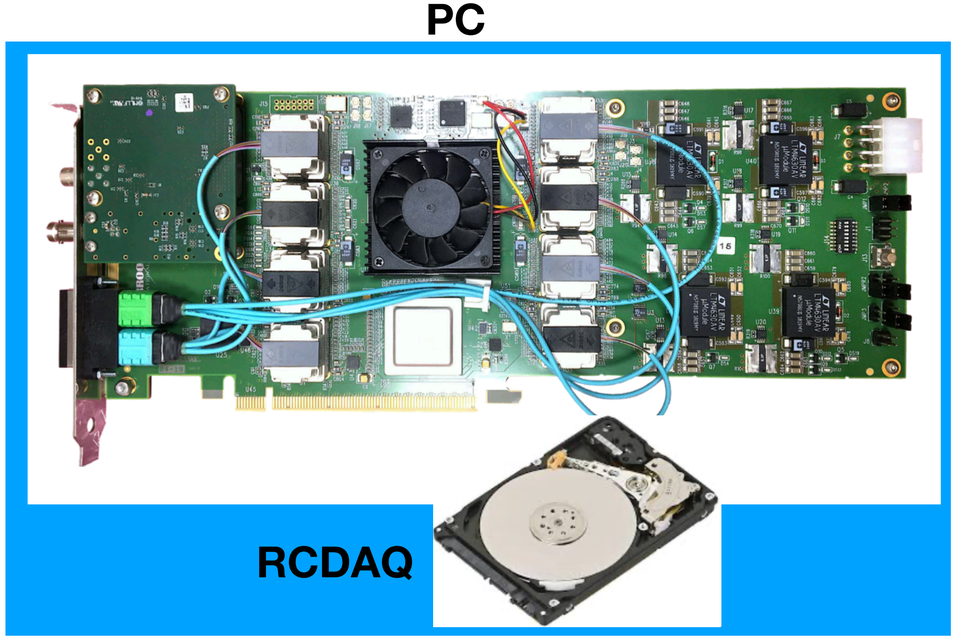
Step 2 - full chain test

Investigate the aggregation ratio (4:1)



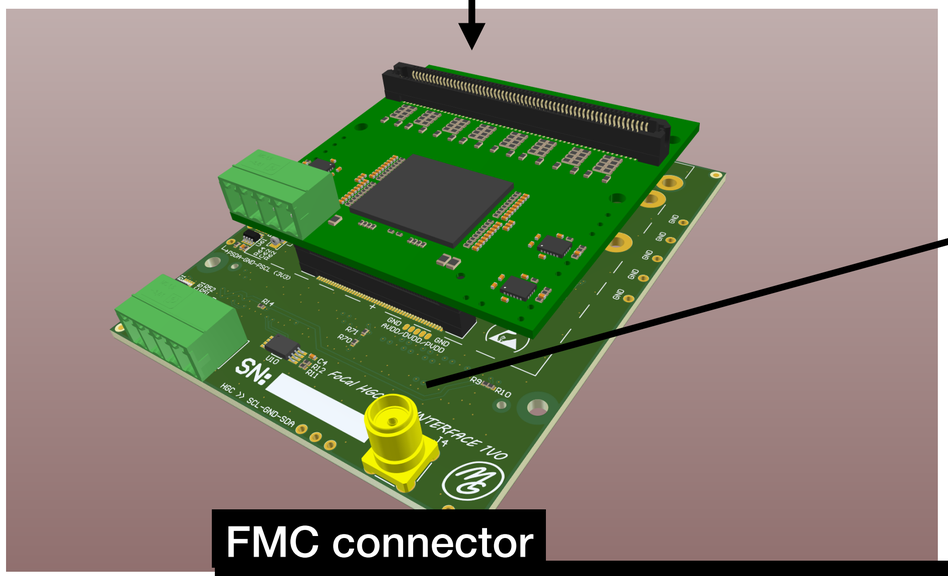
10Gbps fib





LED testing setup

Specifically for BHCal



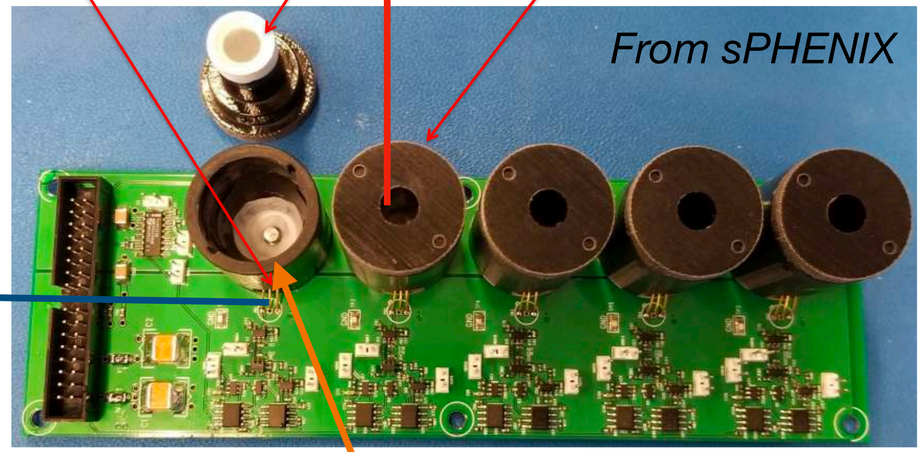
SiPM

Signal response

Light to the tile via fiber

Light to tile

Tile

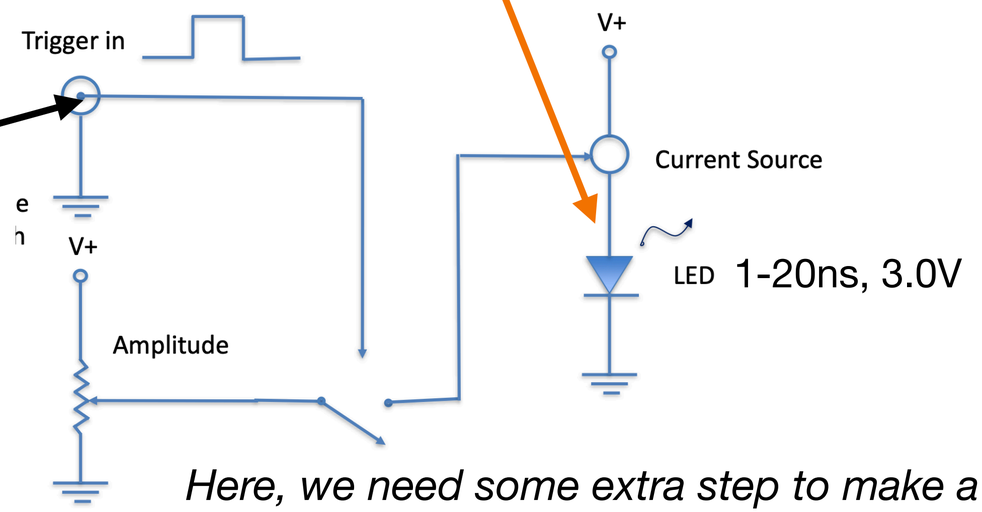


Light from the pin diode

Delay + attenuation

Calibration channel input

The LED for calibration



Here, we need some extra step to make a settable length (via I2C would be the best)

Quick summary

We should soon start receiving CALOROC chips:

- 7-7 from A-B probably already in March
- Total production is 150-150 chips
- Shifting priority to test A vs B usage of CALOROC in 2026

Large scale tests also are coming:

- One FELIX-712 (used in sPHENIX for example) can take 48 fibers, that's 48 CALOROC boards, ~5000 channels
- Full scale testing from ASIC—>DAQ will be the priority in 2026
- Small scale testing (single board with interface board) can be provided to groups - contact me