HGCROC Config

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        "FPGA Address": 0,
        "ASIC Address": 1
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        "Master_TDC_1   ": "37 d4 40 80 08 b0 02 00 00 80 08 b1 02 00 00 00",
        "Digital_Half_1   ": "00 00 00 00 c0 00 00 00 00 00 00 00 00 19 00 08 cc
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        "HalfWise_1   ": "00 00 00 00 00 00 00 00 00 00 00 00 00 00 c0",
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      "Master_TDC_0   ": "37 d4 40 80 08 b0 02 00 00 80 08 b1 02 00 00 00",
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