Status of FLX-155

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On behalf of BNL FELIX team

ePIC Collaboration Meeting

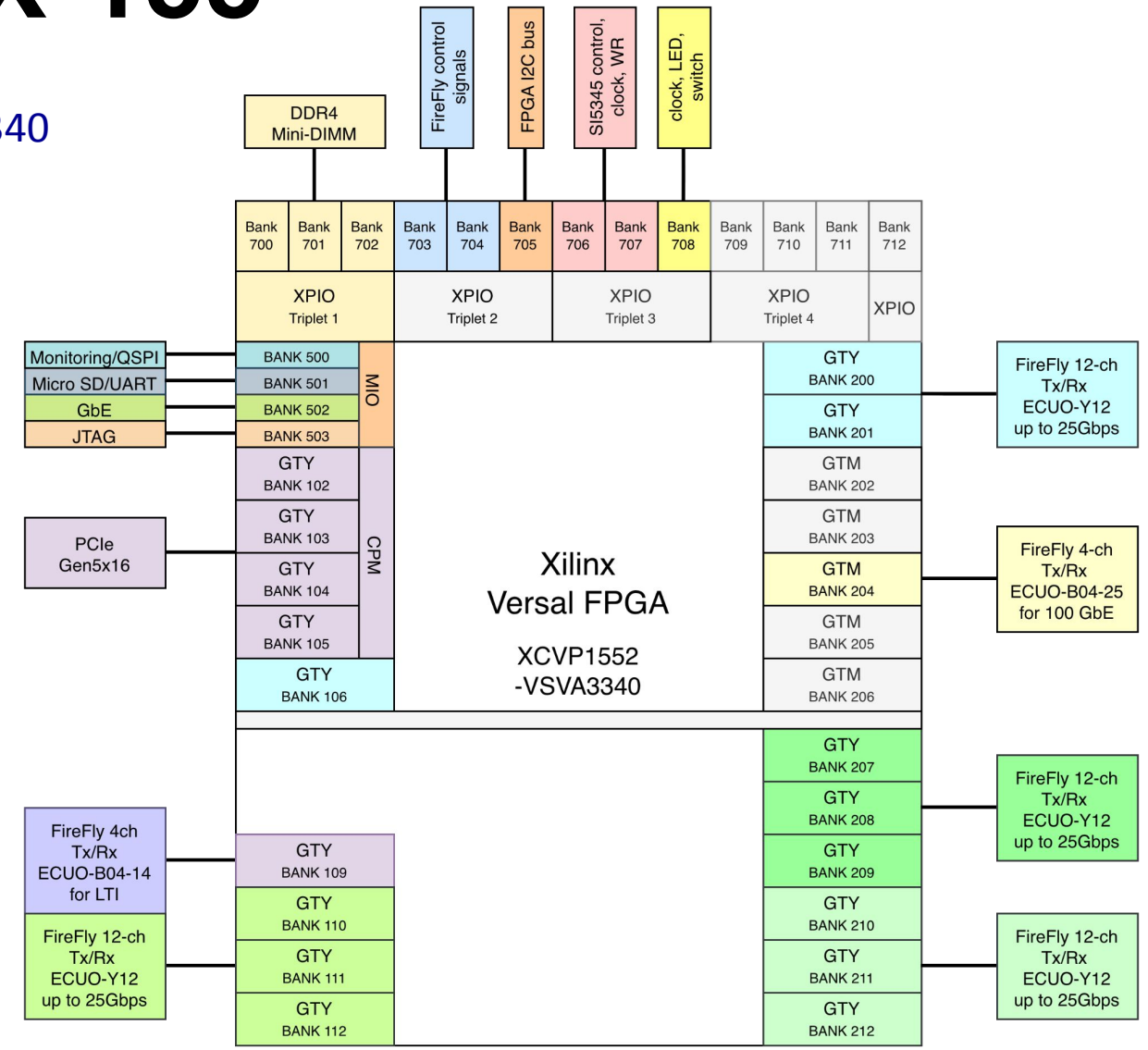
January 21, 2026

Outline

- FLX-155A: Revision of FLX-155
- Test Results of FLX-155A
- Summary

Main Features of FLX-155

- AMD Versal Premium FPGA: XCVP1552-2MSEVSVA3340
- PCIe Gen4 x16 / PCIe Gen5 2x8
- 56 FireFly optical links
  - 48 GTYP:4*12 Y12 FF; 4 GTYP:B04 FF, 4 GTM:B04 FF
  - Compatible with various options
  - Default configuration for ATLAS
    - 48 data links up to 25 Gb/s
    - 4 links for LTI
  - 4 links up to 25 Gb/s for data or 100GbE
- Electrical IOs
- 1 DDR4 Mini-UDIMM
- USB-C JTAG/UART/I2C
- SD3.0/QSPI
- GbE



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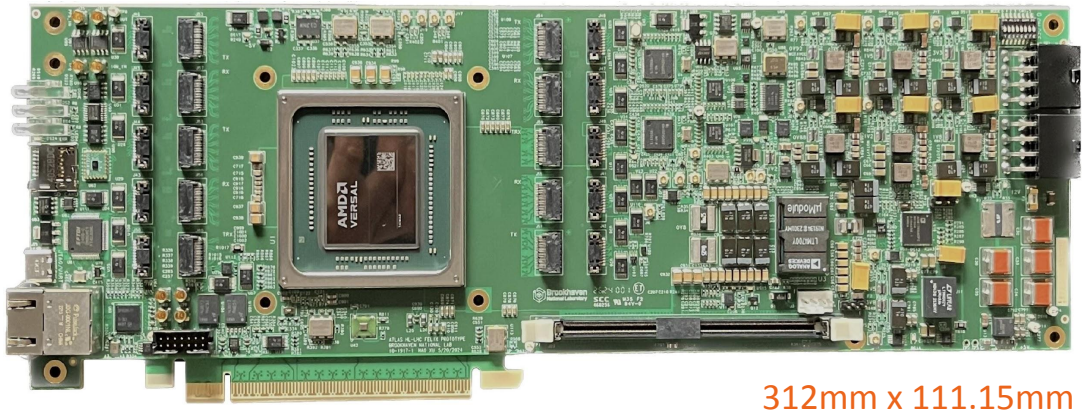
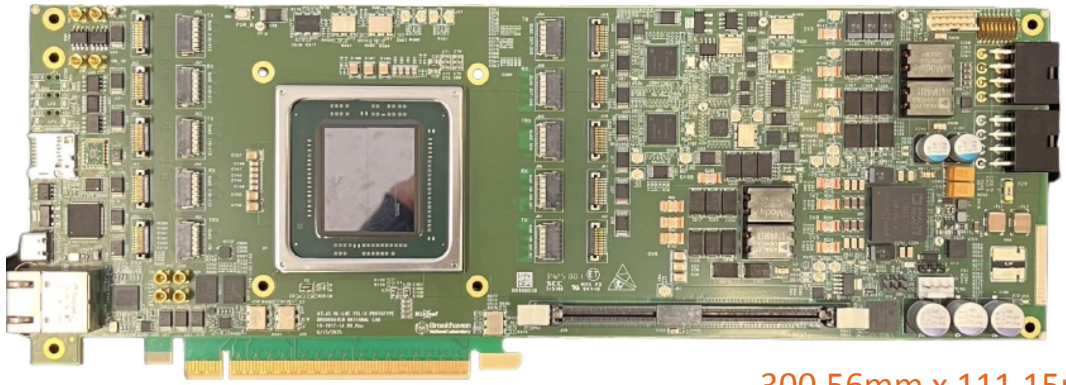
FLX-155 Revision

- Board revision
  - Board size: board length reduced by ~11.5mm, to fit some candidate servers
  - Stack-up: increased from 24 layers to 28 layers for routing and large current power rails
  - Power modules: to use modules with PMBUS for monitoring and protection, and small packages to reduce the board length
  - DDR4 signals routing optimized
  - GTYP/GTM signals routing optimized
- Status update
  - PCB received on Oct. 21
  - First assembled board delivered on Nov. 18



312mm x 111.15mm

Picture of assembled FLX-155



300.56mm x 111.15mm

Picture of assembled FLX-155A

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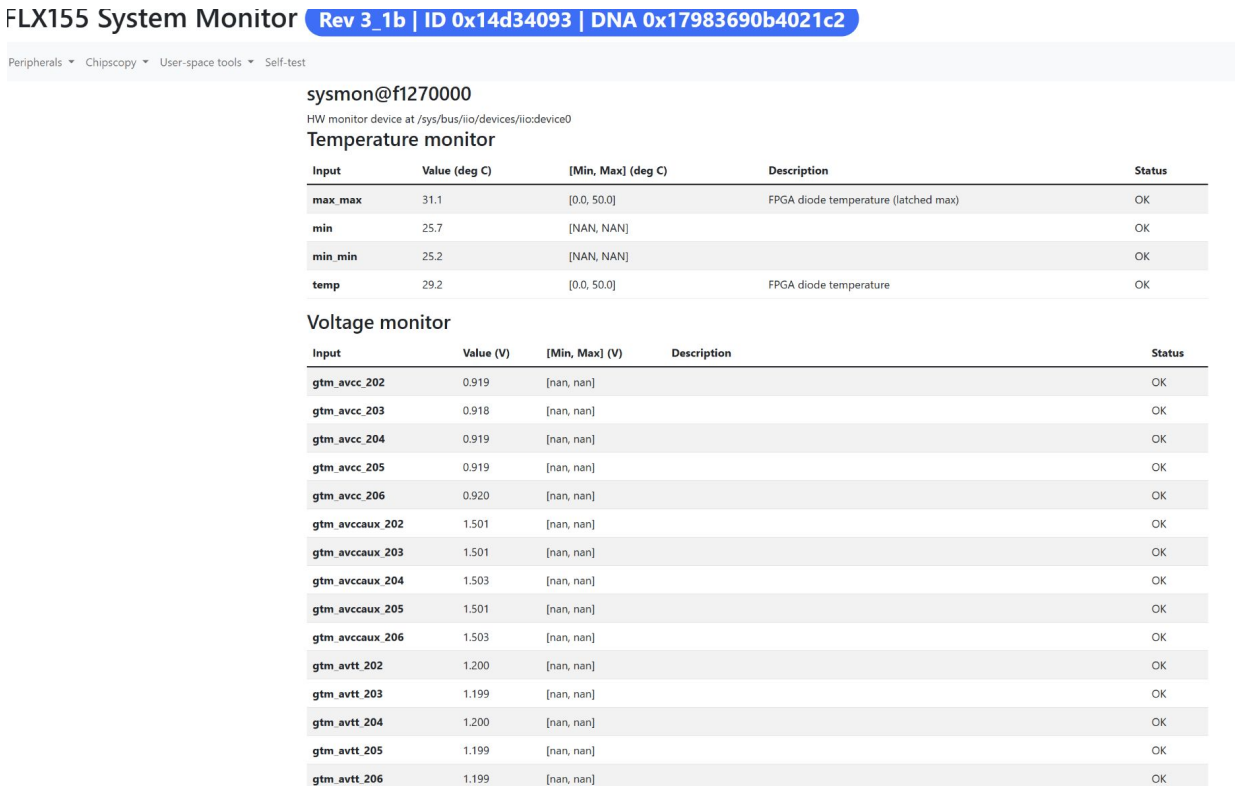
Board Bring-Up

- 2 LTM4681 and 1 LTM4673 with PMBus are used for intelligent management and high integration to save space
- ADM1266 PDIO pins are used to control the enable signals on power modules. Those pins default to a 20 kΩ pull-down resistor at power-up. Thus, there's no pull-down resistor on enable signal on FLX-155A
- The internal pull-down works for all power modules we used except LTM4673. Outputs of LTM4673 will be on during power-up, before ADM1266 sequence gets started
- Change LTM4673 configuration to use 'control is active low', and change ADM1266 to set associated PDIOs 'enable as low' as well
- Pull-down resistors will be added to enable signals on final minor revision

FPGA Boot

- FPGA can be programmed in multiple ways
  - JTAG from USB-C connector on the front panel
  - QSPI
  - SD card
- PetaLinux could boot and run properly
- BIST (not full functions) can also run correctly


FLX155 System Monitor Rev 3_1b | ID 0x14d34093 | DNA 0x17983690b4021c2

Peripherals Chipscopy User-space tools Self-test

sysmon@f1270000

HW monitor device at /sys/bus/iio/devices/iio:device0

Temperature monitor

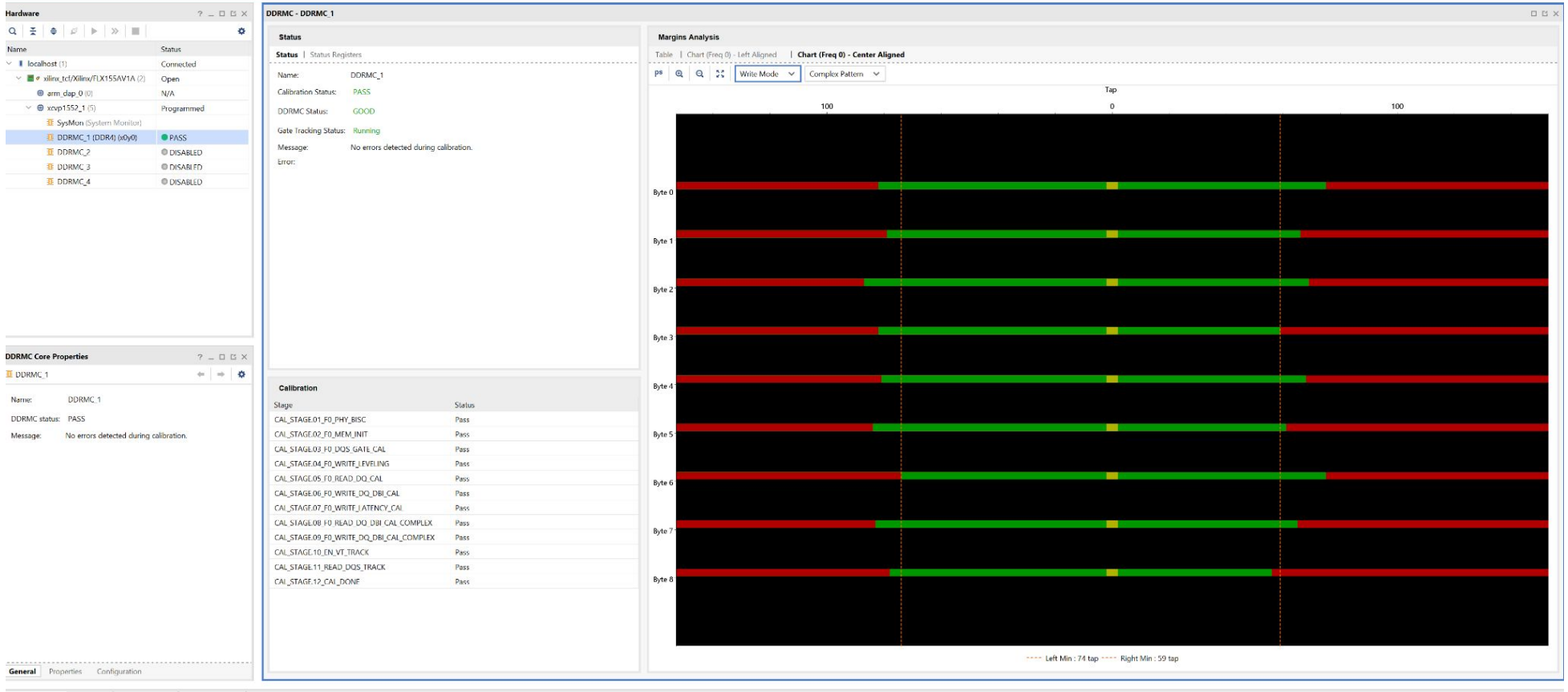
Input	Value (deg C)	[Min, Max] (deg C)	Description	Status
max_max	31.1	[0.0, 50.0]	FPGA diode temperature (latched max)	OK
min	25.7	[NAN, NAN]		OK
min_min	25.2	[NAN, NAN]		OK
temp	29.2	[0.0, 50.0]	FPGA diode temperature	OK

Voltage monitor

Input	Value (V)	[Min, Max] (V)	Description	Status
gtm_avcc_202	0.919	[nan, nan]		OK
gtm_avcc_203	0.918	[nan, nan]		OK
gtm_avcc_204	0.919	[nan, nan]		OK
gtm_avcc_205	0.919	[nan, nan]		OK
gtm_avcc_206	0.920	[nan, nan]		OK
gtm_avccaux_202	1.501	[nan, nan]		OK
gtm_avccaux_203	1.501	[nan, nan]		OK
gtm_avccaux_204	1.503	[nan, nan]		OK
gtm_avccaux_205	1.501	[nan, nan]		OK
gtm_avccaux_206	1.503	[nan, nan]		OK
gtm_avtt_202	1.200	[nan, nan]		OK
gtm_avtt_203	1.199	[nan, nan]		OK
gtm_avtt_204	1.200	[nan, nan]		OK
gtm_avtt_205	1.199	[nan, nan]		OK
gtm_avtt_206	1.199	[nan, nan]		OK

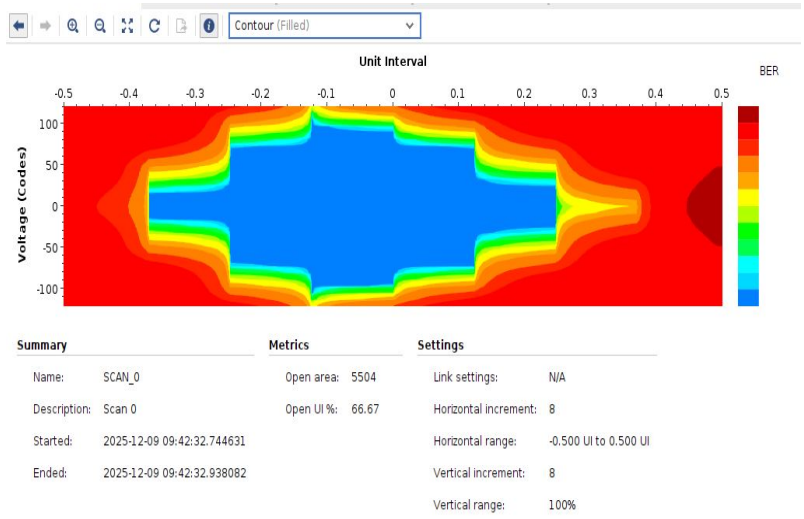
DDR4

- DDR4 layout optimized
- Passed DDRMC calibration test and used for PetaLinux
- The complex width of the data window (margin) is normal

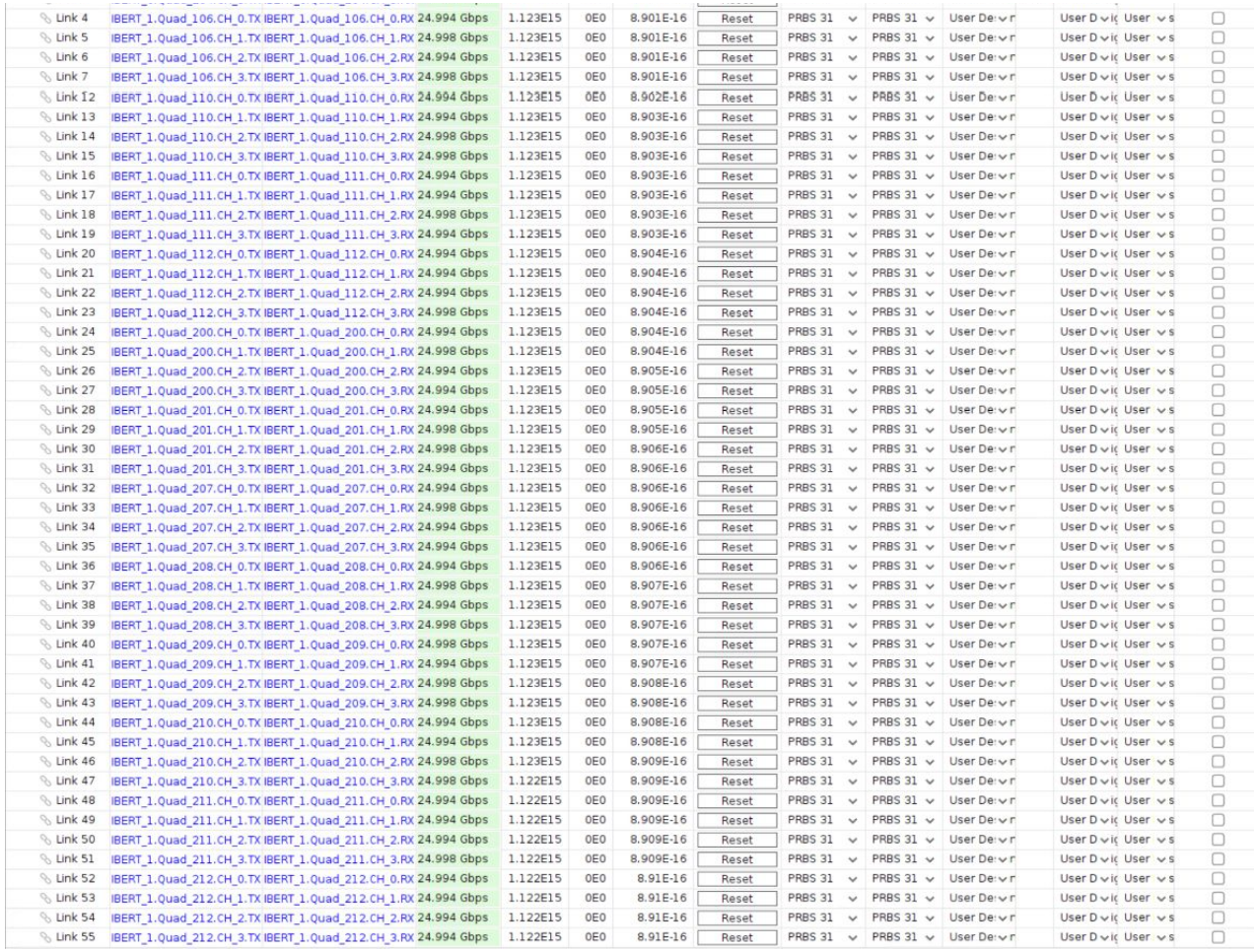


IBERT – GTYP for 48-ch Data

- Tested with 25G FireFly modules
  - 25Gbps, no error was observed during the test, BER < 10^-15
  - 10Gbps, no error was observed during the test, BER < 10^-15



Scan @ 25Gbps



IBERT @ 25Gbps

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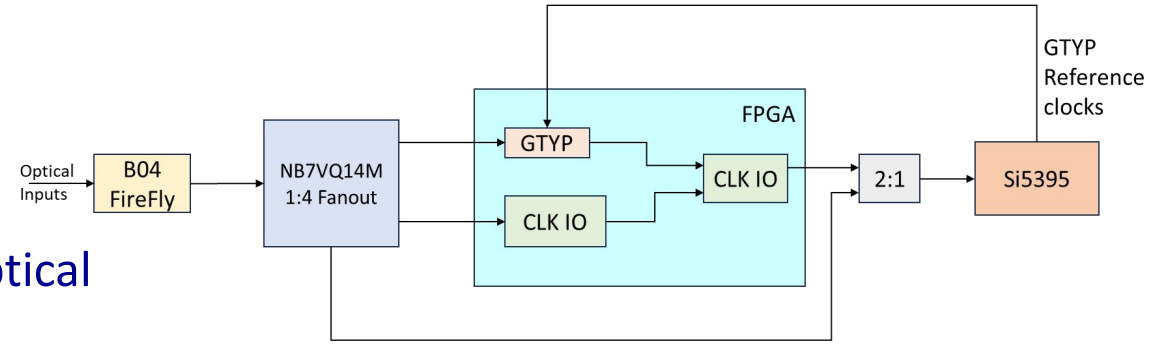
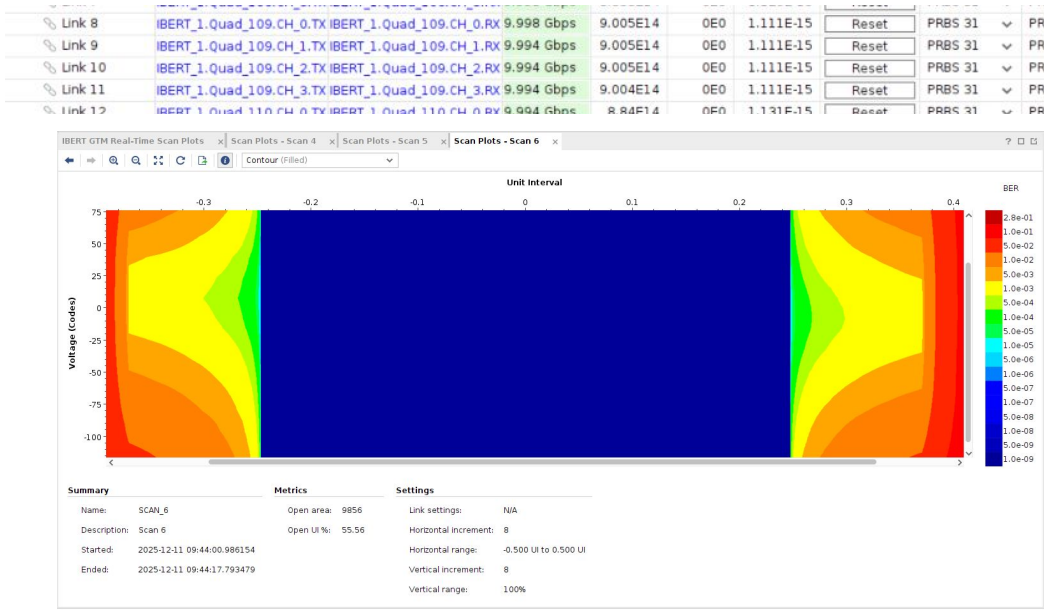
IBERT – GTYP for LTI

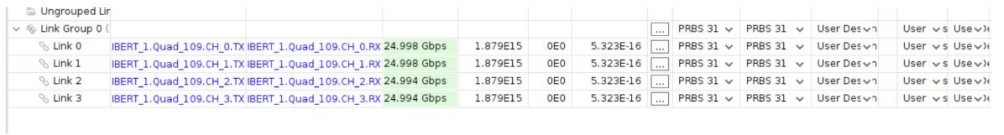
- Either recovered clock from TTC link, or clock from optical link directly
  - Recovered clock from TTC link
  - Connected to GTYP to get recovered clock as system clock
  - 4 TTC links on one B04
- Optional optical clock
  - To use the optical clock as system clock directly, clock buffer NB7VQ14M is added to one RX link, to fan out the optical input link to GTYP and FPGA clock input
  - NB7VQ14M supports up to 14Gb/s
- IBERT
  - For the links connected to GTYP directly
    - No error was observed during both 25Gb/s and 10Gb/s test
  - For the link connected to NB7VQ14M
    - 10Gb/s: BER ~10^-15, no error was observed during test
    - Bypass NB7VQ14M with jumper resistors, no error was observed during test, BER ~10^-15



Block diagram of TTC link scheme



IBERT with NB7VQ14M @10Gbps



IBERT @25Gb/s bypass NB7VQ14M

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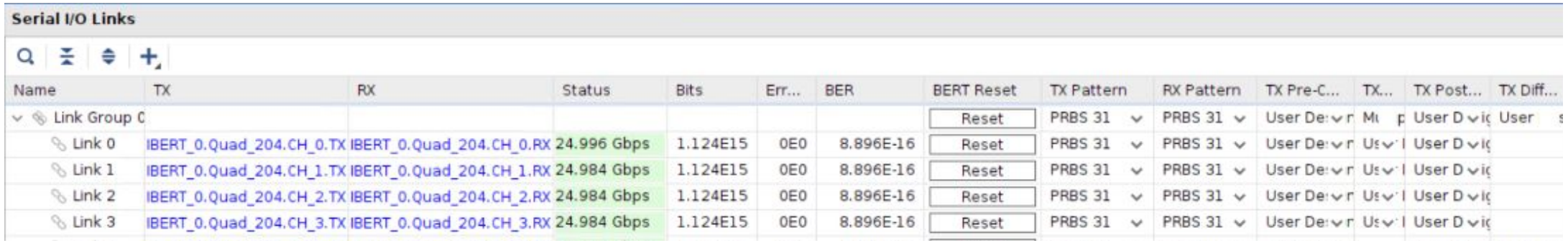
IBERT - GTM

- 4 GTM channels
  - 4 GTM channels with FireFly B04 module have been tested with 25Gb/s
  - No error was observed during test, BER < 10^-15



PCIe Performance

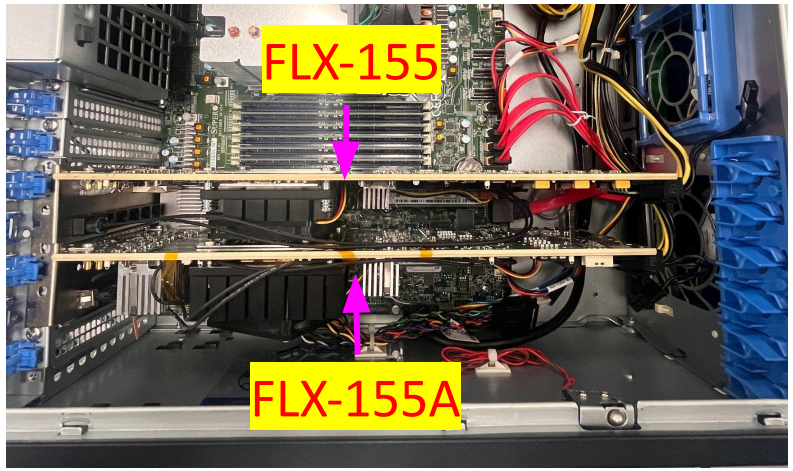
- Tested PCIe Gen5 2 x8 endpoints, bifurcated
- 512-byte TLP size
- Theoretical payload bandwidth: 240.94 Gb/s for each endpoint
- 2 Wupper endpoints, 2*27.457 GB/s (2*219.7 Gb/s), 91.2% theoretical maximum speed

```
[felix@130-199-21-187 bin]$ ./fdaqm -C 2 -t 10
Consume FLX-device data while checking the data (blockheader and trailers)
Also counts chunk CRC errors.
Opened FLX-device 0, FLX155-GBT-2x24CH-241016-1747-GIT:rm-5.2/101, trailer=32bit ChunkHeaders, buffer=1024MB, DMA=0
Opened FLX-device 1, FLX155-GBT-2x24CH-241016-1747-GIT:rm-5.2/101, trailer=32bit ChunkHeaders, buffer=1024MB, DMA=0
**START**
** using DMA #0 polling
  Secs | d-D | Recvd[MB/s] | File[MB/s] | Total[(M)B] | Rec[(M)B] | Buf[%] | Wraps
-------|-----|-------------|------------|-------------|-----------|--------|-------
     1   0-0       28968.5          0.0       28968.5           0       41      26
   ### @Dev-DMA=0-0 Blocks 27898757 Errors: header=27898757 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     1   1-0       27691.9          0.0       27691.9           0       11      25
   ### @Dev-DMA=1-0 Blocks 26958942 Errors: header=26958942 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     2   0-0       27457.2          0.0       56425.7           0        4      52
   ### @Dev-DMA=0-0 Blocks 55103261 Errors: header=55103261 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     2   1-0       27457.6          0.0       55149.5           0       19      51
   ### @Dev-DMA=1-0 Blocks 53689436 Errors: header=53689436 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     3   0-0       27038.8          0.0       83464.6           0       45      77
   ### @Dev-DMA=0-0 Blocks 81090110 Errors: header=81090110 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     3   1-0       27038.4          0.0       82187.9           0       49      76
   ### @Dev-DMA=1-0 Blocks 79787592 Errors: header=79787592 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     4   0-0       27619.5          0.0      111084.1           0        5     103
   ### @Dev-DMA=0-0 Blocks 108480539 Errors: header=108480539 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     4   1-0       27624.1          0.0      109811.9           0       25     102
   ### @Dev-DMA=1-0 Blocks 107015429 Errors: header=107015429 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     5   0-0       27114.8          0.0      138198.9           0       44     128
   ### @Dev-DMA=0-0 Blocks 134541694 Errors: header=134541694 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     5   1-0       27113.8          0.0      136925.7           0       22     127
   ### @Dev-DMA=1-0 Blocks 133521131 Errors: header=133521131 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     6   0-0       27950.7          0.0      166149.6           0        5     154
   ### @Dev-DMA=0-0 Blocks 162255488 Errors: header=162255488 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     6   1-0       27955.1          0.0      164880.8           0       12     153
   ### @Dev-DMA=1-0 Blocks 160932702 Errors: header=160932702 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     7   0-0       27751.4          0.0      193901.0           0       14     180
   ### @Dev-DMA=0-0 Blocks 189245365 Errors: header=189245365 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     7   1-0       27724.4          0.0      192605.2           0       12     179
   ### @Dev-DMA=1-0 Blocks 188007286 Errors: header=188007286 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     8   0-0       27344.0          0.0      221245.0           0       26     206
   ### @Dev-DMA=0-0 Blocks 215836723 Errors: header=215836723 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     8   1-0       27374.2          0.0      219979.5           0       65     204
   ### @Dev-DMA=1-0 Blocks 214182208 Errors: header=214641266 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     9   0-0       27351.0          0.0      248596.1           0       55     231
   ### @Dev-DMA=0-0 Blocks 242239735 Errors: header=242315401 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     9   1-0       27350.4          0.0      247329.8           0       22     230
   ### @Dev-DMA=1-0 Blocks 241338341 Errors: header=241338341 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
    10   0-0       28304.1          0.0      276900.2           0       63     257
   ### @Dev-DMA=0-0 Blocks 269796552 Errors: header=270147127 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
    10   1-0       28280.2          0.0      275610.0           0       47     256
   ### @Dev-DMA=1-0 Blocks 268704255 Errors: header=268704255 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
**STOP**
-> Data checked @Dev-DMA=0-0: Blocks 269796552, Errors: header=270149523 trailer=0
First block with error, index 0, chunk data:
==> BLOCK ###INVALID HEADER (FF FF FF FF) 0 bytes payload
 ## (255x)

-> Data checked @Dev-DMA=1-0: Blocks 268704255, Errors: header=268704255 trailer=0
First block with error, index 0, chunk data:
==> BLOCK ###INVALID HEADER (FF FF FF FF) 0 bytes payload
 ## (255x)
```

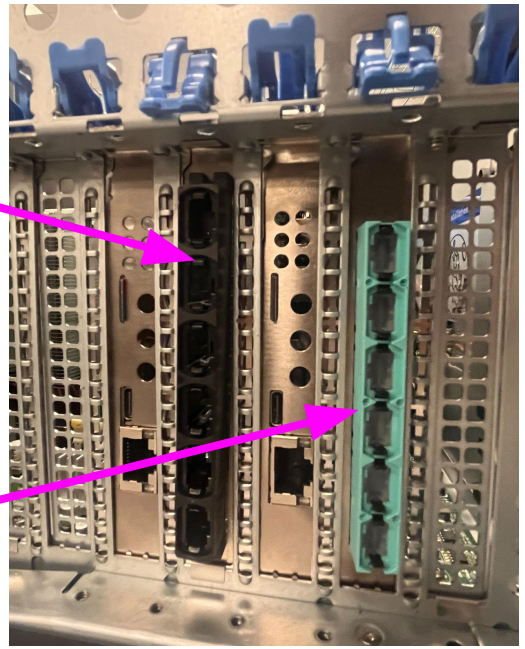
Mechanical Update

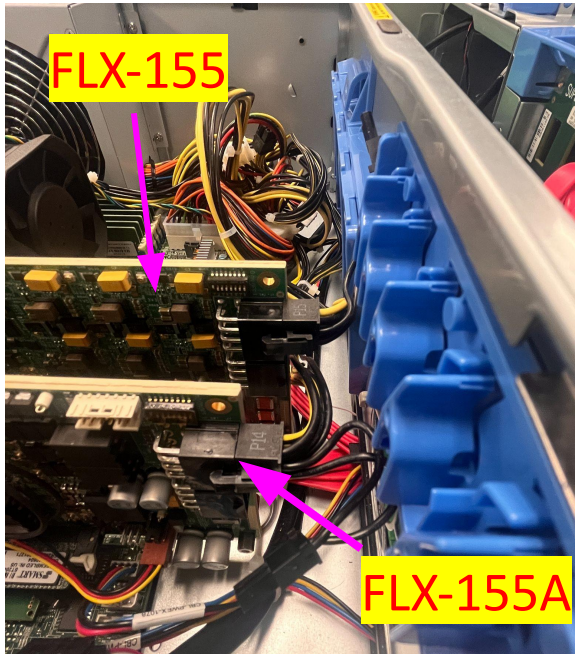
- The board length reduced by ~11.5mm
- A 1x6 snap-in MTP adapter without ear is used
- Two changes make it to be easily installed into the server and plug the power cable into the power connector



1x6 MTP adapter
w/ flange
86.6x9.8 mm

1x6 MTP adapter
w/o flange
77.7x9.75 mm





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FELIX Schedule

- January 2026, 4 more FLX-155A cards are being assembled
- Spring 2026, ATLAS FDR
- After FDR, pre-production (FLX-155B) fabrication, assembly and testing
- Fall 2026, ATLAS PRR
- After PRR, ATLAS production
- End of 2027, ATLAS production complete

Summary

- FLX-155A test results show all main functions work properly as expected. Power on sequence workaround on the current board has been finalized
- 4 more boards are being assembled, 1 for ePIC is expected to be delivered in February
- FELIX for ATLAS production is planned in this year