Brookhaven National Laboratory

Jefferson Lab

U.S. DEPARTMENT of ENERGY | Office of Science

ePIC DAQ Overview and Near-Term Plans

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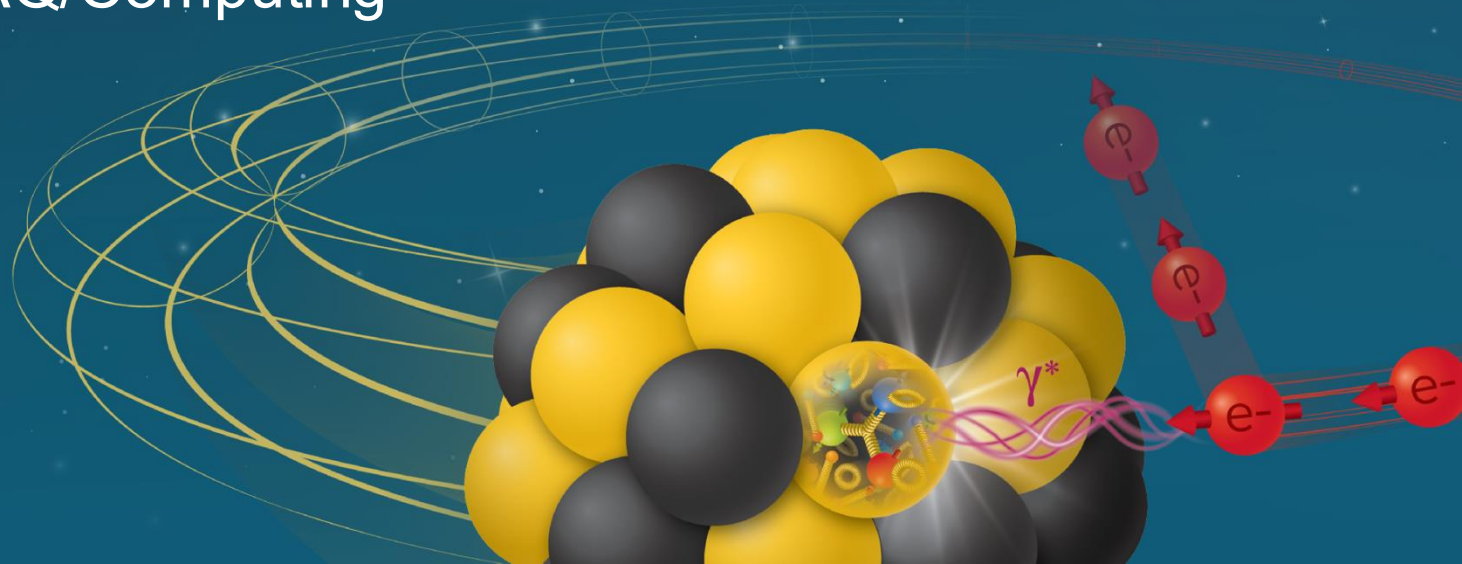
ePIC Collaboration Meeting

January 20th – 23th, 2026

Brookhaven National Lab, Upton, NY

Electron-Ion Collider



ePIC DAQ Schedule

- A functional DAQ will be necessary for small scale detector testing as well as commissioning and pre-ops.
- **Hardware and software development early in the construction phase will involve a series of releases with increasing functionality.**

Detector Install: FY30Q2 - FY33Q2
Cosmics: FY31Q
Early CD-4: FY32Q4

DAQ Releases:

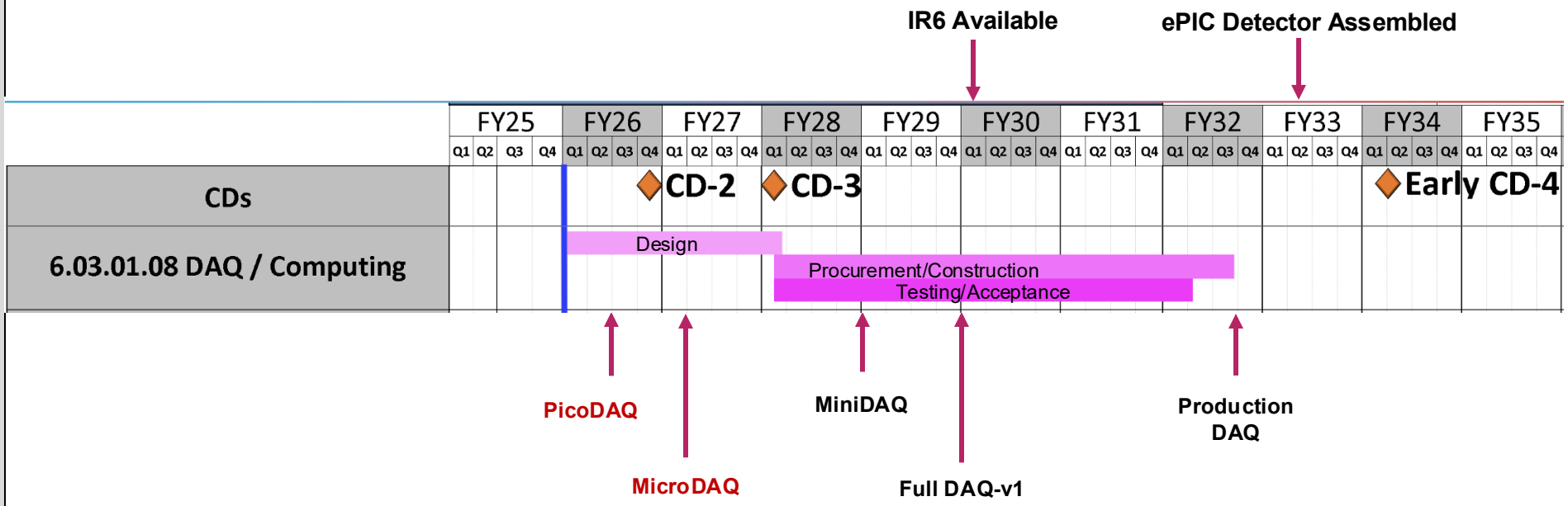
PicoDAQ FY26Q2
Readout test setups

MicroDAQ: FY27Q1
Readout detector data in test stand using engineering articles

MiniDAQ: FY29Q1
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY30Q1
Full functionality DAQ ready for full system integration & testing

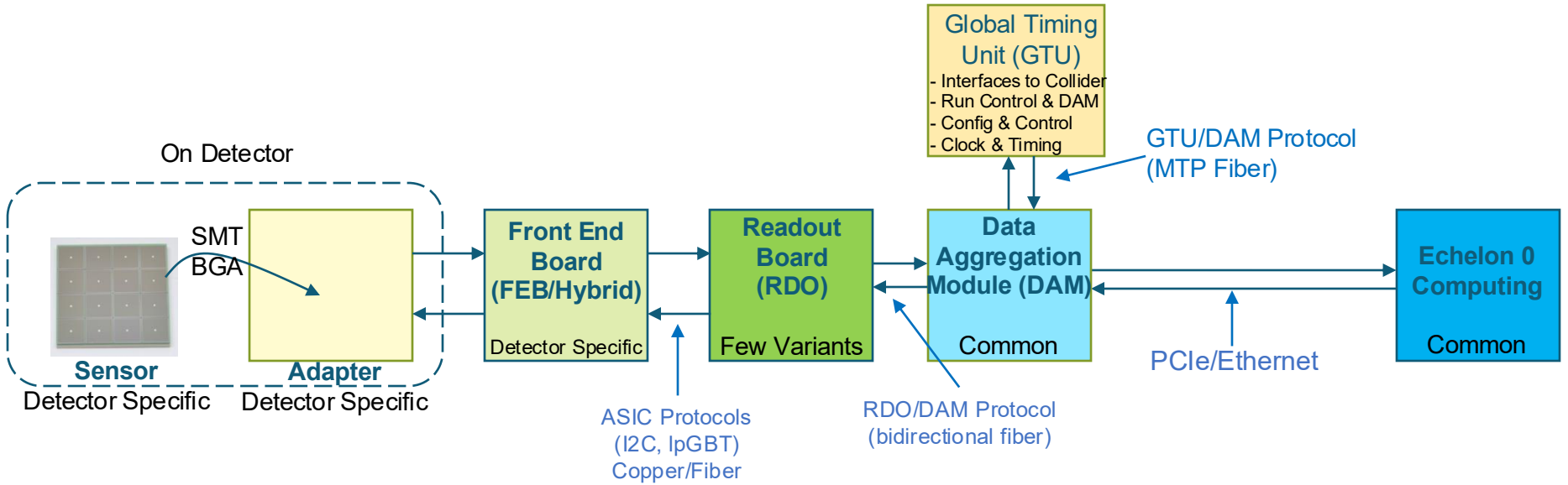
Production DAQ: FY32Q4
Ready for cosmics

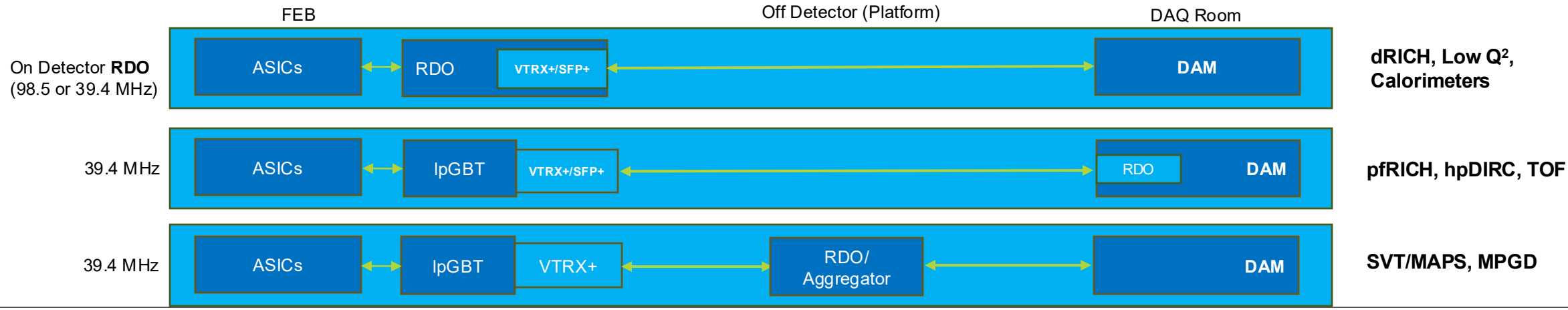


DAQ Production Planning and Timeline

- Starting in 2026 begin utilizing lab space in the BNL Physics building
  - Engineering articles for DAM and GTU hardware will begin testing
  - RDO Engineering articles need to be produced
  - Phase I computing purchase – development/evaluation machines
  - Software and firmware development for initial DAQ releases (**Pico and MicroDAQ**) and full chain testing with substitute FEBs.
- Initial DAQ Enclave implementation in the SDCC (1-2 racks, Q1 FY2027)
  - Implement networking (DAQ VLAN) between Lab test stands and development machines in SDCC
  - Begin software design/development of frame building and buffer box management.
  - Can begin to support/develop the interface to Echelon 1 computing – also support Echelon 1 data challenges
- Beneficial occupancy of Building 1006 (Q1 FY2030)
  - Requisitions of Trunk Fiber, and Phase II computing infrastructure are executed.
  - Installation of Fibers, racks, computing and network infrastructure gets underway.
  - As detector sub-systems are received and tested at BNL the **MiniDAQ** software release will allow these systems to run full chain readout and testing using actual FEB hardware.
- ePIC Detector assembly and integration begins at IP6/Assembly Hall (Q2 FY2030)
  - Development of **Full DAQ** versions progress as detector sub-systems are installed.
  - Assessment of the final Phase III of computing infrastructure procurement and requisition will be executed – most nodes being installed in the SDCC DAQ Enclave. Add racks as needed.
- Full Assembly of ePIC detector is completed (Q2 FY2033)
  - Initial release of the ePIC **Production DAQ** is released, and the fully integrated detector will begin taking cosmic data.
  - Integration of Echelon 1 computing with the Production DAQ will continue.

ePIC Readout Chain

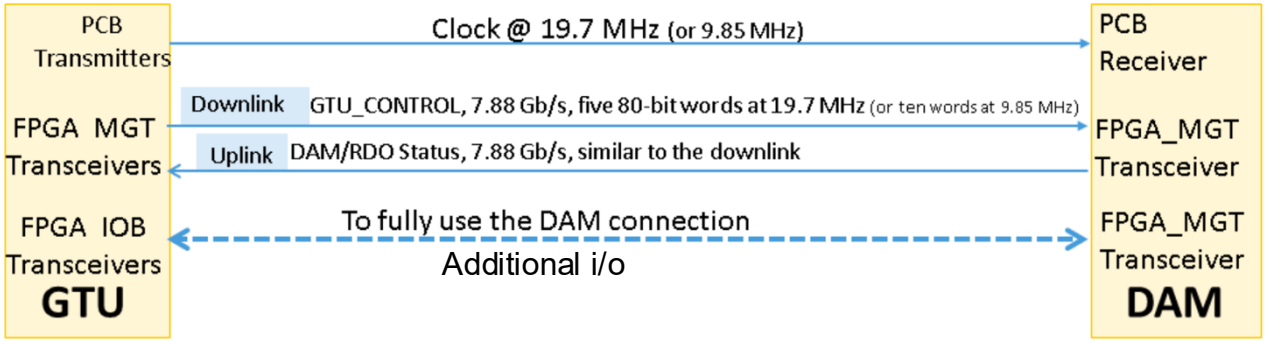


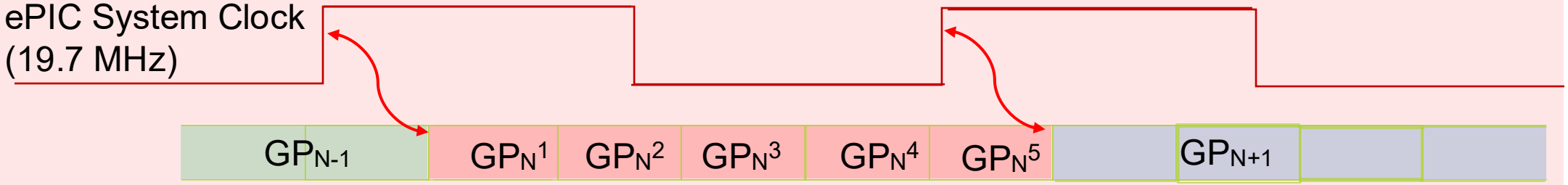


GTU/DAM Protocol

EIC Common Platform: 98.5MHz BeamCrossing (bx) clock
Orbit (RevTick) every 1260 bx

GTU must support: Both 98.5 and 39.4MHz, hence the GTU distributed synchronous system clock will be 19.7MHz → 98.5MHz/5 and 39.4MHz/2

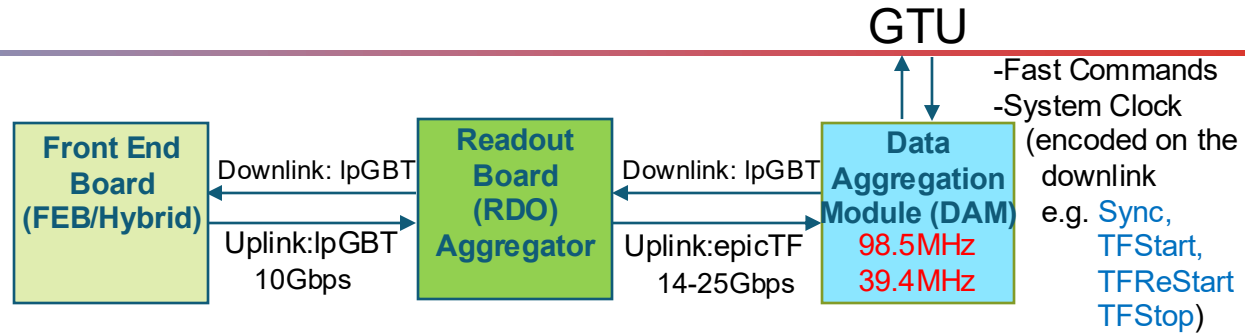




Link speed: 7.88 Gbps, 400 bits per ePIC system clock cycle ➔ 8b/10b encoding ➔ Five 64-bit Words GP_N^x

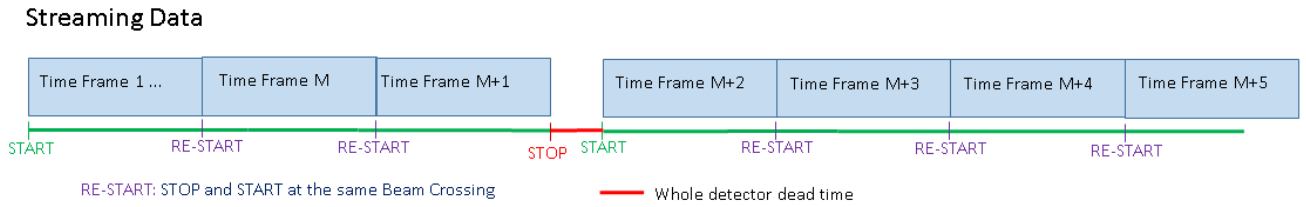
Packet	Packet GP_N (at 19.7 MHz)					
Word #	GP_N^1	GP_N^2	GP_N^3	GP_N^4	GP_N^5	Five BX Words per GTU Packet (GP)
Bit(9:0) abcdeifghj-	K28.1_3C 0011111001 x0111110xx	K28.2_5C 0011110101	K28.3_7C 0011110011	K28.4_9C 0011110010	K28.5_BC 0011111010 x0111110xx	Bit Alignment and Data ID (1 Byte)
Bit(19:10)	GTU_RC	GTU_RC	GTU_RC	GTU_RC	GTU_RC	Synchronous RC codes/Fast Commands (1 Byte)
Bit(49:20)	e.g. BX(15:0) Orbit(7:0)					Bunch Crossing Counters (3 Bytes)
Bit(79:50)	DAM/User	DAM/User	DAM/User	DAM/User	DAM/User	DAM/User specific (3 Bytes)

RDO/DAM Protocols



- ePIC TimeFrame (epicTF) Format
  - Length nominally defined by the BX Clock (10.15ns) in 16 bits (up to 665.19ms)
  - But must follow the 5:2 ratio of the two system clocks (98.5MHz and 39.4MHz)
  - Max timeframe length is then (2^{16} – 11)= 65525 BX clocks == 10484 39.4Mz clocks == 665.079ms

- Downlink Protocol: lpGBT (FULL / private)?, (FEC5, FEC12)?
  - Define single standard, or at least define which standard to use for which detector
  - List of fast commands for each ASIC needs to be specified and documented
  - Implementation of slow control (e.g. I2C) communication for ASIC configuration/control
- Uplink Protocols: (lpGBT decoding, epicTF creation/aggregation)
  - Data formats for each ASIC are mostly known but need to documented in a single place for ePIC.
  - Define header formats, specification of which components add headers and what types.
  - Specification of detailed time ordering of hits from front-end and aggregation algorithms



Early DAQ Support for ePIC

- In near term, as we are working with engineering articles for all the DAQ components (FEB,RDO,DAM,GTU), we need to create early “releases” of firmware/software that will support a subset of hardware that is generally available – both commercially and from new and existing hardware designs.

- **PicoDAQ**
  - Focused around RDO/ASIC configuration and readout.
  - This is for simple test systems supporting a single RDO (FPGA) connected to one or multiple FEBs (ASICS/Digitizers).
  - Ethernet-based configuration, control and readout support from a Linux PC or server.

- **MicroDAQ**
  - Build on PicoDAQ by adding DAM and GTU hardware support
  - Implementation of GTU<->DAM<->RDO clock distribution and communication protocol.
  - Support via DAM for time frame building of data from multiple RDOs.
  - PCIe and Ethernet readout options from the DAM.

Discussion Topics

- In addition to the ASIC developments, we have multiple groups actively working with FEB<->RDO<->DAM hardware implementations
  - dRICH readout ALCOR<->RDO<->DAM (on detector RDO)
  - Generic RDO
  - MAPS control/readout and the fiber aggregator RDO
  - Readout FEB Hybrid direct to DAM (firmware RDO)

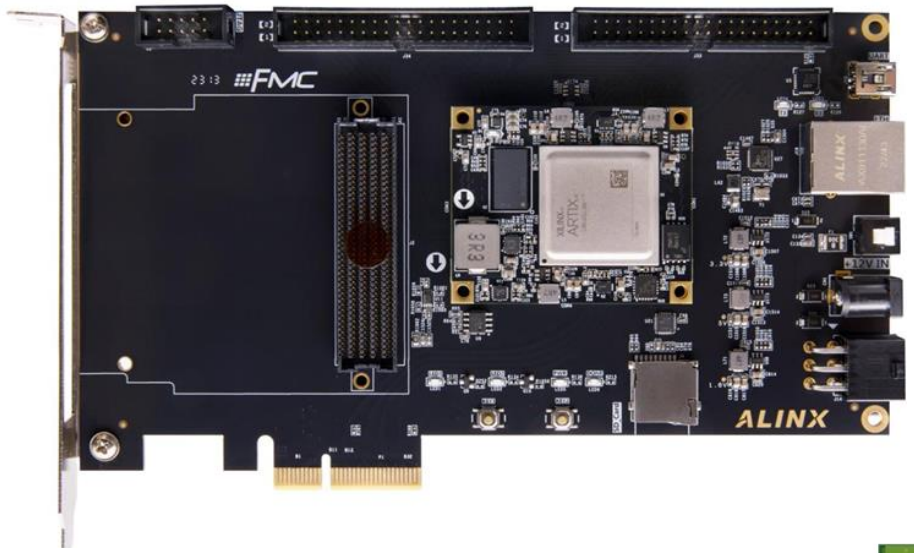
- Developments presented in this workshop should lead to defining:
  - All the ePIC DAQ link protocols including a timeframe data format
  - Core firmware/software support for both PicoDAQ and MicroDAQ
  - What RDO engineering article(s) should be produced now?

- **We need to coordinate these efforts within the active development groups**

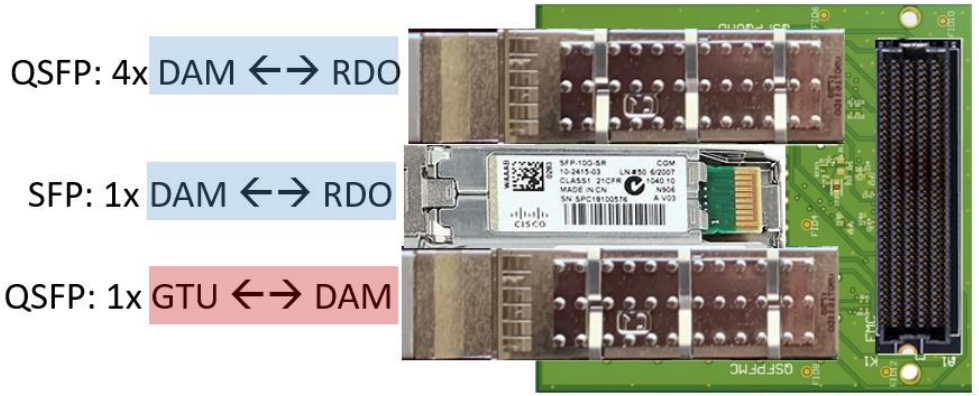
Backup

Mini-DAM/GTU Support

- Inexpensive FPGA development board can be used as an RDO interface to ASIC FEBs via the FMC connector.
- With the addition of an FMC adaptor board developed at JLAB it can be used as a “mini” DAM with readout/control support for up to 5 RDO boards.
- In addition, a clock chip on the adapter card will provide GTU services for distribution of 98.5 MHz or 39.4MHz clocks



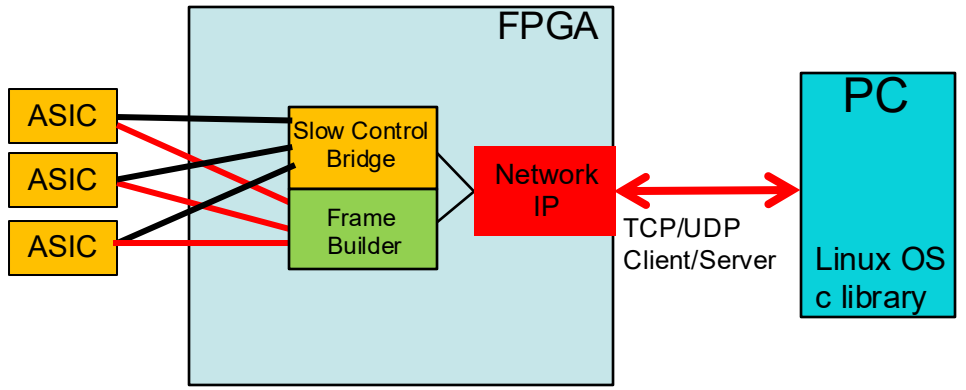
Alinx AXAU15
(Artix Ultrascale+ FPGA)
~$800

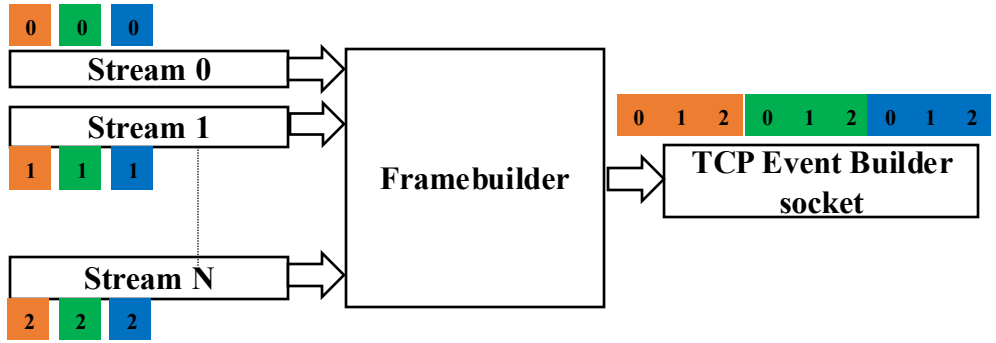


FMC DAM adapter board (JLAB Design)

Front-End readout currently supported at JLab

- TCP Socket based slow control protocol from a Linux-based PC using a 1/10Gb ethernet port
  - 32bit registers map to ASIC configuration bus.
- FPGA based block RAM used to aggregate data and build frames/events
  - Up to 32 input streams to create one ~1GB/s output stream
- Low cost commercial TCP/IP block supporting 1 or 10Gb ethernet links (Client and Server)
  - Low resource utilization
  - License will allow JLAB to distribute downloadable firmware using this IP for ePIC associated projects
- We plan to continue and expand support for this firmware/software for both existing and future projects.





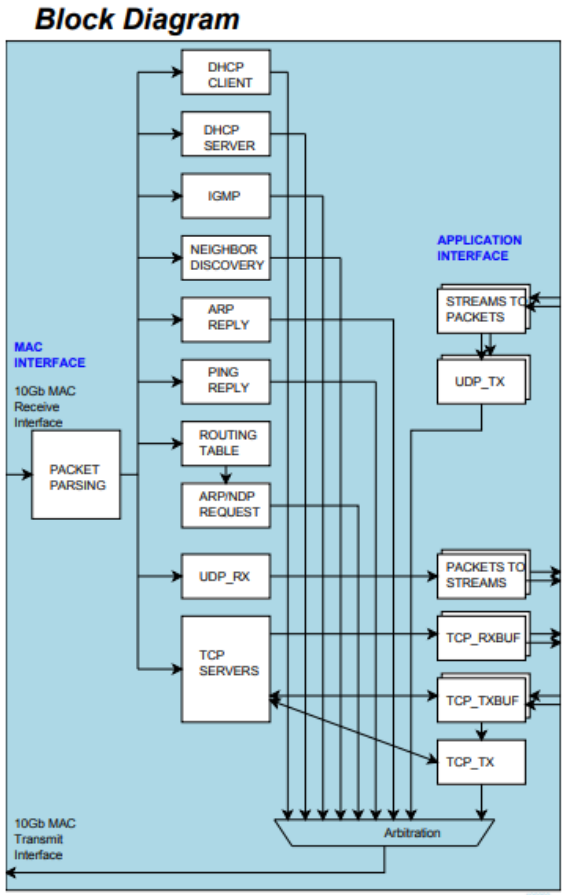
TCP/IP IP Blocks for FPGAs

Low cost 10Gbps TCP/IP IP blocks from COMBLOCK (also 1Gbps version are available)

- **Very flexible license**
- **Low resource utilization**
- **TCP <-> Peripheral bus bridge used, but this bridge can be replaced by many other bus types if needed without changing the register map of the front-end unit**

- **JLAB can distribute downloadable firmware using this IP for ePIC associated projects**

10G TCP/IP Server



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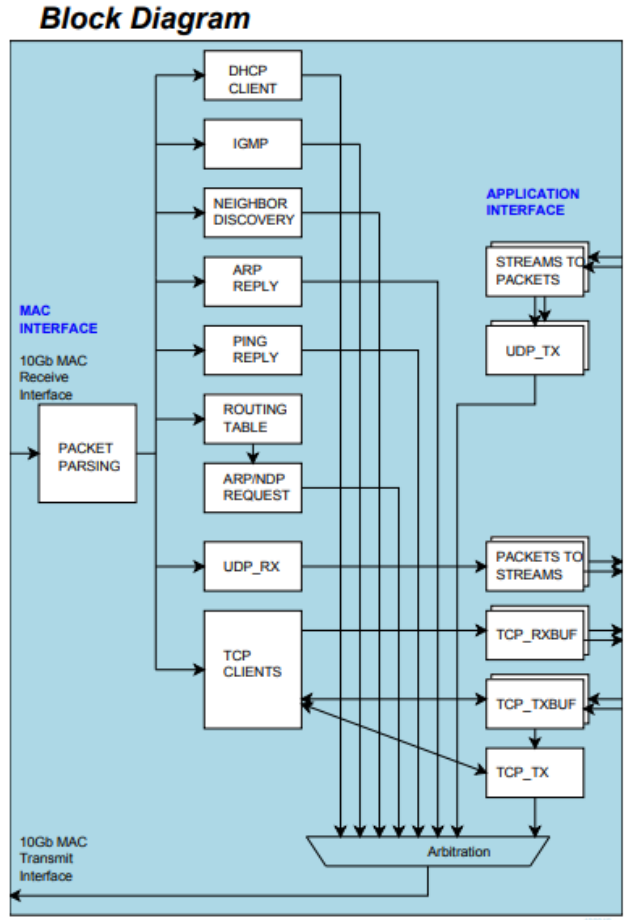
10G TCP/IP Client



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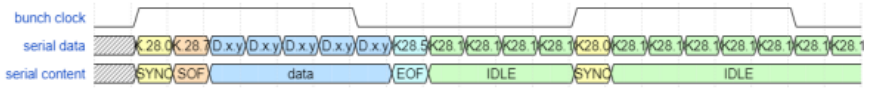
Timing Resolution with Reconstructed Clock

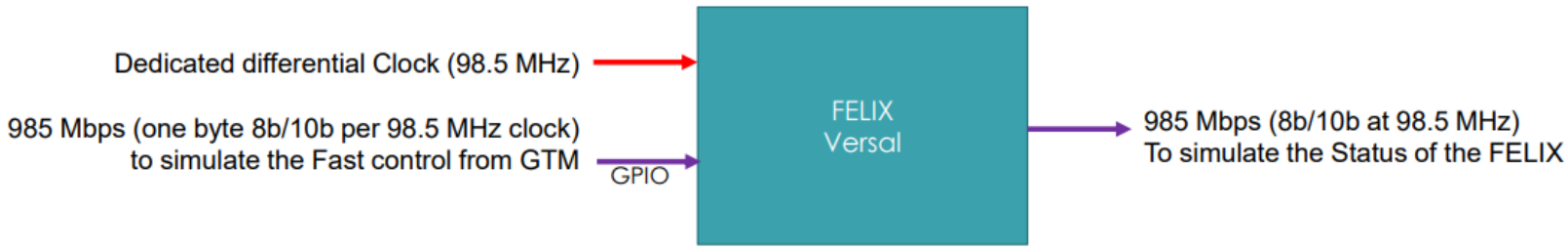
First Results (W. Gu, Jefferson Lab):

- Downlink Custom Protocol:
  - Eight bytes (8b10b) payload per Clock (98.5 MHz)
  - **7.88 Gbps** line rate (6.304 Gbps payload rate)
  - Clock embedded transmission via **GTH** transmitter
- **GTY** Clock recovery works OK
  - The TIE (σ) is below **4ps**
  - Phase is stable, recovered clock reproduces the original (GTH_Ref) Clock
- A **Clock Jitter Cleaner** further improves recovered clock with a TIE (σ) below **2ps**
- Future Tests: Use (Versal based) FELIX prototype

Encoding:



7.88 Gbps line rate
Eight 8b/10b payload per clock (98.5 MHz) equivalent (downlink)
control words: 6.304 Gbps
Control symbols as frame delimiters, BC markers, and IDLEs



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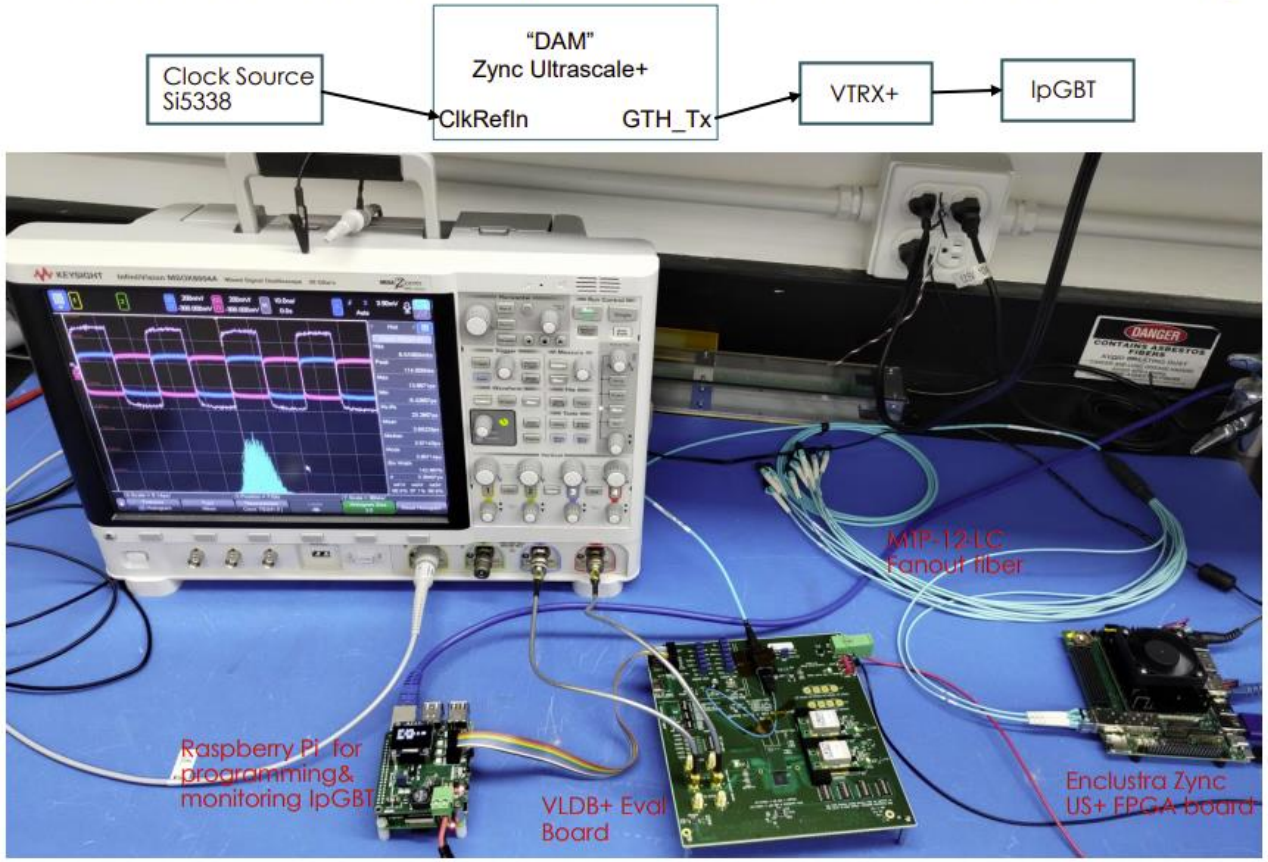
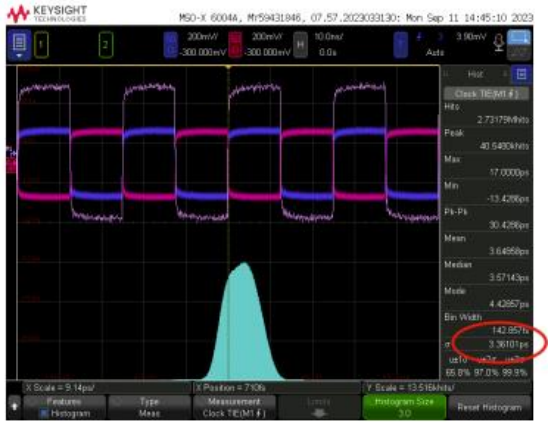
Timing Resolution with Reconstructed Clock

First ePIC Test with lpGBT / VTRx+ based Timing Distribution





- RefClk in: 315.27 MHz (EIC x 2 / 5)
- Phase Adjustable Clock output from lpGBT: 39.4MHz
- TIE: **3.36ps**

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