OAK RIDGE National Laboratory

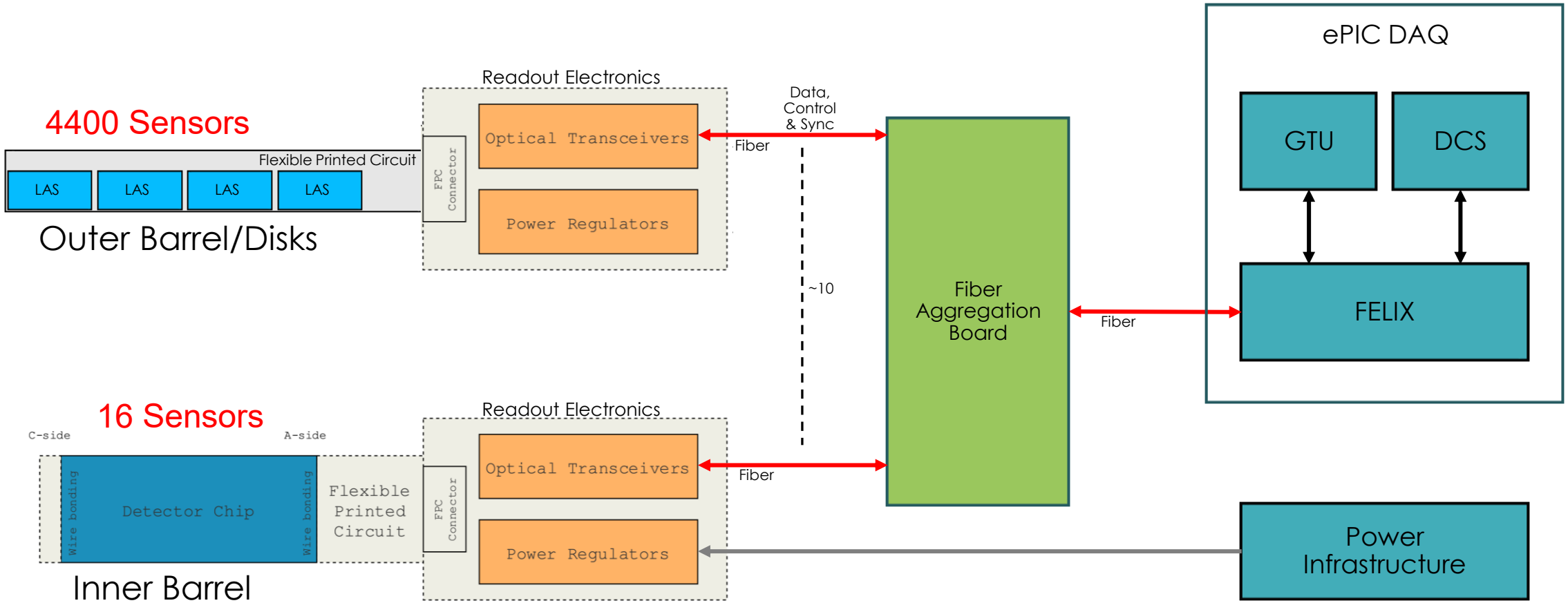
SVT Fiber Aggregation

J. Schambach

ORNL is managed by UT-Battelle LLC for the US Department of Energy

U.S. DEPARTMENT OF ENERGY

SVT Electronics – Simplified Overview



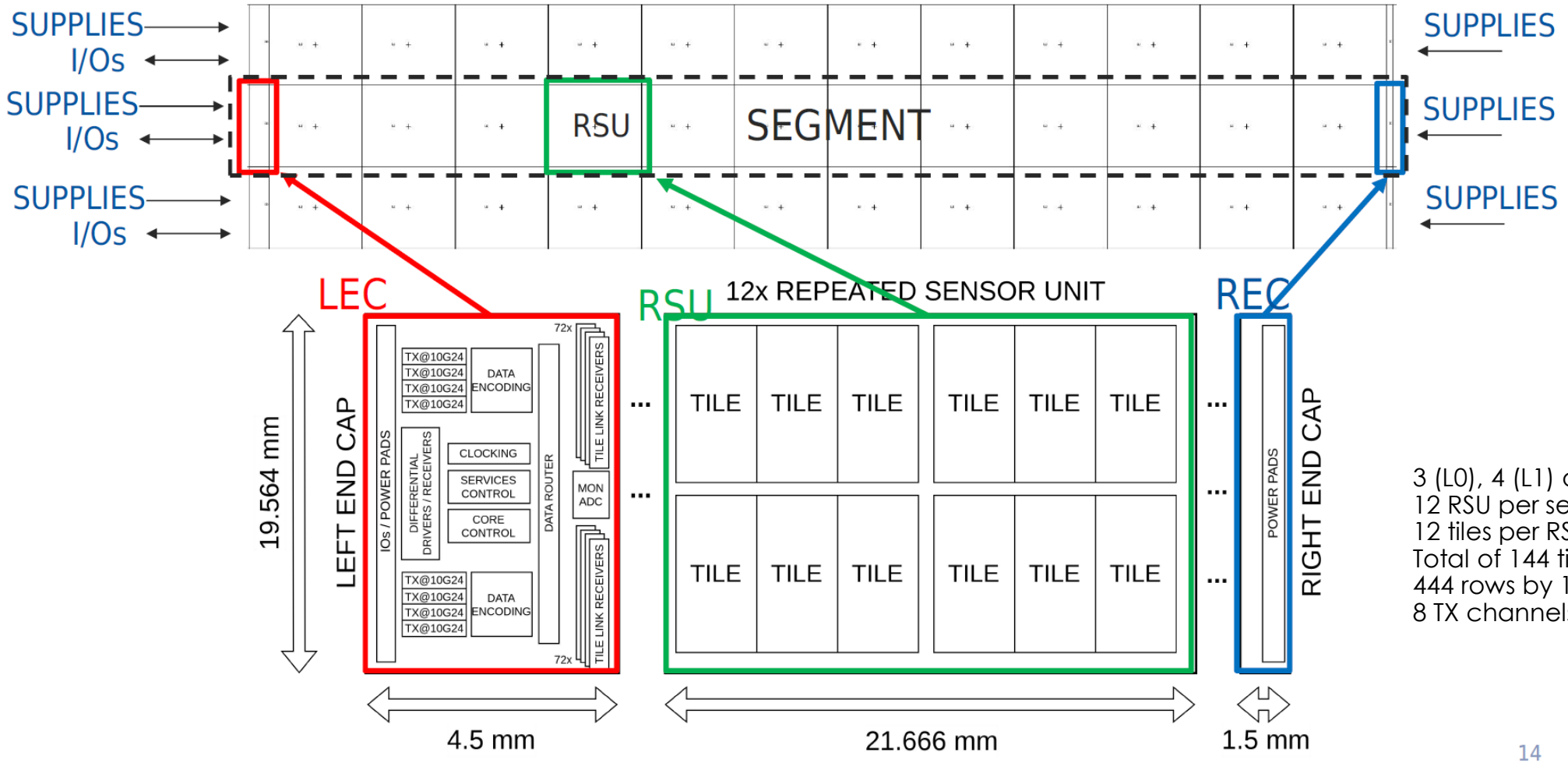
SVT Simulated Data Rates (including SR)

Barrel							10x275 GeV	
Layer Index	Area (mm^2)	# sensors	# pixels	# Data Fibers	# SC Fibers	Hit Rate/ms	Data Rate (Mbps)	Data Rate / Fiber (Mbps)
L0	58,811	4	119,688,192	96	6	1791732.00	218717.29	6075.48
L1	78,414	4	159,584,256	128	8	1095604.00	133740.72	2786.27
L2	196,035	8	398,960,640	320	20	600729.00	73331.18	611.09
L3	882,158	368	1,835,218,944	368	16	1645551.00	200872.92	545.85
L4	2,216,706	1120	4,654,540,800	1120	48	888591.00	108470.58	96.85
e-endcap								
Disk index								
ED0	176,710	96	398,960,640	96	8	538309.00	65711.55	684.50
ED1	536,815	334	1,388,050,560	334	16	976195.00	119164.43	356.78
ED2	553,632	334	1,388,050,560	334	16	940608.00	114820.31	343.77
ED3	552,835	334	1,388,050,560	334	16	618422.00	75490.97	226.02
ED4	551,127	334	1,388,050,560	334	16	97019.00	11843.14	35.46
h-endcap								
Disk index								
HD0	176,710	96	398,960,640	96	8	438216.00	53493.16	557.22
HD1	536,815	334	1,388,050,560	334	16	624534.00	76237.06	228.25
HD2	553,216	334	1,388,050,560	334	16	165565.00	20210.57	60.51
HD3	548,909	334	1,388,050,560	334	16	14334.00	1749.76	5.24
HD4	542,422	334	1,388,050,560	334	16	7064.00	862.30	2.58
TOTAL	**8,161,315**	**4448**	**19,070,318,592**	**4896**	**242**	**1.0442E+10**	**hits/s**	
						1244.8	**Gbps**	
			Noise Rate			1.00E-06	(1/pixel/10us)	
			Total Noise Pixels/s			1.91E+07	pixel/s	
			Total Noise Rate			**114**	**Gbps**	

32bit/pixel

64bit/pixel

MOSAIX Architecture



SVT IB

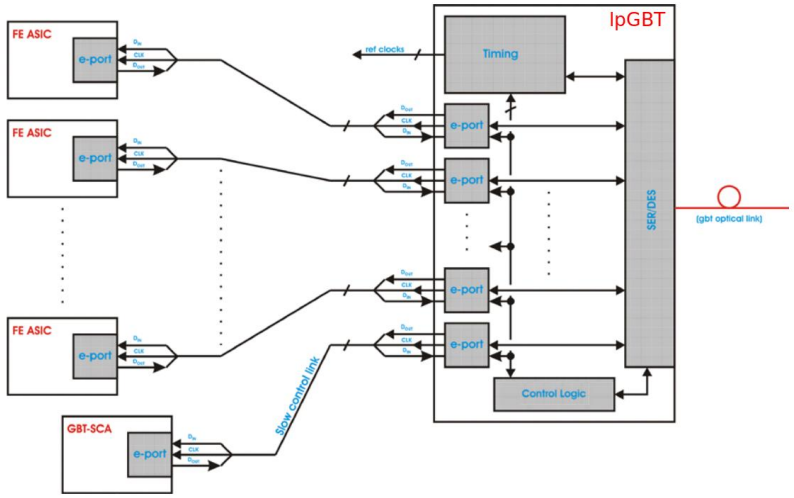
3 (L0), 4 (L1) or 5 (L2) segments
12 RSU per segment
12 tiles per RSU
Total of 144 tiles per segment
444 rows by 156 columns per tile
8 TX channels per segment

14

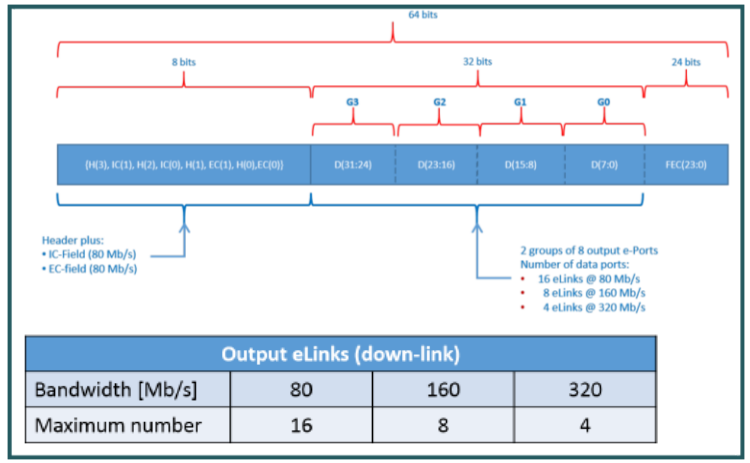
SVT **LAS** (OB, disks) is a MOSAIX with a **single** segment and only **6 RSU**, using only **1 TX** channel

OAK RIDGE National Laboratory

lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 256 bit or 128 bit
  - 256bit frame contains 192 bits of payload (7.68 Gbps)
  - 128bit frame contains 96 bits of payload (3.84 Gbps)



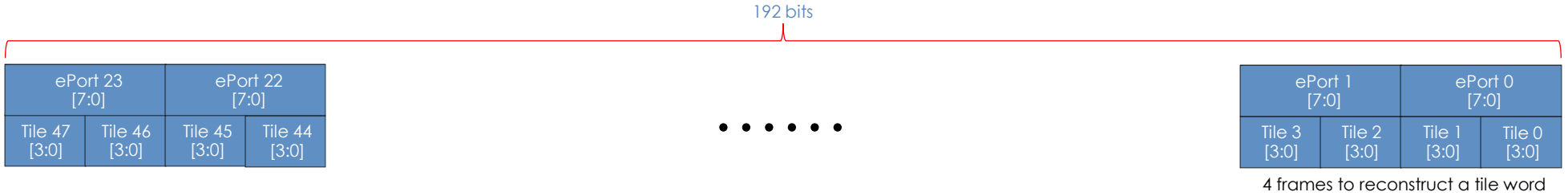
Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

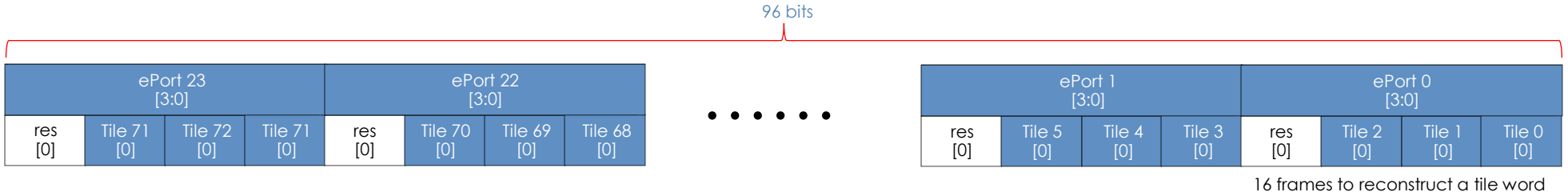
Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

SVT Data Format

MOSAIX: 10.24 Gbps



LAS: 5.12 Gbps



Tile Data Words

READOUT PROTOCOL

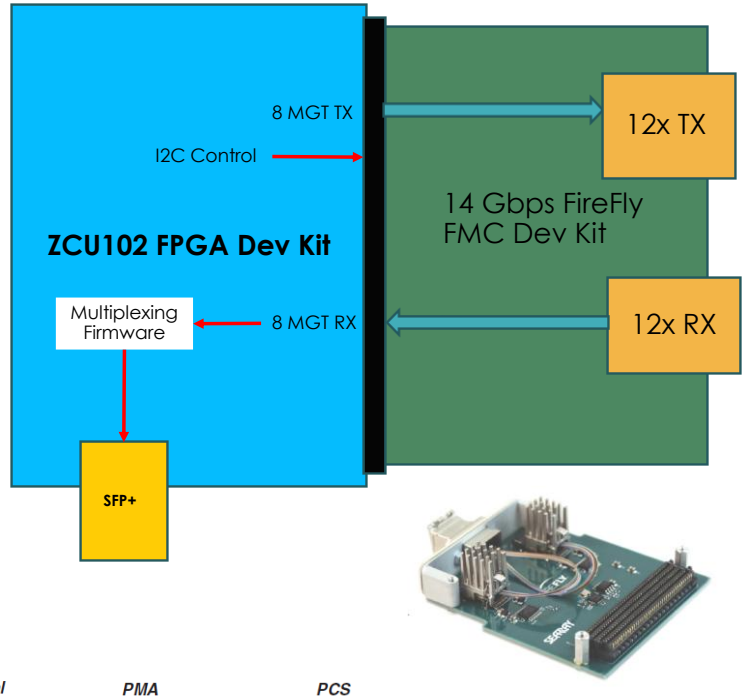
Word type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]								Drop
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]								Drop
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]								Drop
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]				Integration Window Counter [7:0]								Drop
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]					Tile [1:0]		T/B	
REGION_HEADER	1	0	1	0	1	1	Region Address.		Integration Window Counter [7:0]								
DATA	0	Pixel Address Row [8:0]									Pixel Address Column [5:0]						
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]				Packet Checksum [7:0]								
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]				Integration Window Counter [7:0]								Drop
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]				Integration Window Counter [7:0]								Drop
RECOVERY	1	0	0	1	0	0	1	1	'0								Drop
RESERVED	1	0	0	0	RESERVED												

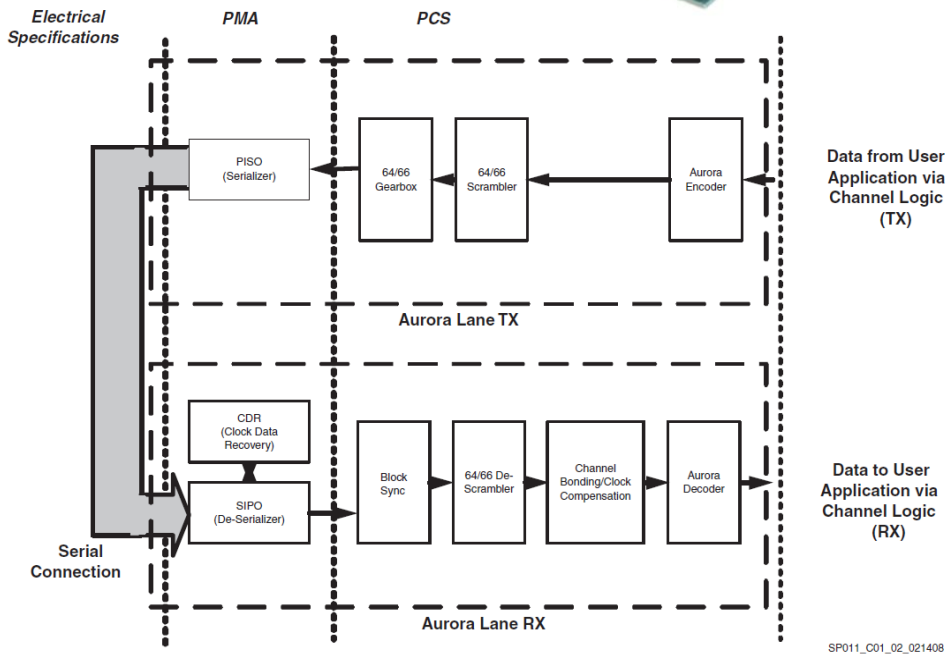
Text is not SVG - cannot display

OAK RIDGE National Laboratory

Implementation Proposal

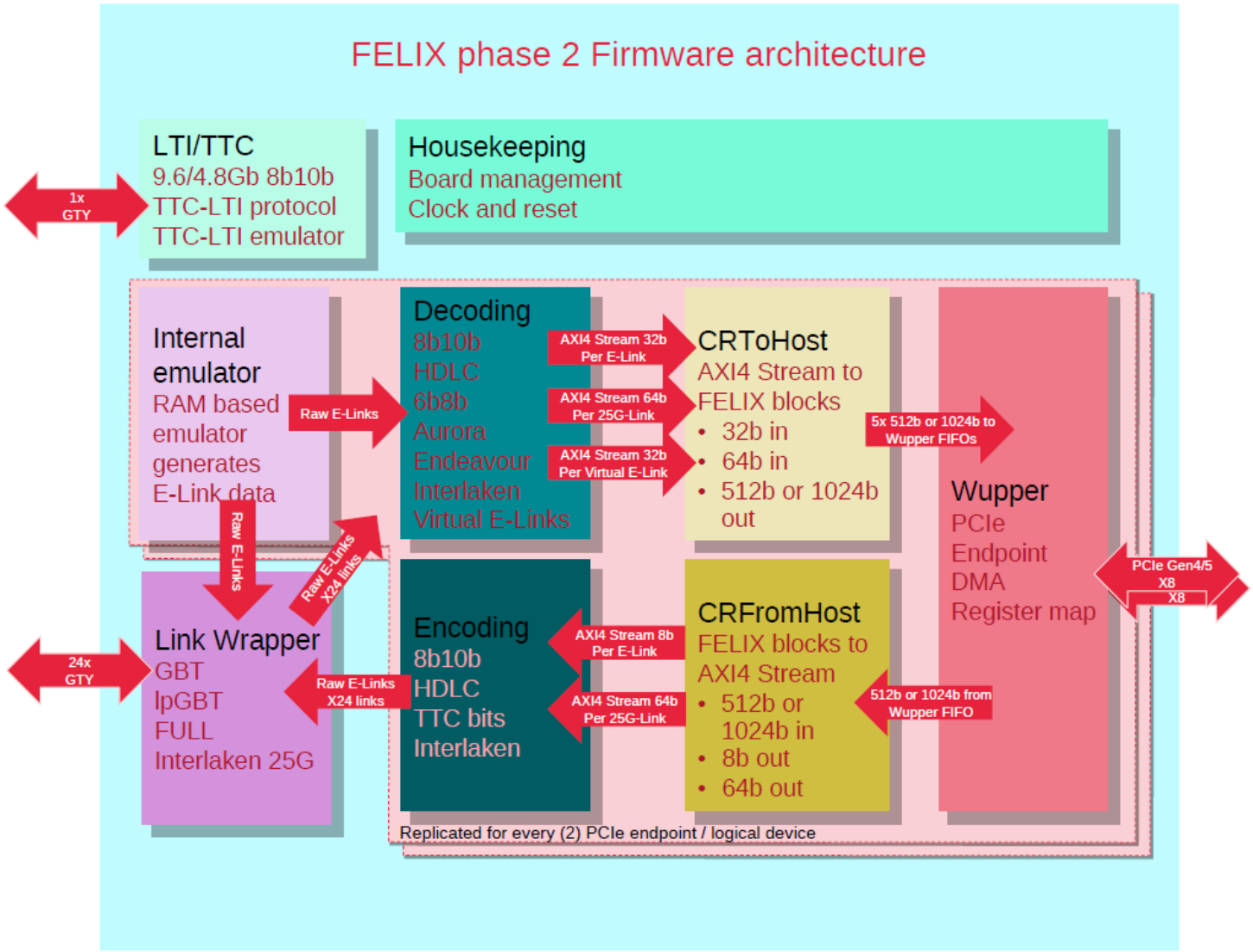
- **Kintex Ultrascale+** based (custom) board, ~500 boards
- Interface to SVT via GTH/GTY channels using **Samtec Optical FireFly** for up to 10 (?) RX or x (?) TX channels
- Using **lpGBT** protocol, **10.24/5.12 Gbps**, on SVT side
- Interface to FELIX via single bidir GTY channel up to **25.7813 Gbps** using **SFP+**
- Using e.g. **Aurora 64B/66B protocol** on FELIX side (https://docs.amd.com/v/u/en-US/aurora_64b66b_protocol_spec_sp011):
  - Lightweight link-layer protocol to move data point-to-point across one or more high-speed serial lanes.
  - Using 64B/66B encoding (more efficient than 8B/10B)
  - Data transferred through Aurora "channels" in frames
  - Frames share channel with control, clock compensation & idles
  - Frames can be any length, any format
  - Frames can be interrupted by flow control or idles



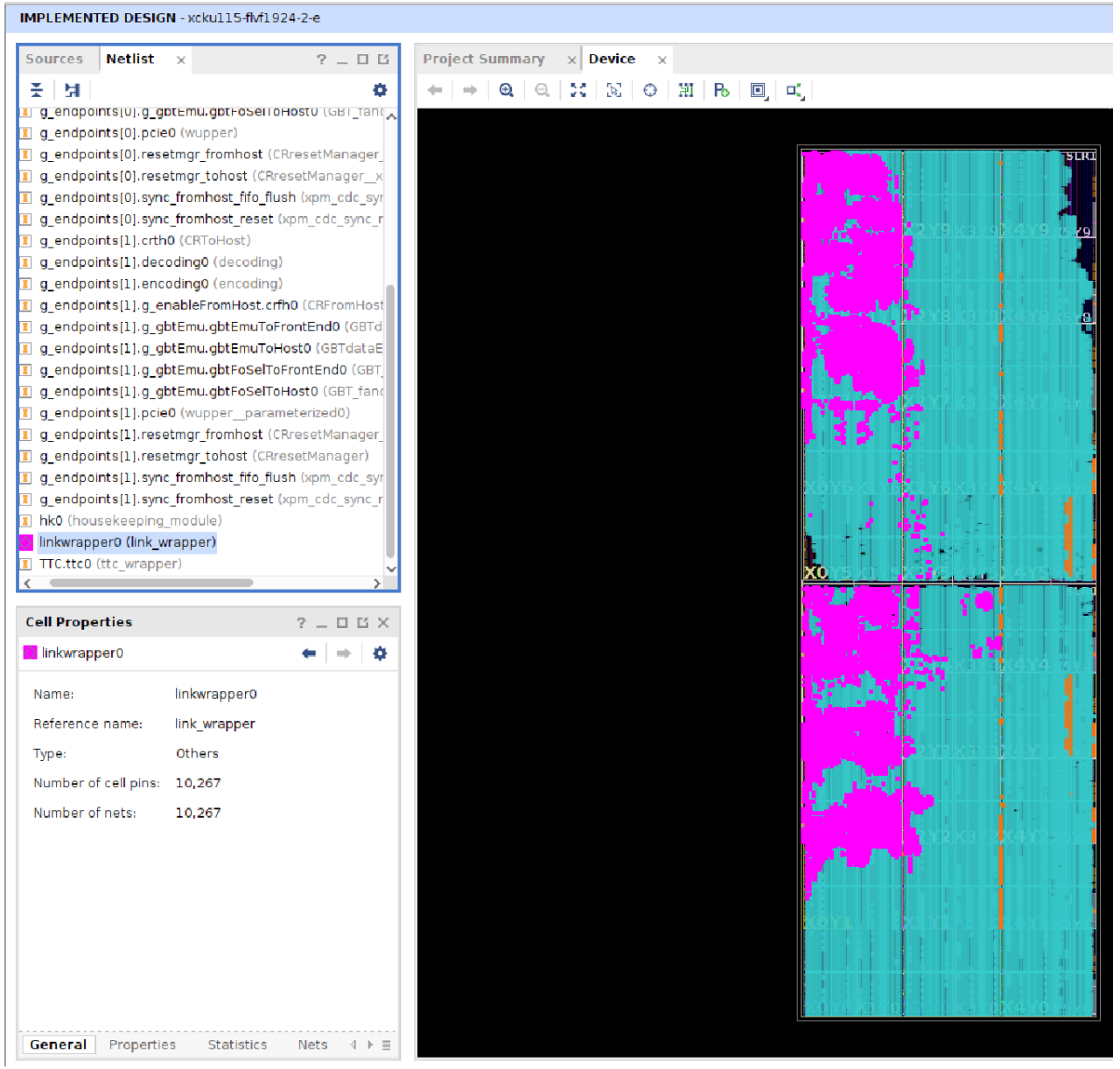


OAK RIDGE National Laboratory

FELIX Firmware as an example for fiber aggregation



Vivado Impementation Results



OAK RIDGE National Laboratory

FELIX Resource Usage for 24 lpGBT Links (xcku115)

Name	CLB LUTs (663360)	CLB Registers (1326720)	CARRY8 (82920)	F7 Muxes (331680)	F8 Muxes (165840)	CLB (82920)	LUT as Logic (663360)	LUT as Memory (293760)	Block RAM Tile (2160)	Bonded IOB (728)	HPIOB (624)	HRIO (104)	HPIOBDIFFINBUF (480)	HPIOBDIFFOUTBUF (480)	BITSLICE_RX_TX (7488)	BUFGCE (576)	BUFGCE_DIV (96)	BUFG_GT (384)	BUFGCTRL* (192)	MMCME3_ADV (24)	GTHE3_CHANNEL (64)	GTHE3_COMMON (16)	IBUFDS_GTE3 (32)	PCIE_3_1 (6)	SYSMONE1 (2)
felix_top	60.73%	35.43%	4.19%	2.84%	1.33%	95.65%	59.90%	1.87%	44.19%	18.54%	9.94%	70.19%	0.83%	0.42%	0.01%	3.30%	1.04%	15.10%	0.52%	20.83%	62.50%	25.00%	12.50%	33.33%	50.00%
busy0 (ttc_busy)	0.77%	0.38%	0.00%	0.00%	0.00%	1.62%	0.77%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
clk0 (clock_and_reset)	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.03%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.21%	0.21%	0.01%	1.74%	0.00%	0.00%	0.52%	12.50%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].crth0 (CRToHost	1.84%	1.27%	0.62%	0.07%	0.00%	5.34%	1.82%	0.04%	4.84%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].decoding0 (dec	17.21%	6.57%	0.07%	0.21%	0.00%	28.64%	16.98%	0.52%	4.49%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].encoding0 (enc	0.33%	0.41%	0.00%	0.04%	0.00%	1.48%	0.33%	0.00%	0.56%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].g_enableFromHo	0.37%	0.23%	0.03%	0.00%	0.00%	0.80%	0.27%	0.21%	2.22%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].g_gbtEmu.gbtEn	0.04%	<0.01%	<0.01%	0.00%	0.00%	0.15%	0.04%	0.00%	0.74%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].g_gbtEmu.gbtEn	0.24%	<0.01%	<0.01%	0.00%	0.00%	1.01%	0.24%	0.00%	4.70%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].g_gbtEmu.gbtFo	0.00%	0.10%	0.00%	0.00%	0.00%	0.45%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].g_gbtEmu.gbtFo	0.28%	0.62%	0.00%	0.00%	0.00%	2.98%	0.28%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].pcie0 (wupper	7.21%	5.34%	0.66%	1.03%	0.65%	25.02%	7.15%	0.14%	2.52%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.52%	0.00%	1.30%	0.00%	4.17%	12.50%	12.50%	3.13%	16.67%	0.00%
g_endpoints[0].resetmgr_fromh	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.02%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].resetmgr_tohost	<0.01%	<0.01%	0.00%	0.00%	0.00%	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].sync_fromhost_f	0.00%	<0.01%	0.00%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].sync_fromhost_r	0.00%	<0.01%	0.00%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].crth0 (CRToHost	1.84%	1.27%	0.62%	0.07%	0.00%	5.06%	1.82%	0.04%	4.84%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].decoding0 (dec	17.20%	6.57%	0.07%	0.21%	0.00%	28.41%	16.97%	0.52%	4.49%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].encoding0 (enc	0.33%	0.41%	0.00%	0.04%	0.00%	1.36%	0.33%	0.00%	0.56%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].g_enableFromHo	0.37%	0.23%	0.03%	0.00%	0.00%	0.76%	0.27%	0.21%	2.22%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].g_gbtEmu.gbtEn	0.04%	<0.01%	<0.01%	0.00%	0.00%	0.10%	0.04%	0.00%	0.74%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].g_gbtEmu.gbtEn	0.24%	<0.01%	<0.01%	0.00%	0.00%	0.98%	0.24%	0.00%	4.70%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].g_gbtEmu.gbtFo	0.00%	0.10%	0.00%	0.00%	0.00%	0.47%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].g_gbtEmu.gbtFo	0.28%	0.62%	0.00%	0.00%	0.00%	2.64%	0.28%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].pcie0 (wupper	7.16%	5.18%	0.66%	1.04%	0.63%	23.90%	7.10%	0.13%	2.52%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.52%	0.00%	1.30%	0.00%	4.17%	12.50%	12.50%	3.13%	16.67%	0.00%
g_endpoints[1].resetmgr_fromh	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.02%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].resetmgr_tohost	<0.01%	<0.01%	0.00%	0.00%	0.00%	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].sync_fromhost_f	0.00%	<0.01%	0.00%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[1].sync_fromhost_r	0.00%	<0.01%	0.00%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
hk0 (housekeeping_module)	0.38%	0.32%	0.25%	0.04%	0.04%	0.87%	0.37%	<0.01%	0.00%	0.00%	0.00%	0.00%	0.21%	0.00%	0.00%	0.17%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	50.00%
linkwrapper0 (link_wrapper)	4.90%	5.66%	0.82%	0.06%	0.00%	13.58%	4.90%	0.00%	3.89%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	12.50%	0.00%	0.00%	37.50%	0.00%	6.25%	0.00%	0.00%
TTC.ttc0 (ttc_wrapper)	0.16%	0.13%	0.08%	0.01%	<0.01%	0.44%	0.15%	0.03%	0.16%	0.00%	0.00%	0.00%	0.42%	0.00%	0.00%	0.17%	1.04%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
g_endpoints[0].sync_fromhost_r	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].crth0 (CRToHost	12176	16824	516	240	0	4196	12044	132	104.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].decoding0 (dec	114126	87218	56	713	0	23559	112594	1532	97	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].encoding0 (enc	2198	5470	0	144	0	1124	2198	0	12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].g_enableFromHo	2425	2994	24	0	0	631	1801	624	48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].g_gbtEmu.gbtEn	235	15	2	0	0	80	235	0	16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].g_gbtEmu.gbtEn	1567	70	2	0	0	811	1567	0	101.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].g_gbtEmu.gbtFo	0	1296	0	0	0	390	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].g_gbtEmu.gbtFo	1848	8244	0	0	0	2192	1848	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].pcie0 (wupper	47467	68733	551	3456	1037	19818	47072	395	54.5	0	0	0	0	0	0	3	0	5	0	1	8	2	1	1	0
g_endpoints[1].resetmgr_fromh	21	10	0	0	0	16	21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].resetmgr_tohost	12	11	0	0	0	7	12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].sync_fromhost_f	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
g_endpoints[1].sync_fromhost_r	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
hk0 (housekeeping_module)	2493	4188	209	129	64	721	2465	28	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	
linkwrapper0 (link_wrapper)	32510	75126	678	192	0	11260	32510	0	84	0	0	0	0	0	0	0	0	48	0	0	24	0	2	0	0
TTC.ttc0 (ttc_wrapper)	1055	1695	67	35	14	364	966	89	3.5	0	0	0	2	0	0	1	1	0	0	0	0	0	0	0	0

CLB = Configurable Logic Block (LUTs, FFs, Arith. Carry Chains, MUXs, Shift Register Logic, Distributed RAM)

Kintex UltraScale+ FPGA Feature Summary

Table 5: **Kintex UltraScale+ FPGA Feature Summary**

	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
System Logic Cells	355,950	474,600	599,550	653,100	746,550	1,143,450
CLB Flip-Flops	325,440	433,920	548,160	597,120	682,560	1,045,440
CLB LUTs	162,720	216,960	274,080	298,560	341,280	522,720
Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
Block RAM Blocks	360	480	912	600	744	984
Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
UltraRAM Blocks	48	64	0	80	112	128
UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
CMTs (1 MMCM and 2 PLLs)	4	4	4	8	4	11
Max. HP I/O(1)	208	208	208	416	208	572
Max. HD I/O(2)	96	96	96	96	96	96
DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
System Monitor	1	1	1	1	1	1
GTH Transceiver 16.3Gb/s	0	0	28	32	28	44
GTY Transceivers 32.75Gb/s(3)	16	16	0	20	0	32
Transceiver Fractional PLLs	8	8	14	26	14	38
PCIe Gen3 x16 and Gen4 x8	1	1	0	4	0	5
150G Interlaken	0	0	0	1	0	4
100G Ethernet w/RS-FEC	0	1	0	2	0	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See Table 6.

Kintex UltraScale FPGA Feature Summary

Table 3: **Kintex UltraScale FPGA Feature Summary**

	KU025(1)	KU035	KU040	KU060	KU085	KU095	KU115
System Logic Cells	318,150	444,343	530,250	725,550	1,088,325	1,176,000	1,451,100
CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	4.1	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM Blocks	360	540	600	1,080	1,620	1,680	2,160
Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
I/O DLLs	24	40	40	48	56	64	64
Maximum HP I/Os(2)	208	416	416	520	572	650	676
Maximum HR I/Os(3)	104	104	104	104	104	52	156
DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
System Monitor	1	1	1	1	2	1	2
PCIe Gen3 x8	1	2	3	3	4	4	6
150G Interlaken	0	0	0	0	0	2	0
100G Ethernet	0	0	0	0	0	2	0
GTH 16.3Gb/s Transceivers(4)	12	16	20	32	56	32	64
GTY 16.3Gb/s Transceivers(5)	0	0	0	0	0	32	0
Transceiver Fractional PLLs	0	0	0	0	0	16	0

Notes:

1. Certain advanced configuration features are not supported in the KU025. Refer to the Configuring FPGAs section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See Table 4.
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 4.

FELIX
BNL712

Fiber Aggregator Firmware

- Up to 20 lpGBT channels should be possible in one of the smaller US+ FPGAs based on resource usage in ATLAS FELIX firmware
- Add firmware for Aurora protocol
- Aggregation Firmware (**uplink**):
  - Assemble lpGBT frames into 16bit tile words for each tile depending on data rate (LAS vs MOSAIX)
  - Only keep "data" tile words
  - Drop other tile words or handle locally (errors, dropped frames, empty frames, status, …)
  - Add geometric word to identify tile and mux into TX channel towards FELIX
  - Add summary status for locally handled conditions
- Slow Controls Firmware (**downlink, maybe separate boards not shared with uplink?**):
  - Separate downlink data into individual lpGBT channels and interpret (pass-through, handle locally)
  - Add sync signal to delimit readout frames for IB
  - Add commands for readout frame generation on AncASIC for OB and disks
  - (others?) …..