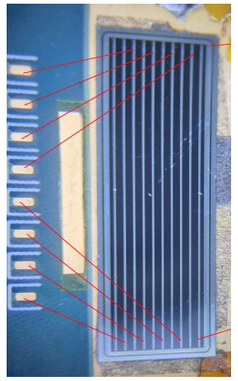
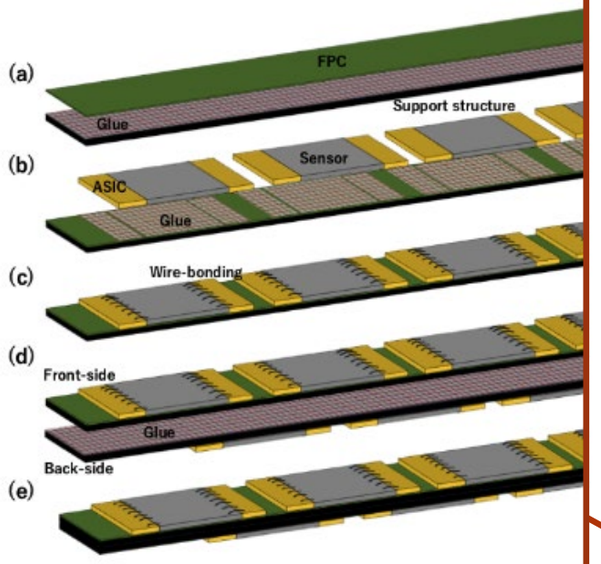
TOF QA plans

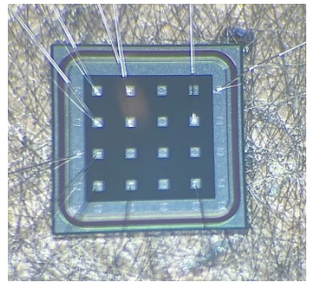
Dr. Simone M. Mazza (SCIPP, UC Santa Cruz)
For the BTOF/FTOF group

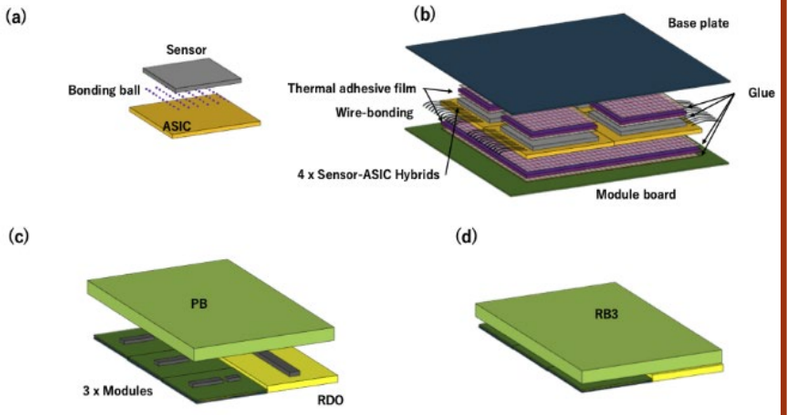
TOF layout in ePIC





Sensors: strips
Readout: FCFD

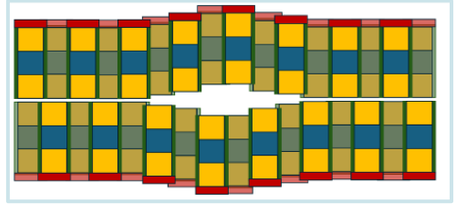




Sensors: pixels
Readout: EICROC

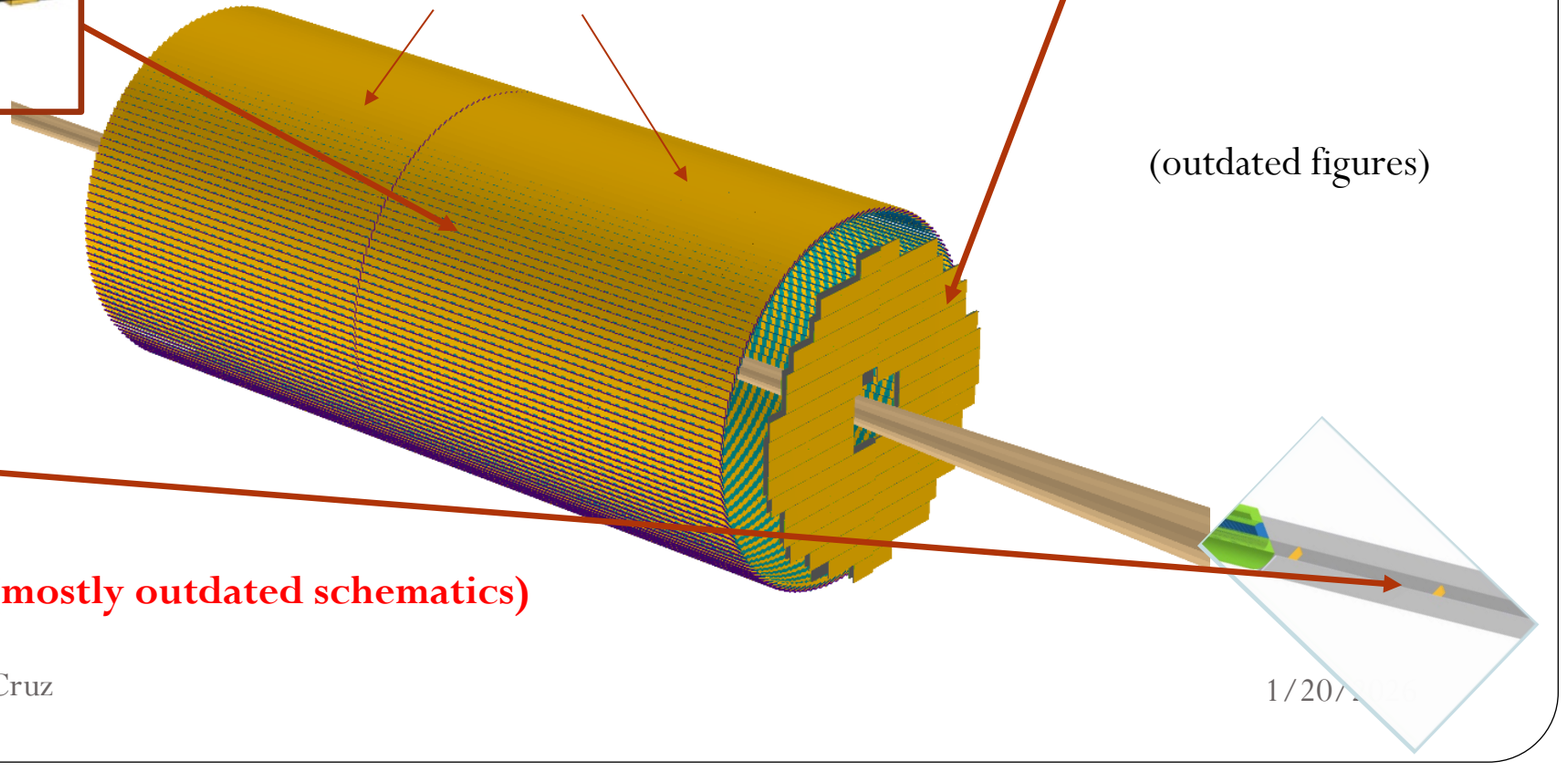
Divided in two halves

(outdated figures)



Sensors: pixels
Readout: EICROC

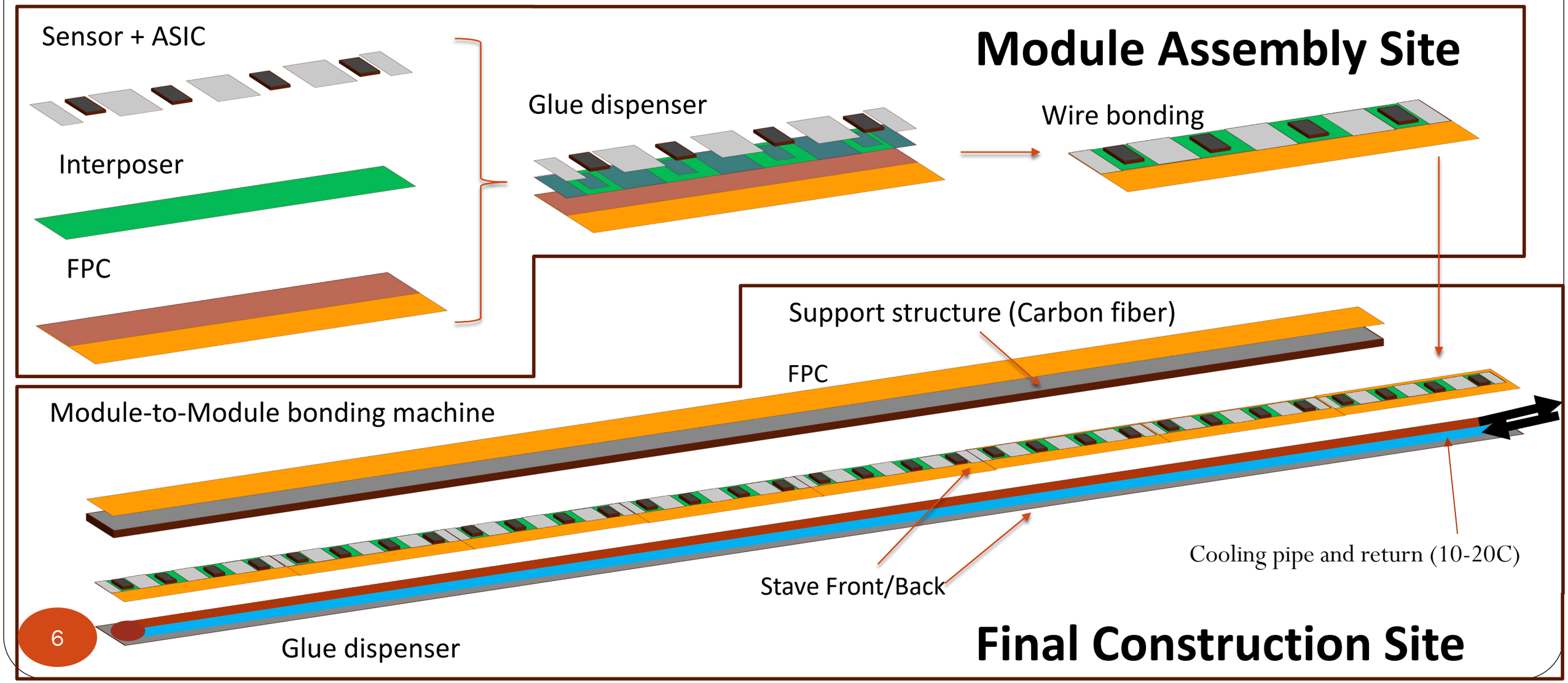
Off-Momentum Detectors (OMD)



(mostly outdated schematics)

BTOF

Stave Assembling Steps (Opt1)



BTOF QA

- Sensors
  - IV on all sensor during pre-production, CV on a fraction to monitor gain layer homogeneity. N+ resistivity test on a subset. Small fraction tested with laser (and TB) to check homogeneity of response.
  - Equipment: probe station, laser TCT, test beam
- ASIC
  - Powering some chips during pre-production, test with calibration input. A fraction integrated with sensor and tested with laser/source
  - Equipment: wire-bonder, probe station, laser TCT
- Interposer and FPC
  - Impedance tests and thickness measurement
  - Equipment: measuring tools, electrical tools
- Gluing process
  - Stress test (pull, move) and temperature cycling. Pull apart and check glue layer. Thermal connection tests
  - Equipment: glue robot, climate chamber, tooling

BTOF QA

- Stavelet assembly
  - Placement test, connection test, charge collection test
  - Equipment: glue robot, wire bonder, smart scope, probe station, testing board and bench (to be developed)
- Stave assembly
  - Placement test, charge collection test, thermal tests
  - Equipment: glue robot, wire bonder, large testing area, smart scope, probe station, power board
- Power board
  - Electrical tests

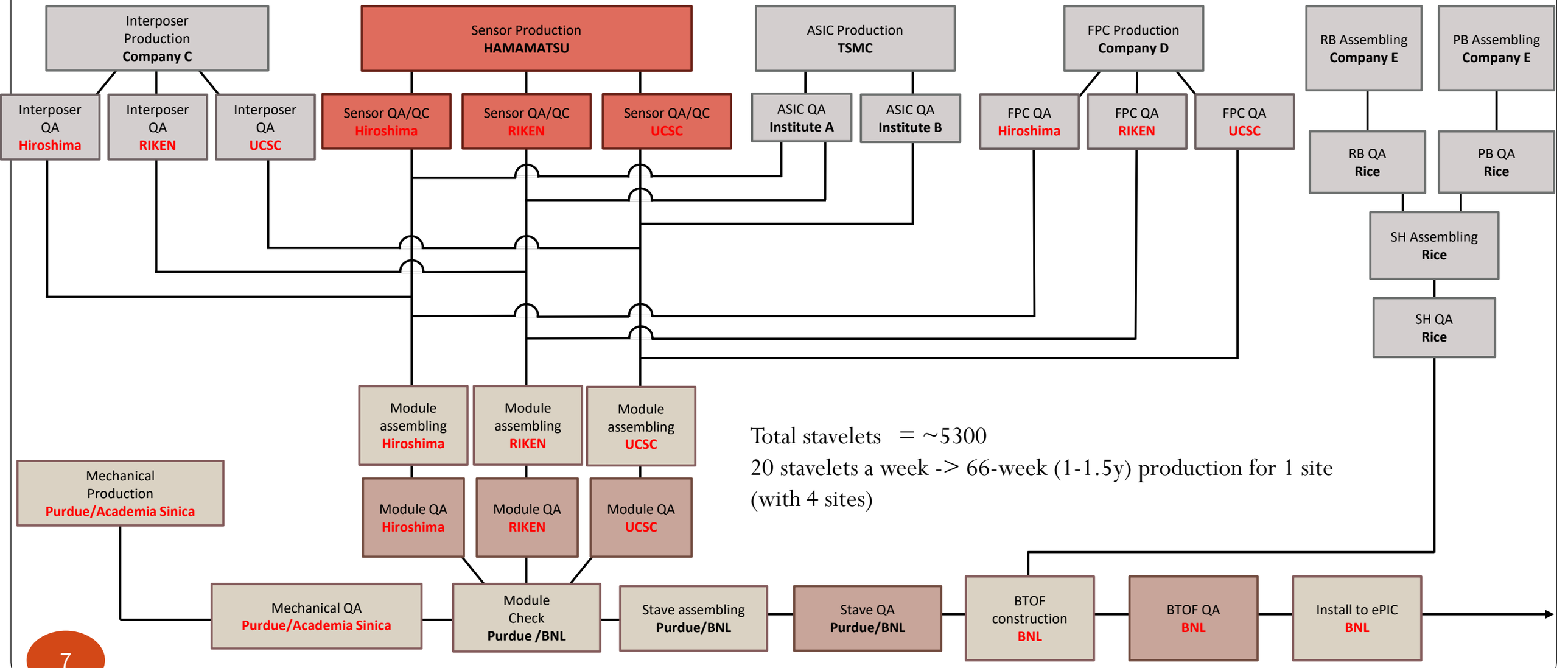
FTOF

FTOF QA

- The main deliverable for the module part of the scope is known good modules , tested to meet a set of requirements at the assembly site
- The testing of production modules done covers
  - Electrical testing of sensors, ASIC and assemblies → Probe station
    - IV curves
    - Functional testing of ASIC, Assemblies
  - Visual inspection of the Sensor, ASIC, Assemblies and module after assembly → Smart scope
  - Functional testing: Power-up, tuning, stress test, thermal cycling (important for bump-bonding assessment) → climate chamber, tooling
- Source testing : Functional testing with source, test beam with subset of modules for QA (identify disconnected bumps, assess performance during production) → sources, test bench
- Repeat test after irradiation to verify compliance with requirements

Facilities

Detector Assembling Workflow BTOF



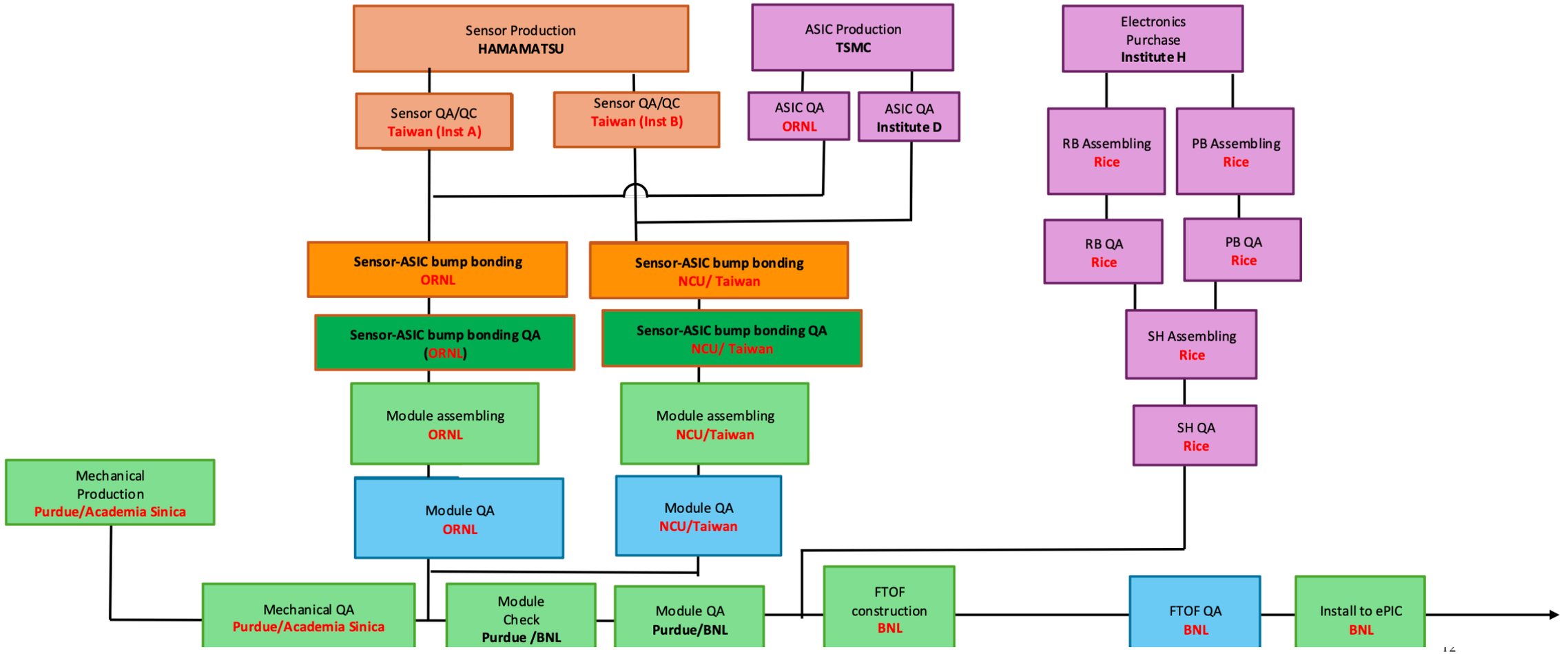
Total stavelets = ~5300

20 stavelets a week -> 66-week (1-1.5y) production for 1 site (with 4 sites)

BTOF institutes QA

- Hiroshima – Sensor QA, FPC QA, interposer QA, wirebond and assembly QA
- Riken – design FPC, define FPC QC/QA, wirebond and assembly QA
- UCSC – Gluing QA, sensor QA, wirebond and assembly QA
- UIC – module QA?
- FNAL – FCFD QA?
- Purdue – Stave assembly QA
- Additional stavelet QA/QC site?
- Rice – power board QA
- ? – database set up and maintenance

FTOF Assembly Workflow



Total modules = ~856

20 modules a week -> 43-week (<1 year) production for 1 site

FTOF institutes QA

- ORNL - Sensor QA, ASIC QA, bump-bonding
- NCU, Taiwan – Sensor QA, bump-bonding
- Purdue – mechanical QA, module QA
- Rice – electronics (power board) QA
- BNL – module QA

Conclusions

- Multiple institution needed for QA process
  - Need to define roles
  - Need to match assembly task plans
- Assembly procedure generally defined, but missing a lot of details
  - More institutions involved might be necessary, especially for module testing

Backup

BTOF Plans

Thermo mechanical test – 2025

- Ongoing with PED funds 2025, production of a simple 1 stavelet demonstrator front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers.

Assembly R&D - 2026

- Define glue and first version of Jigs. Define assembly procedure and QC procedure before assembly

Prototype 1 – 2026

- Production of a full stave demonstrator front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers.

Assembly R&D – 2027

- Shipping tests, finalize assembly and identify assembly machines, finalize jigs. QC procedure before-after assembly. Build first QC test station for stavelet

Prototype 2 – 2027

- Production of a full stave rack demonstrator (4 staves) front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers. Production of a stavelet with working ASIC and development of PCB for stavelet testing.

Pre-production – 2028

- 10% of production, 500 stavelets

Production – 2028-2030

- Remaining 90% of production, 5000 stavelets

Stavelet production volume

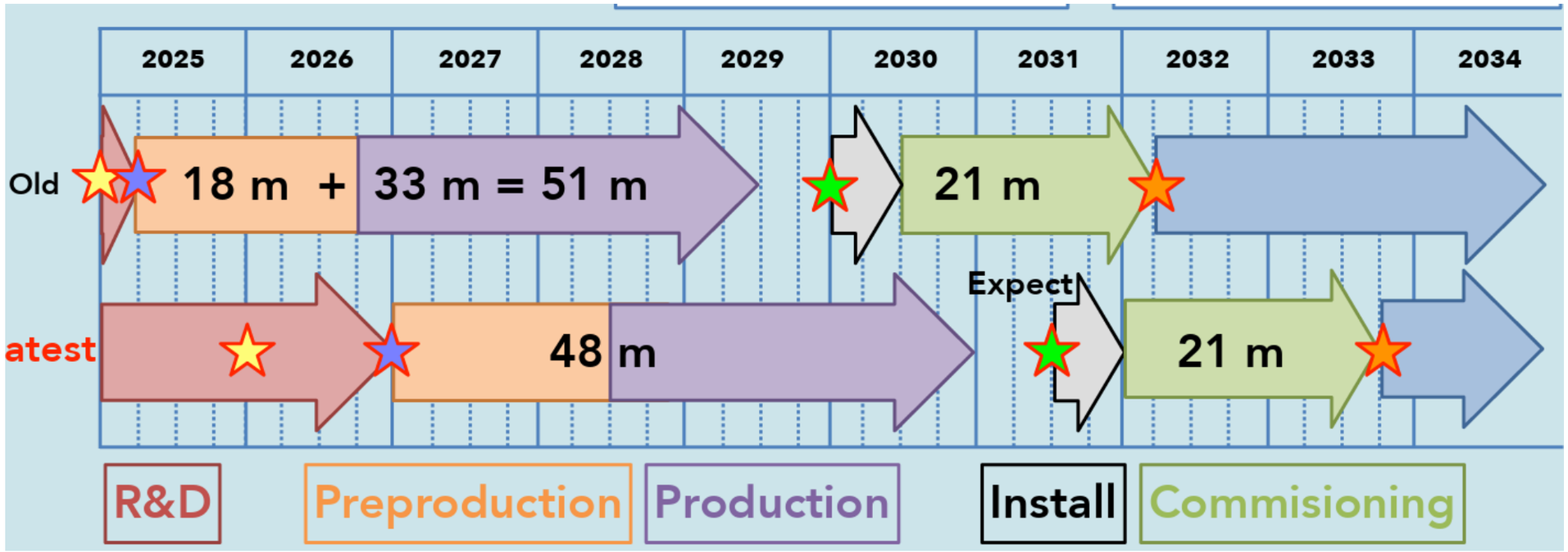
- BTOF has 18432 ASICs that need to be connected to sensors. Assuming 4/5 yield, we need to connect 23040 ASICs. ASICs and sensors are assembled on a stavelet.

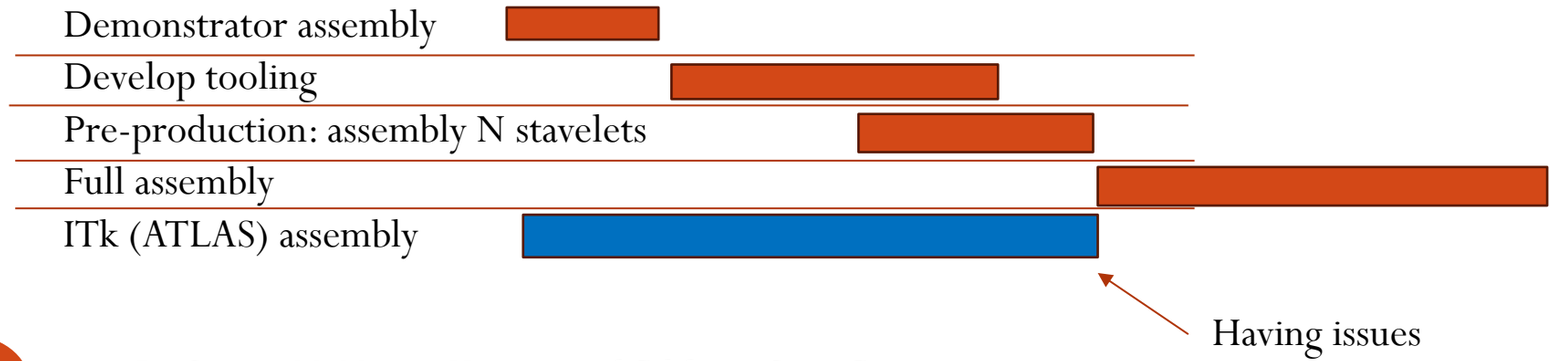
- Volume: 144 staves, 288 half staves made of 16 stavelets (top and bottom)
  - Wirebonds per stavelet: ((128 + 128)x2 (sensors-> interposer ->chip) + ~20(chip))x4 -> ~2000 bonds.
  - 4608 stavelets +10-20% yield adjustment, ~5300 to assembly in 2 years
  - Assuming 4 BTOF assembly sites: ~1300 stavelets per site in 2 years, around 3 stavelet per day -> possible

Crucial activities for the next year or two

- Interposer board finalized design, to do when FCFD is available
- Interposer board simulation in HFSS to understand transient signal effects
- Identification of correct glue (UV or bi-component), viscosity, thermal conductivity
  - It might be necessary to use two different types of glue: thermally conductive glue for ASIC, electrically conductive for sensor
  - If UV glue, design of UV curing box. If bi-component glue, glue robot calibration vs viscosity. If thermal cure, check effects on components
- Identification of glue robot configuration or glue panning with jigs
- Define QC procedure before assembly
- Define QC during assembly (metrology)
- Define QC procedure after assembly (DAQ?) and testing PCB
- Design jigs for stavelet assembly, movement and shipping
- Define wire bond encapsulation needs and procedure
- Define and build database
- To identify the correct components, it might be useful to go to fairs, like Semiconductor West

BTOF road-to-assembly





Assembly time of one stavelet

- Glue placement: 20 minutes
- Component placement: 20 minutes
- Glue cure: UV 5-10 minutes, bi-component 12h, thermal ~1h
- QC on glued component: 30 minutes (metrology)
- Wire bonding: 20 minutes
- QC on full stavelet: 1h
- Full time: ~2-3h per stavelet (minus long glue cure time)

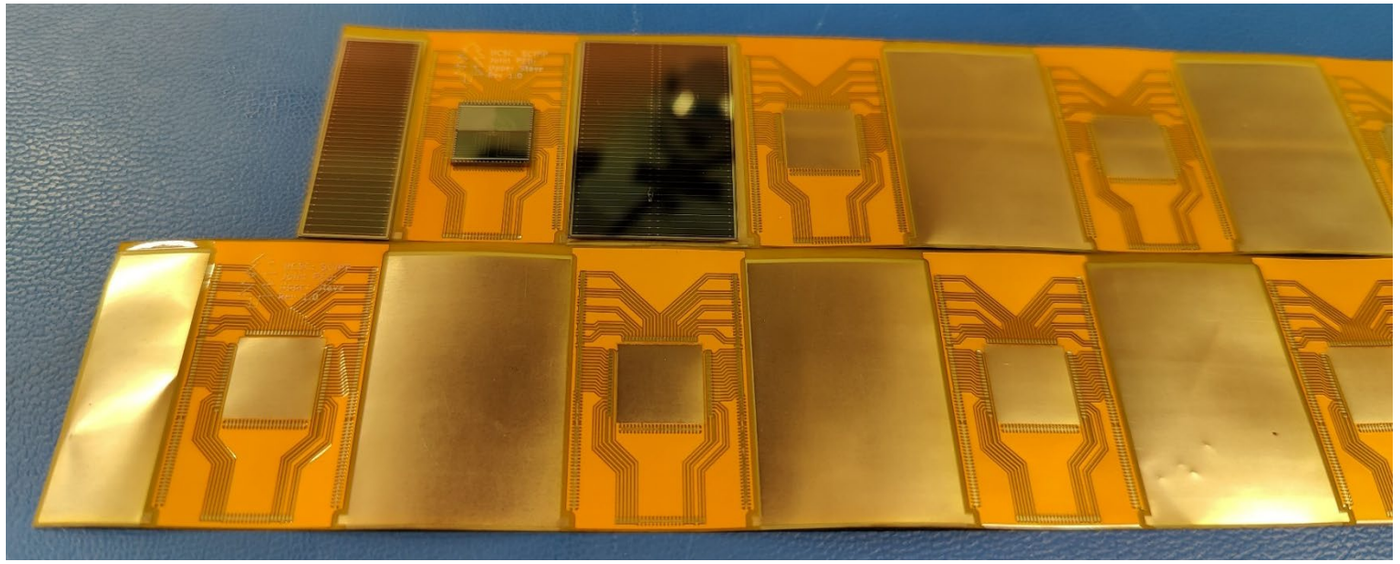
- With parallelization it can be lowered (e.g. glue deposit on a jig with multiple stavelets). **Likely QC will be most time consuming.**

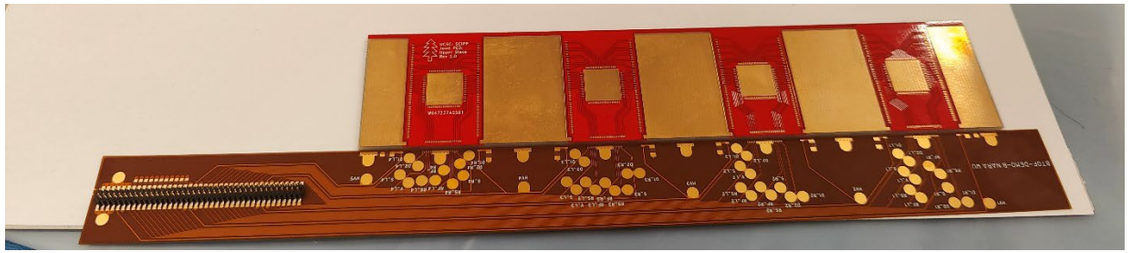
Assembly procedure for stave tray

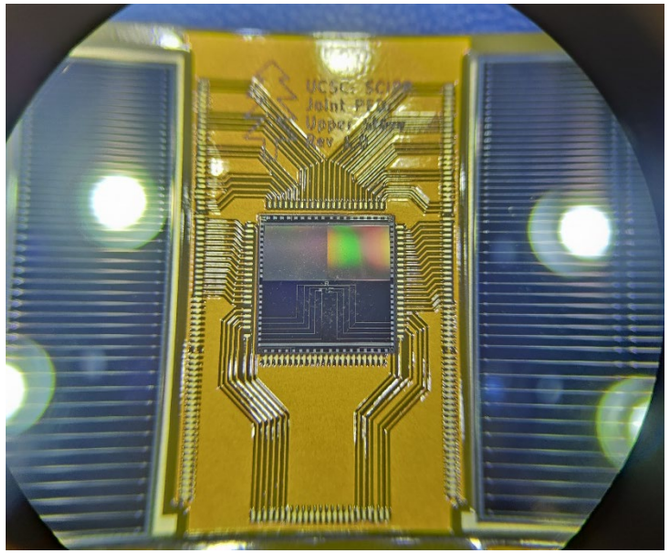
- Co-cure two halves of the stave with FPC
- Glue stavelets on stave
- Wirebond stavelets on to FPC
- QC on half stave?
- Assemble two halves with cooling pipe in between
- QC on full stave
- Assemble in trays

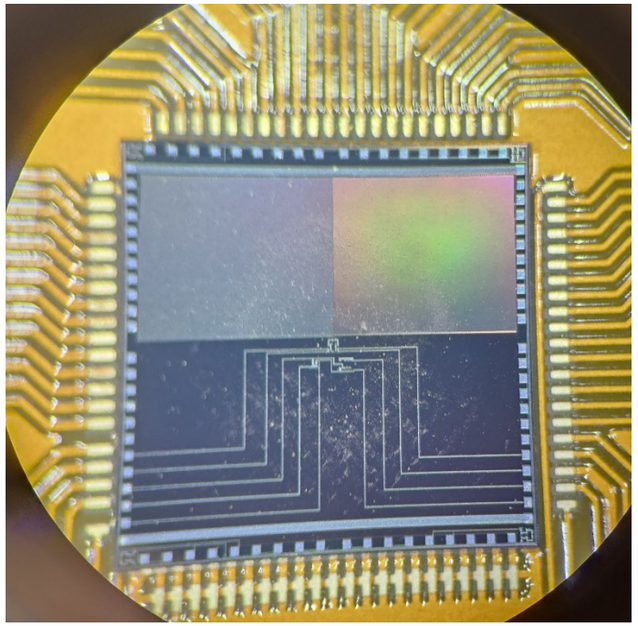
Stavelet demonstrator - 2025

- Plan to demonstrate the assembly procedure and study the thermal characteristic of a stavelet
- First prototype of interposer board produced
- Using non-working detectors from the HPK production
- Si heaters to simulate ASIC
- Fully load a double-sided stavelet with active pipe cooling and check thermal dissipation in prototype





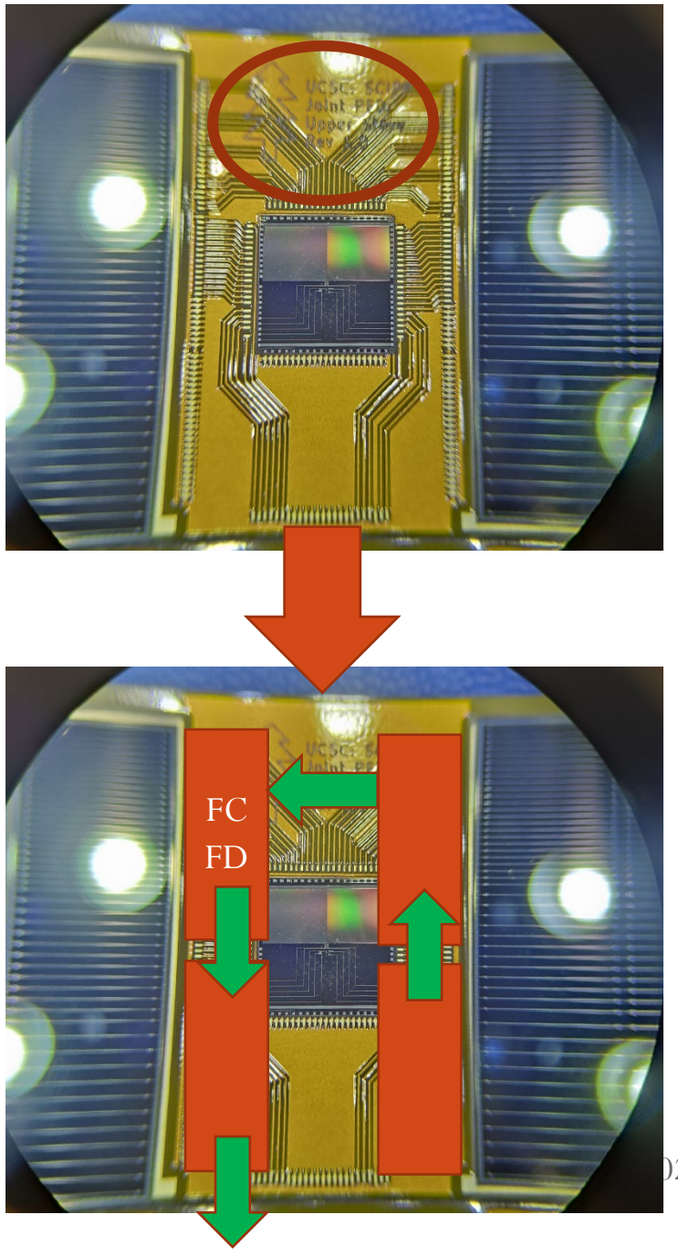




Discussion with FCFD developers

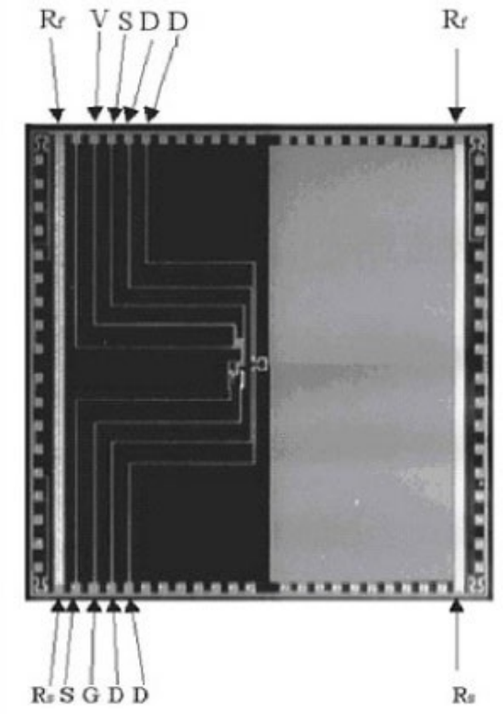
- Fan-in lines can be an issue for the chip readout, degrade the signal and introduce extra capacitance
- Solution: use 4 chips per 2 half-sensors, long and narrow with same pitch as sensor
  - Direct connection to sensor
- 4 chips will be condensed in only one set of lines, no increase in connections

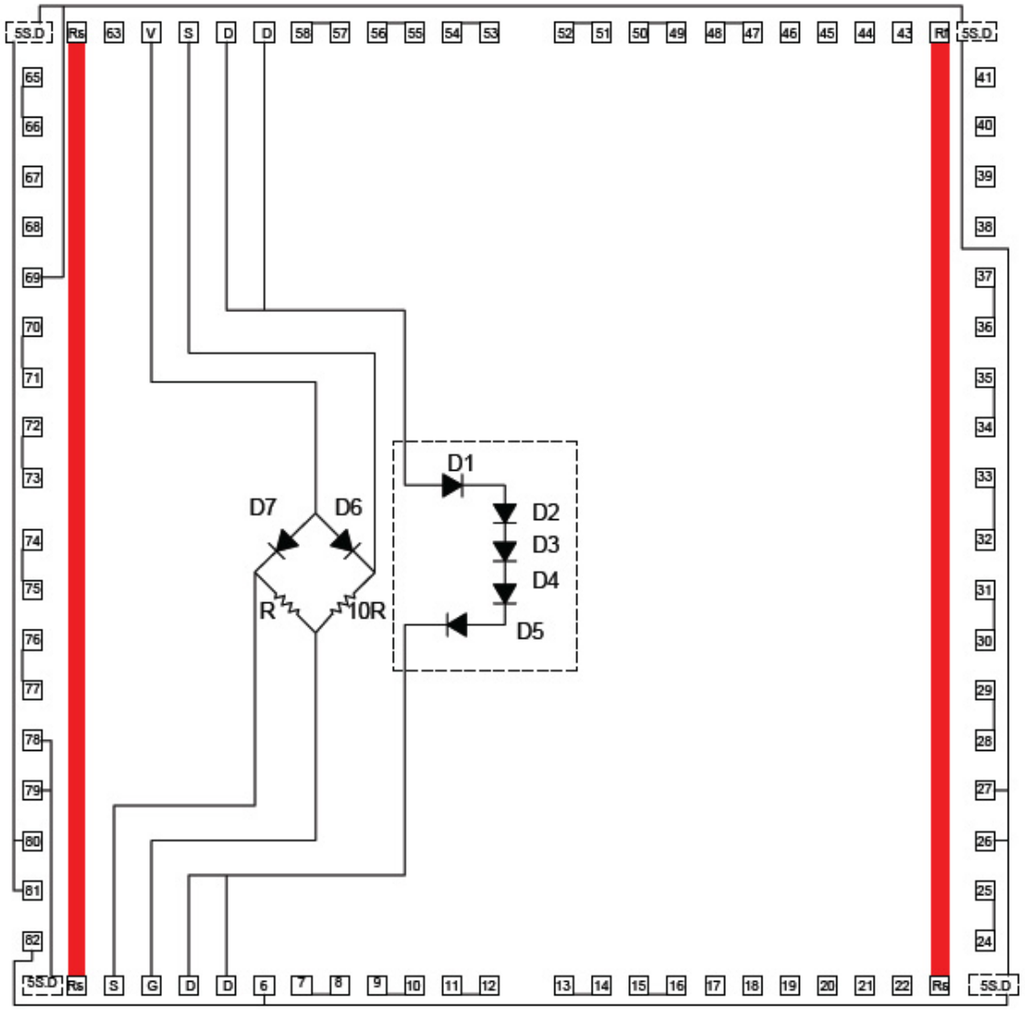
- Stavelet design remains the same, we can't split in the middle the interposer (need lines between chips)



Test Si heater

- 1x1 cm size, 20 in SC right now
- 9 needed for the design
- Each one need 1 line for heaters and 5 (?) for sensors
- Has 2 sensors, one for absolute (less precise) and one for relative (more precise)

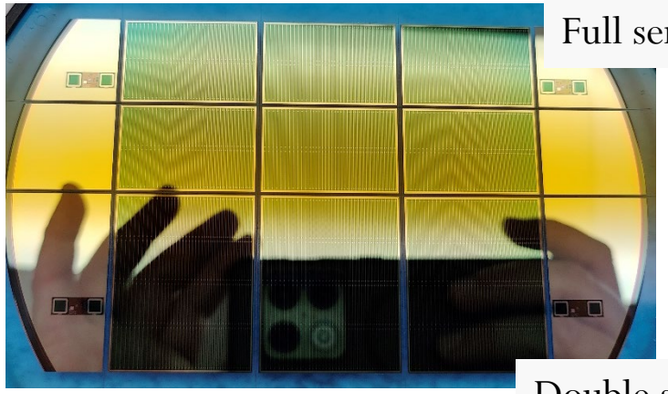




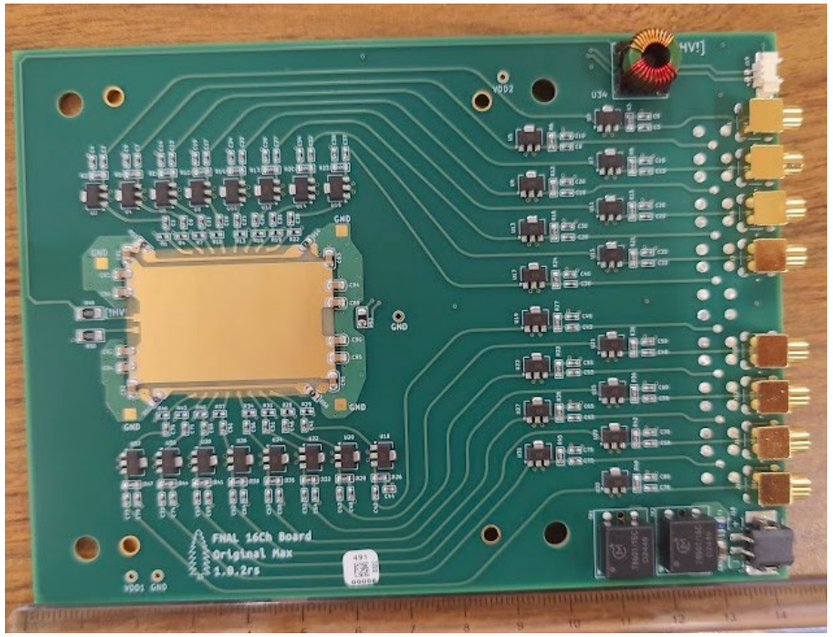
HPK AC-LGAD strip production

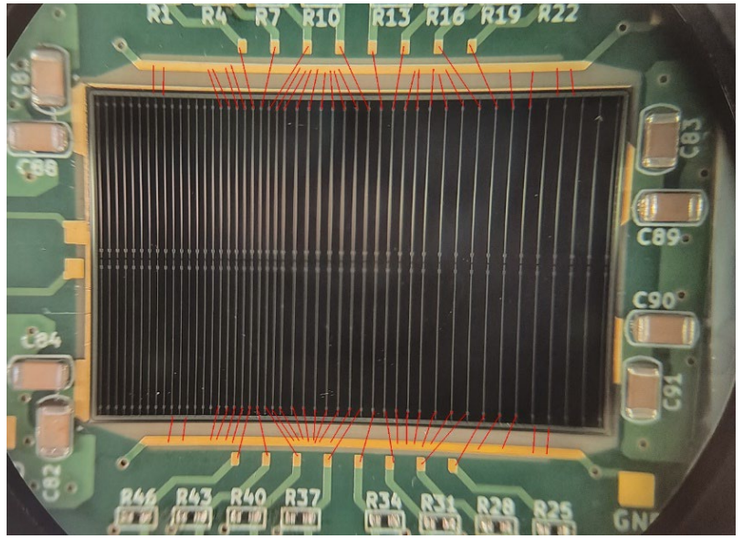
- ePIC full-size production of HPK strip AC-LGADs with devices up to 3.2x4.2 cm
  - Nominal size 3.2x2.2 cm with 1cm strip ‘segments’
  - Strip width: 40-50um, strip pitch 500, 750, 1000 um
- 8 wafers in hand, four 50um thick and four 30um thick

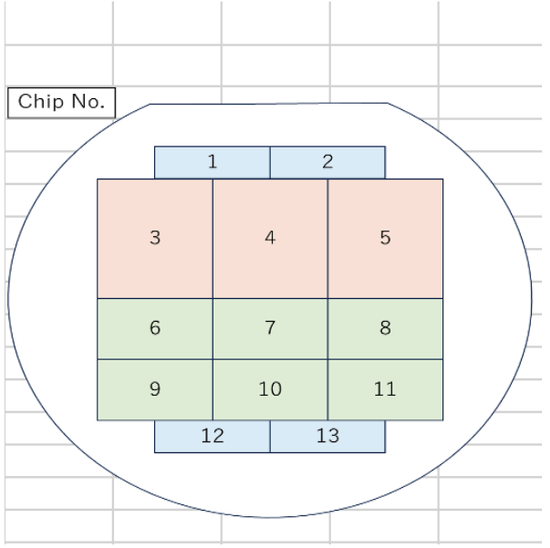

Half sensors


Full sensors

Double sensors

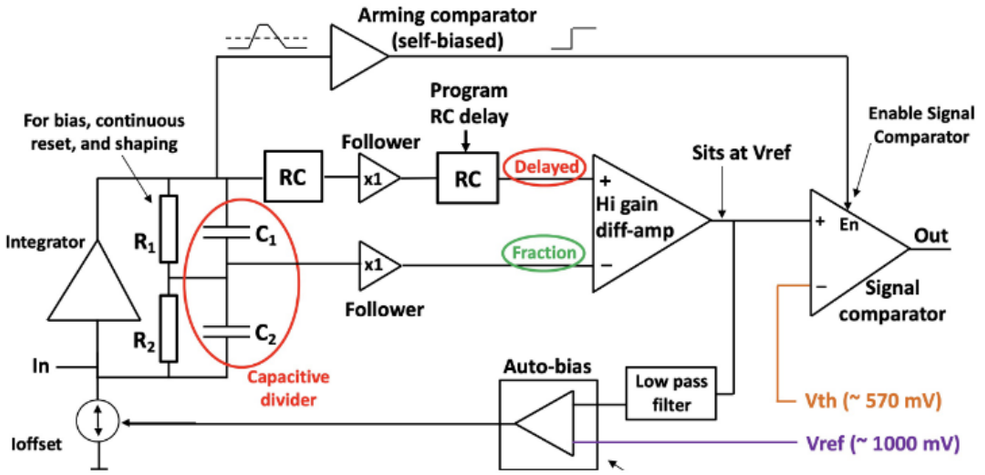


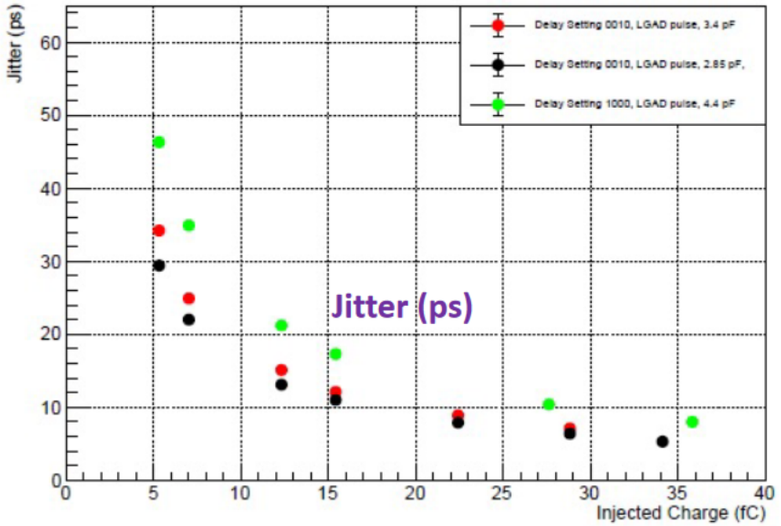




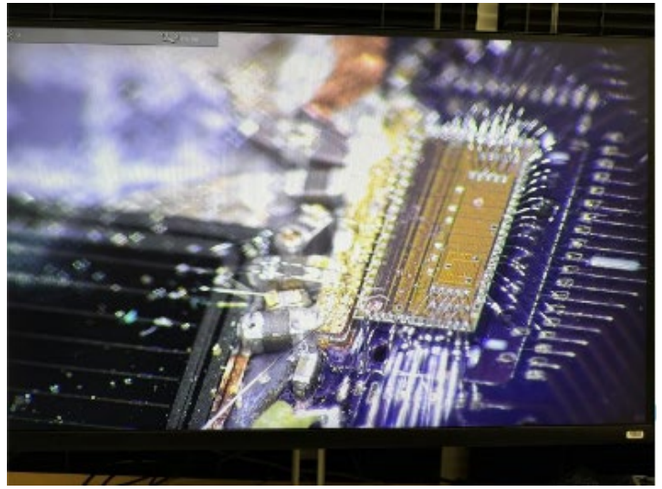
AC-LGAD strip readout – FCFD (FNAL)

- AC-LGAD strip readout developed at Fermilab
  - Can accept high input capacitance o(10pF)
  - Target Jitter <10ps
- FCFDv1 – 6 channel received Jan 2024.
  - Tested at FNAL in May/June 2024, AC & DC-LGAD (1 mm):
- DC-LGAD @ 50 ps; AC-LGAD @ 52 ps
- AC-LGAD should get ~35 ps with improved comparator.
- **FCFDv1.1 –TSMC May 2025; DESY tests in July 2025.**





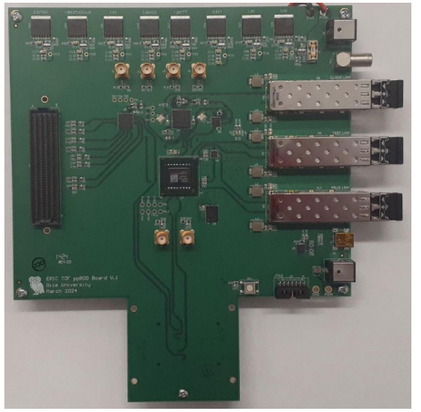
- 128 ch strip readout
- 65 nm CMOS
- Constant Fraction Discriminator
- Plus TDC, ADC, interfaces
- Cdin: <15 pF
- Dynamic Range: 5-40 fC
- Timing: 10-30 ps
- Links: ~Gbps, multiple
- Radiation tolerant.



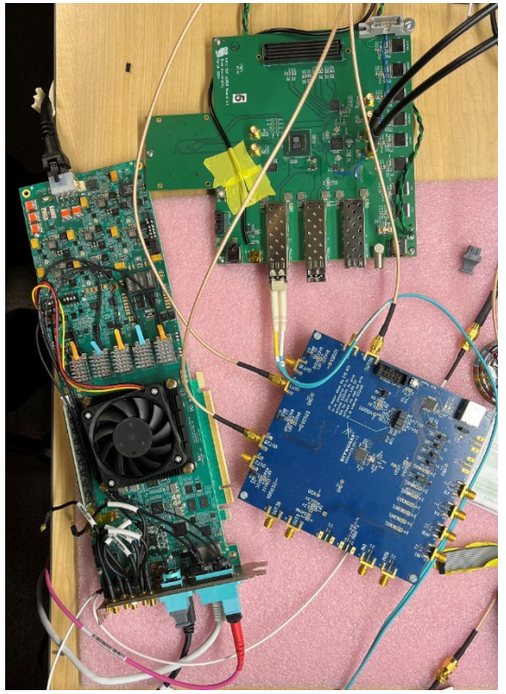
High Precision Clock Distribution

- ppRDO – pre-prototype Readout Board:
  - Generalized to allow readout from various ASICs – FMC connector
  - Xilinx Artix+ FPGA (low cost, CERN TCLink compatible)
  - Clock Jitter cleaner – 5 ps
  - Clock recovery on Rx of SFP or direct clock on dedicated fiber
  - Establish procedures to readout ePIC's ASICs prototype PCBs
  - Develop common streaming readout scheme with DAQ's protocols
  - Platform for radiation tests (SEU measurement and handling)

- Produced and tested 6 PCBs.
  - Jitter measured at 3 ps (Ref clock – FLX182 Tx serializer – ppRDO)



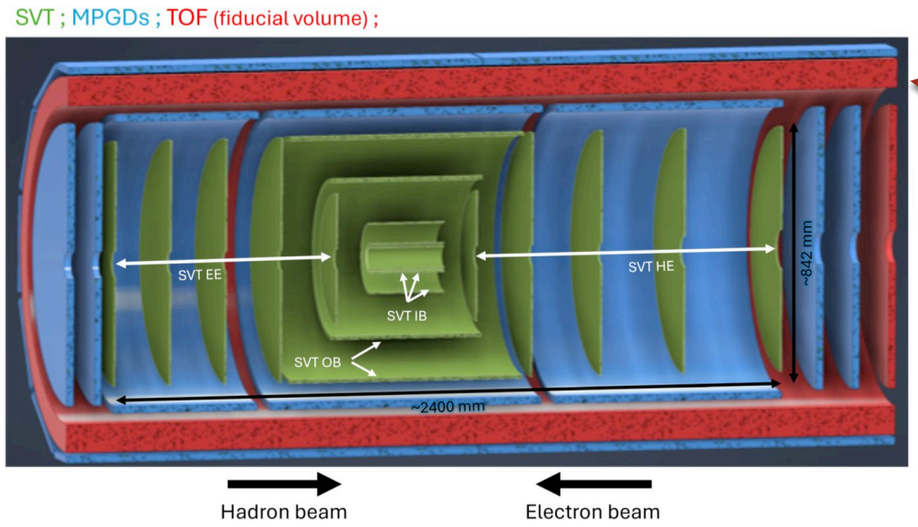
ppRDO
(ADCLK944)



Si5344H
(ref Clock)

FLX182

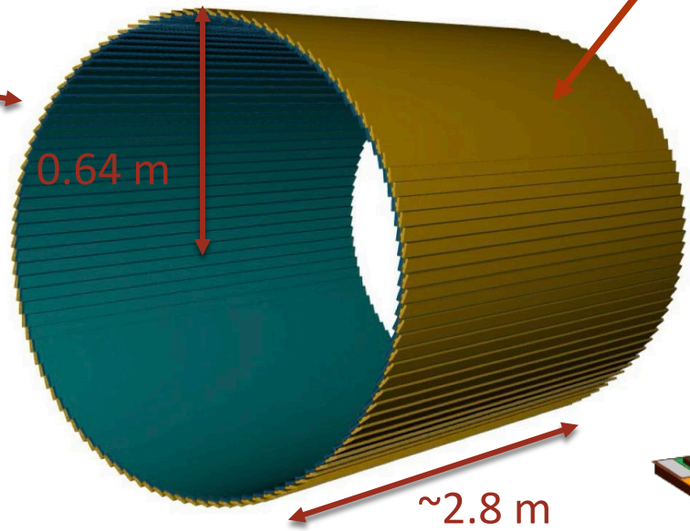
Barrel-**TOF**

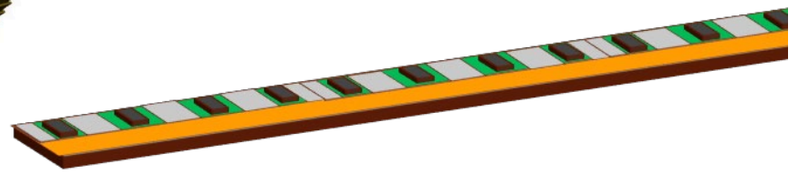


Staves mounted in 'trays' that can be removed for servicing

Barrel-TOF (BTOF)

144 x Staves

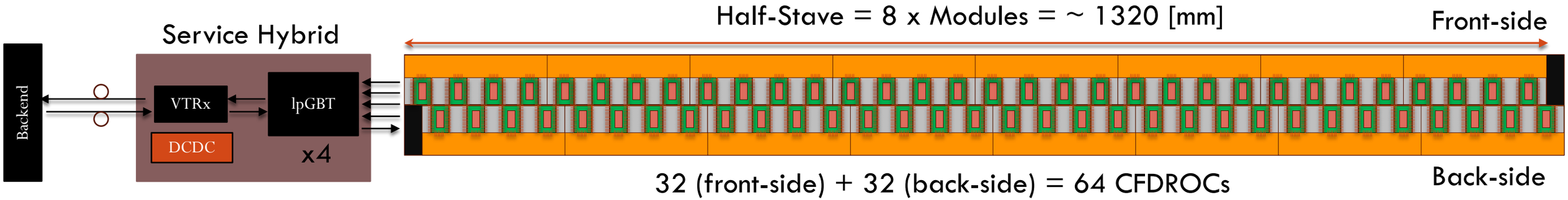




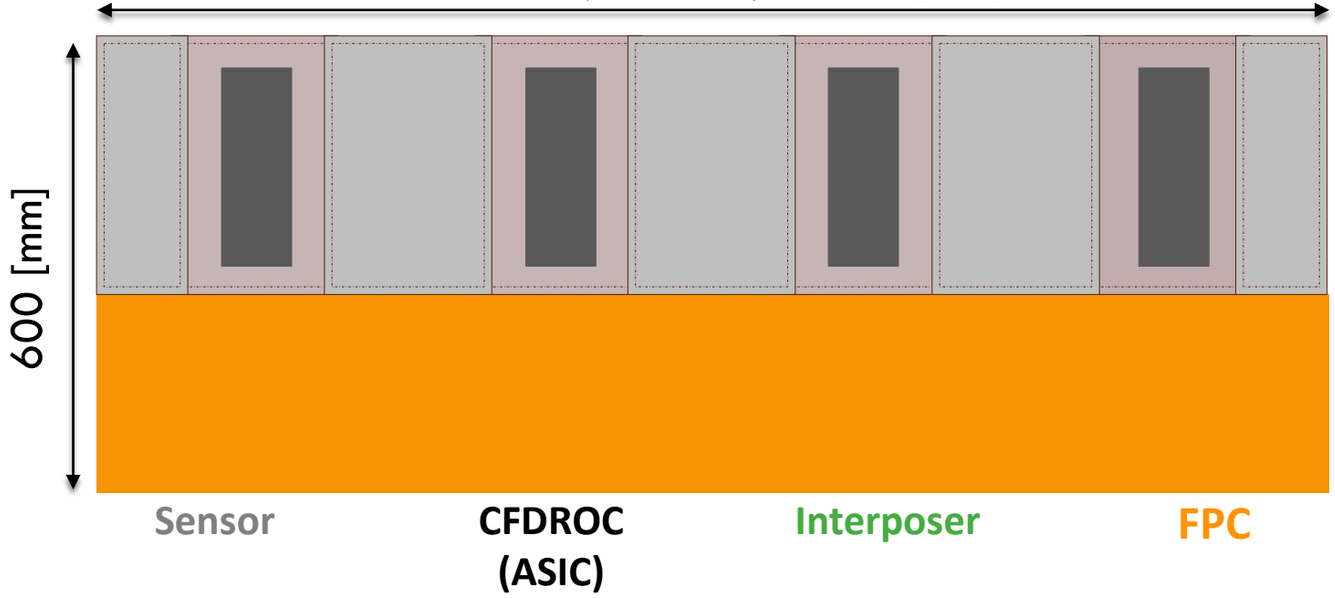
-1.33<η<1.74

- The ePIC AC-LGAD TOF is PID, tracking and background rejection detector for mid-rapidity (BTOF: -1.33<η<1.74)
- Cylindrical shape is composed of 144 tilted staves (288 half-staves)
- Strip-type AC-LGAD sensor is used to meet the requirement of ~35 ps and ~30 um timing and spatial resolution respectively

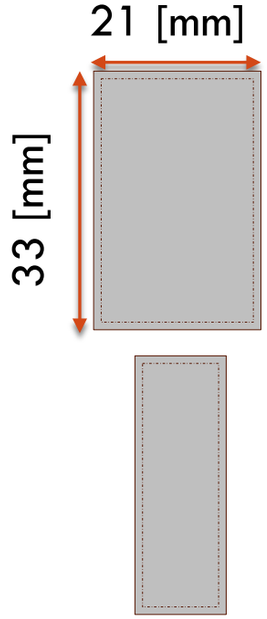
Data Transmission



32 (front-side) + 32 (back-side) = 64 CFDROCs



8 x 2 x 288
=4608



3 x 8 x 2 x 288
=13824

2 x 8 x 2 x 288
=4608

$X/X_0 < 3\%$ (including support structure)