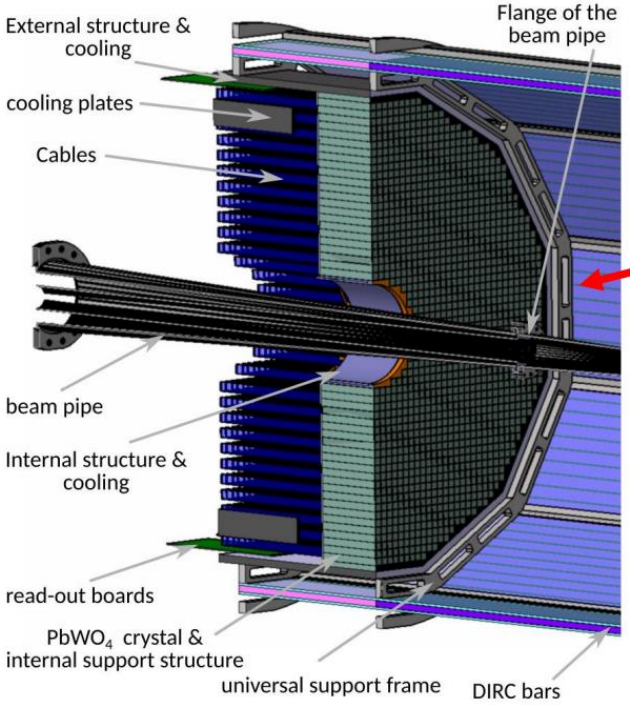
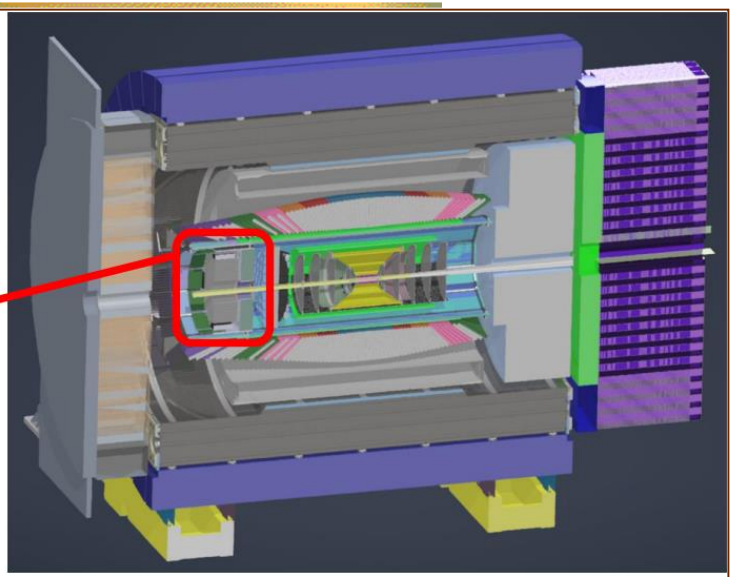
CALOROC FEB for the EEEMCal

O. Le Dortz, Yoann Le Roux (LLR, Palaiseau, France)

January 2026 ePIC Collaboration meeting
CALOROC Session

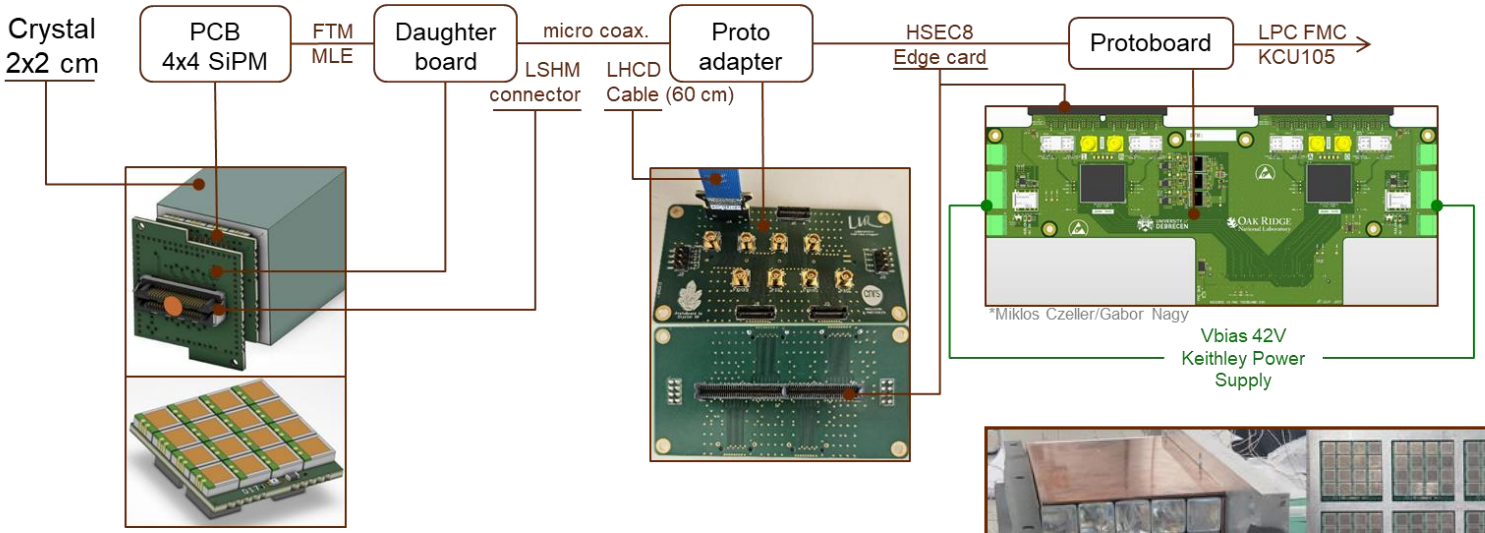
The context: EEEMCal

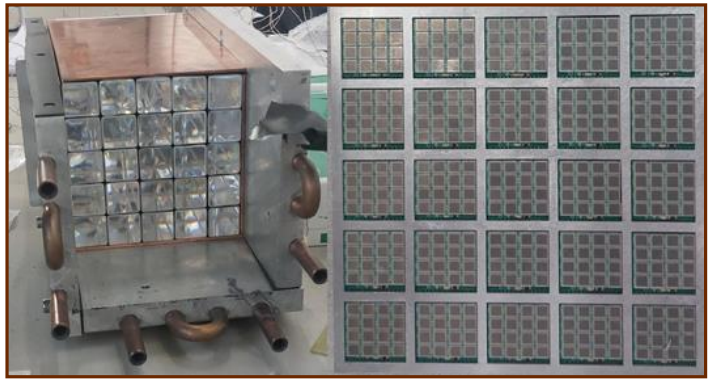




- 2932 lead tungsten crystas
- Scintillating light read out by SiPMs
- Temperature controlled detector (cristals + SiPM): ± 0.1°C
- Calibration/monitoring system: fibers + laser/LED

Initial prototype, with HGCROC and ORNL Protoboard





- 16 SiPM channels per crystal
- 1 HGCROC, SiPM individual readout => 4 crystals, 64 channels
- 1 Protoboard/KCU module => 8 crystals

NB: High SiPM capacitance (500pF). HGCROC not adapted to read merged channels from several channels

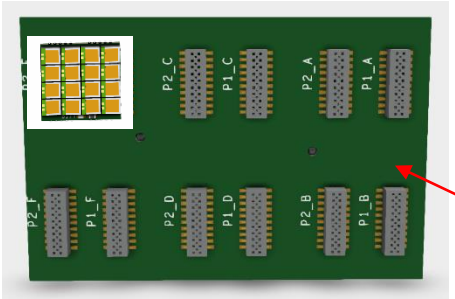
Adaptation to CALOROC

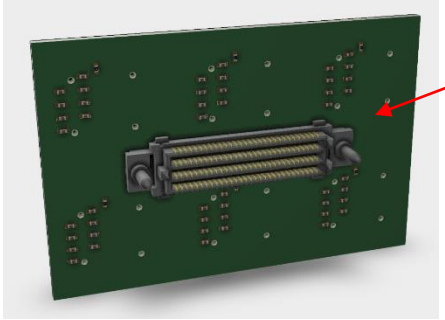
- Requirements
  - CALOROC A/ CALOROC B
  - Have some flexibility to test individual SiPM readout or merged channels (possible with CALOROC B, but still to be validated)
  - Being able to reuse the original SiPM matrices PCB
  - Accommodate with the challenging mechanical constraints of the calorimeter (2x2 cm^2 for 16 channels) With the original design, a lot of cables required

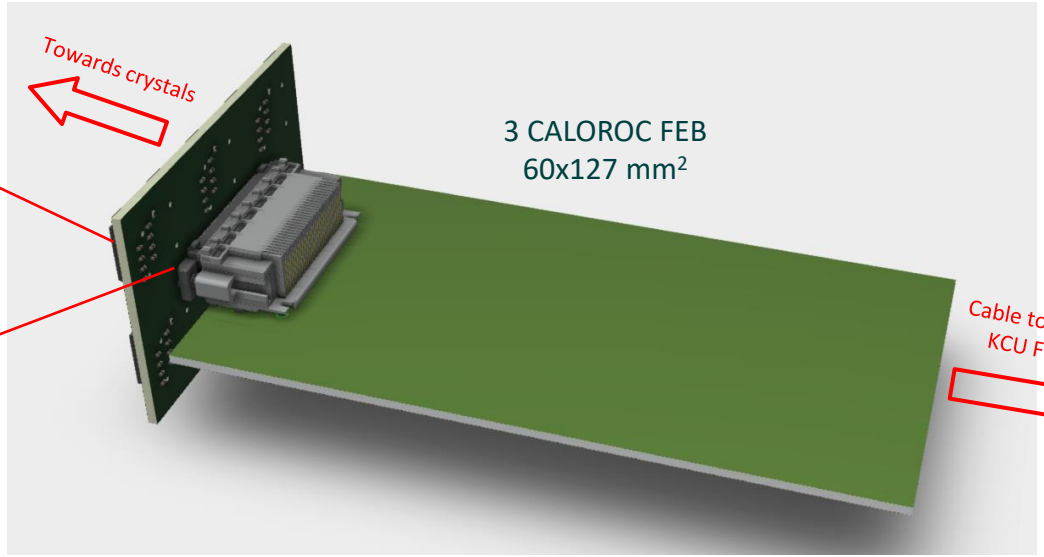
- At a first step, CALOROC digital IO lines (CLK, FCMD, output data links) carried on copper, but with a modularity close to what the lpGBT offers:
  =>1 lpGBT ⇔3 32-channel CALOROC ⇔ 96 individual SiPM channels / 6 crystals

Adopted solution

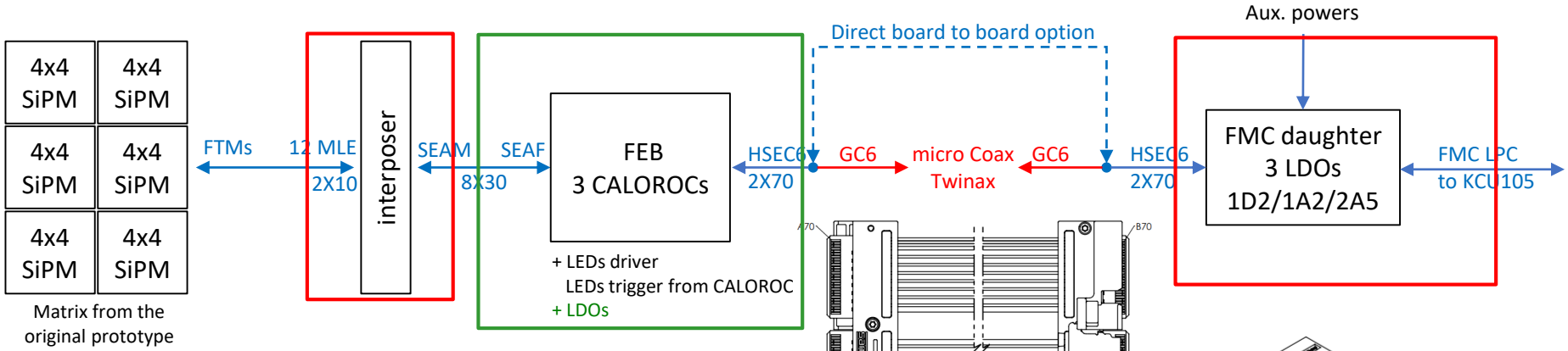
Interposer board : 62x41 mm^2

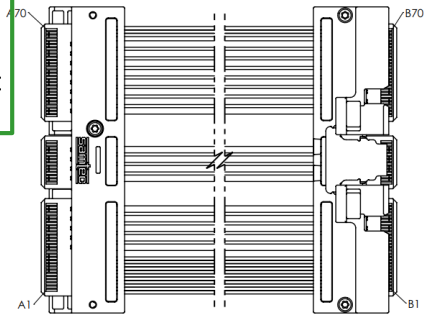


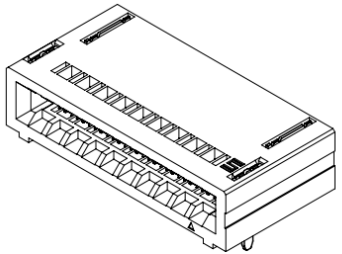




System Overview





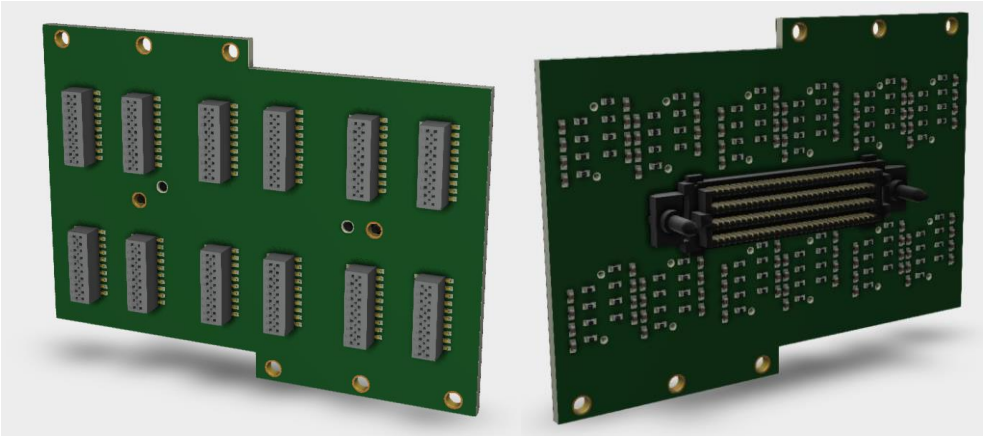


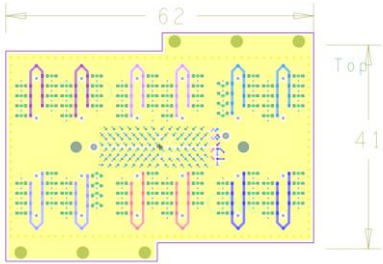
GC6 cable 70 pins/row, HSEC6 right angle

- Interposer ⇔ FEB: High density connector couple
- FEB:
  - 3 CALOROC / 96 channels
  - Power: local LDO or from cable 1.2A, 1.2D, 1.2/2.5A_PAD
  - 6 LED drivers to individually control the LEDs on each crystal (command from the KCU/FMC)
- FEB⇔FMC:
  - micro-twinax lines
  - power lines
- FMC daughter board: 1 slot width

Boards Status

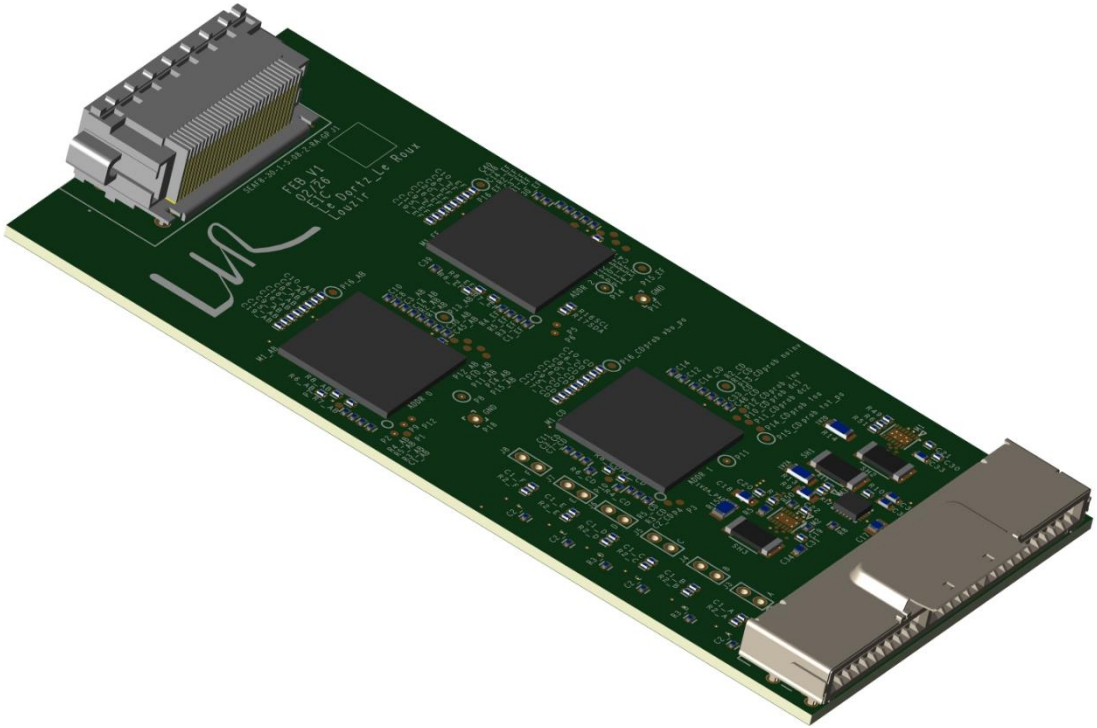
- Interposer: PCB received, ready to be sent to assembler (5 units)





Boards Status

- Interposer: PCB received, ready to be send to assembler (5 units)
- 3 CALOROC FEB: Design finished, ready for PCB production (5 units)



Boards Status

- Interposer: PCB received, ready to be send to assembler (5 units)
- 3 CALOROC FEB: Design finished, ready for PCB production (5 units)
- FMC Daughter board:
  - Design underway
  - Main features:
    - Some extra power distribution
    - Cable to FMC signals interconnections

Control Firmware and Software

- Compatible with the KCU105 firmware developed by Miklos for the Protoboard, with minor modifications
  - Production of 3 CLK/FCMD outputs
  - Common I2C for the 3 ASICs. But slightly differs from the HGCROC I2C scheme
  - LED drivers to implement: 1 fast pulse + 6 enables
  - Output data links frames have variable word sizes

- In the meantime, at LLR, we are developing a firmware derived from some versions used at Omega for ASIC characterization.
  - Scheme common with the FW used to characterize the CALOROC ASICs
  - Can then benefit from all the software developments written at LLR and Omega with previous ASICs
  - For now, 1 GBE control link (IPBUS based), 10 GBE version foreseen

Conclusion

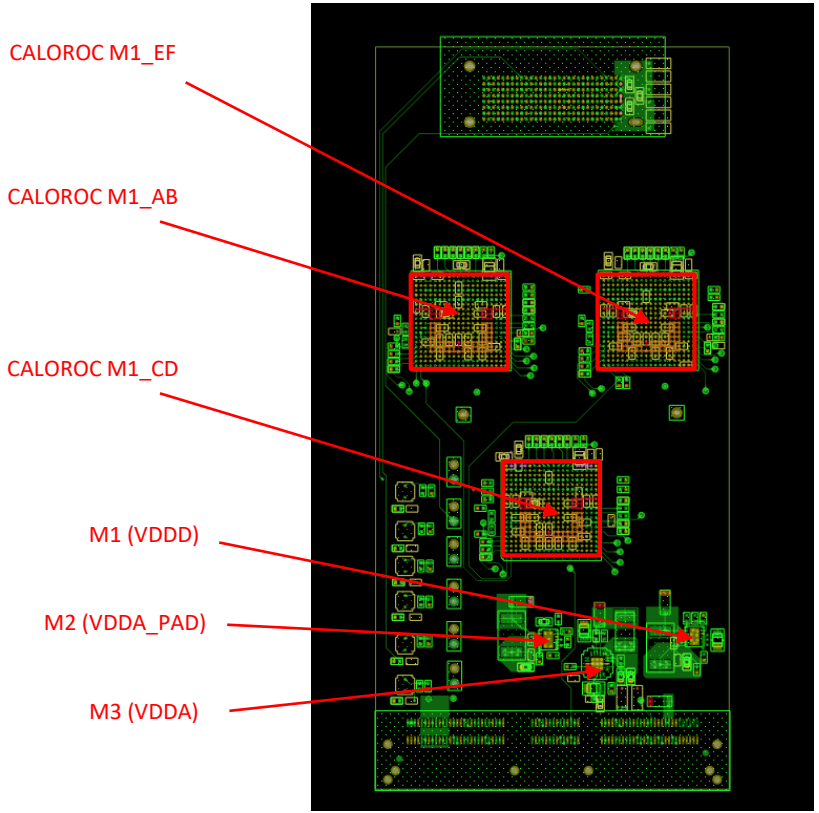
- Waiting for the budget to be received.
  This front-end system is expected to be ready when some CALOROC ASICs are available for assembly (after test by the Omega team: spring ‘26)

- This system is a new step forward but not the final design:
  - We still need to validate the final adopted channel modularity
  - Some mechanical aspects still to improve (especially on the detector edge and close to beam)
  - This will depend on the performance of the CALOROC B ASIC, more suited for high capacitance SiPMs

Extra Slides

Consumption and Thermal Studies

- Components consuming some power:
  - 3 CALOROC : M1_AB, M1_CD, M1_EF
  - 3 Voltage regulators : M1, M2, M3
- Power supplies:
  - 1.2V A, 1.2V D
  - VDDA_PAD :
    - 2.5 V for CALOROC A
    - 1.2 V for CALOROC B



CALOROC Consumption

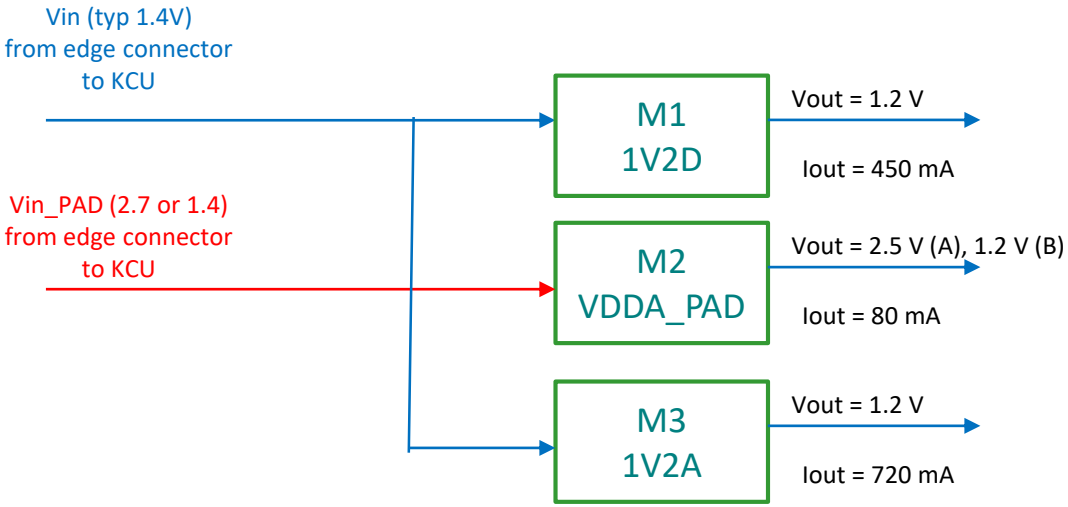
CALOROC A	Volts	mw/chn	Pdis (W)	Current	Count	Tot Current
1V2D	1.2	5	0.180	0.150	3	0.450
VDDA_PAD	2.5	2	0.072	0.029	3	0.086
1V2A	1.2	8	0.288	0.240	3	0.720
Total			**0.540**			

- 36 channels per CALOROC
- Data from Frédéric Dulucq, but 1.2V Digital probably overestimated

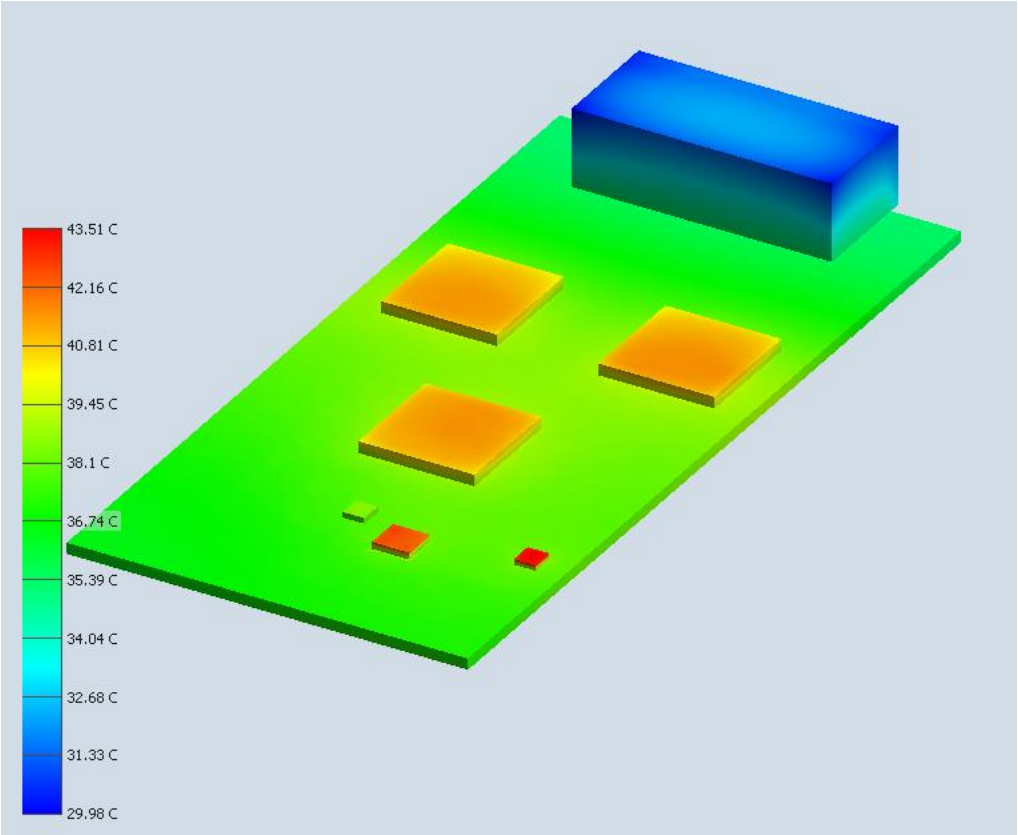
~540 mW or less power dissipation per ASIC

Power Scheme

- 2 power lines from the FEB⇔FMC Cable



Thermal studies, (no cooling, ambient air temp)



Thermal studies, (no cooling, ambient air temp)

Reference Designator	Dissipation + PowerLoss (W)	CaseTopDissipation (W)	CaseSideDissipation (W)	PCBDissipation (W)	Junction (C)	Case (C)	Board (C)
J1	0.000000	0.047659	0.150372	-0.198032	35.686185	32.358739	35.522059
M1	0.090000	0.002260	0.002564	0.085176	43.514072	43.514072	38.579785
M1_AB	0.540000	0.051075	0.025697	0.463228	41.453643	41.453643	39.406277
M1_CD	0.540000	0.051510	0.025983	0.462508	41.553693	41.553693	39.393694
M1_EF	0.540000	0.051445	0.025901	0.462654	41.578820	41.578820	39.574894
M2	0.017000	0.001666	0.002125	0.013209	38.648441	38.648441	37.951606
M3	0.144000	0.005390	0.004963	0.133646	42.730639	42.730639	39.616153