Nine chip module test & beam test prep.

BIC Wafers, Modules & Staves Meeting

2026/2/2

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For the upcoming beam test

- Available AstroPix Setup
  - Single chip/ three quad-chips/ one nine-chip module
  - 1 GECCO+FPGA / 1 HV board+ASTEP board (one HV board and two(or three) ASTEP boards available)
  - V3 Single chip + GECCO / three layers of Quad-chips + ASTEP / nine-chip module + ASTEP

  → Need more **HV board**: Sanghoon working on assembling HV boards and ASTEP boards.

  → Only one ASTEP setup available, can we use this upcoming beam test?
- What's the limitation on our current ASTEP setup?
  - Readout speed, count rates (→ Good to discuss with Adrien and Dan)
- What's needed for the upcoming beam test? (short-term goal, FY2026)
- What's needed for the upcoming review? (long-term goal, FY2026)
  - Using RCDAQ, AstroPix (ASTEP) + Calorimeter (H2GCROC) → Synchronization!
  - AstroPix V3? V5?
  - AstroPix (ETC) ?
    - For v3? V5?
    - When is available? Can we use ETC for the upcoming beam test?
  - AstroLinx?
    - For v3? V5?
    - When is available? Can we use ETC for the upcoming beam test?

Why KEK beam test is important?

- Using three-layer of quad-chips
  - First aim to understand how AstroPix hit data are read out across chips and layers in a three-layer AstroPix system under the KEK beam condition (up to 2.3 kHz).
  - Since FPGA timestamps are assigned when AstroPix hit data arrives at the FPGA, I study whether hits across layers originate from the same particle using KEK beam test data.
  - Important step toward achieving precise synchronization with the calorimeter system in the upcoming beam test.

- Using three-layer of quad-chips with W plates placed between quad-chip layers
  - Observed that max buffer issues using three-layer of quad-chips with two W plates
  - Readout limitation about EM shower from electron beam

  →Need to improve readout speed

  → Chip-level design issue or ASTEP sw/fw issue?

Available AstroPix setup

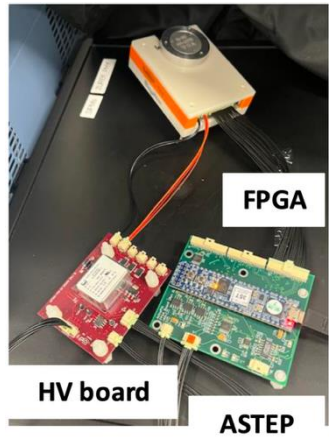
AstroPix

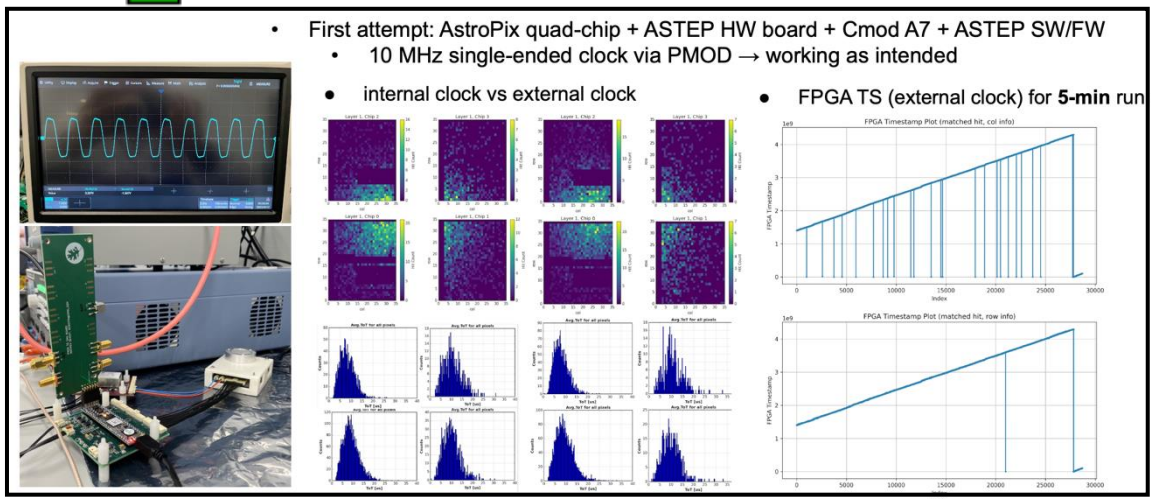
- Nine-chip Module
  - ✅ Only Module4 is working well.
  - Need to debug
    - Module1, 2, 3, 🟡 7, 8
- Quad-chip Module
  - Used in KEK beam test in Dec. 2025
    - ✅ W112q06
    - ✅ W101q04
    - ✅ W101q12(malfunctional chip0)
- Single chip
  - ✅ W06s01 (used in FNAL beam test in Jun. 2024)
  - ✅ W08s06

1. Test AstroPix using 40 MHz external clock
2. Test H2GCROC and AstrroPix using 40 MHz external clock

GECCO / A-STEP setup

- 1 GECCO+FPGA board available
  - Running with v4 chip currently
  - External clock didn't work well.
- **1 A-STEP setup** available
  - HV board + ASTEP board
    - ✅ Only **one HV board** available
    - ✅ **Two ASTEP board** available
    - One ASTEP board need to change FPGA board
  - Using external HV+ASTEP
    - Can't use it due to plenty of noise
  - ✅ **External clock** available





Current Status: Nine-chip module

- ✅ Module 4; working well.
  - After checking sampling clock (can be fixed with wire-bonding), configured up to 9 chips.
    - Last chip (chip8) is noisy and gives 0 ToT value (can be fixed with wire-bonding as well)
    - ✅ Mask maps ✅ Response to Sr-90 (for BIC review; Sep, 2025)
- 🟡 Module 7; Not fully working yet but at least communication with PC and all AstroPix chips
  - After checking sampling clock (Jan 16, 2026);
  - ✅ Respond to the injection voltage
    - 0 ToT value: chip 2, 5, and 8
- Module 8; Need to check sampling clock!

🟡 Module 7

Module 8

✅ Module 4

Previous nine-chip modules

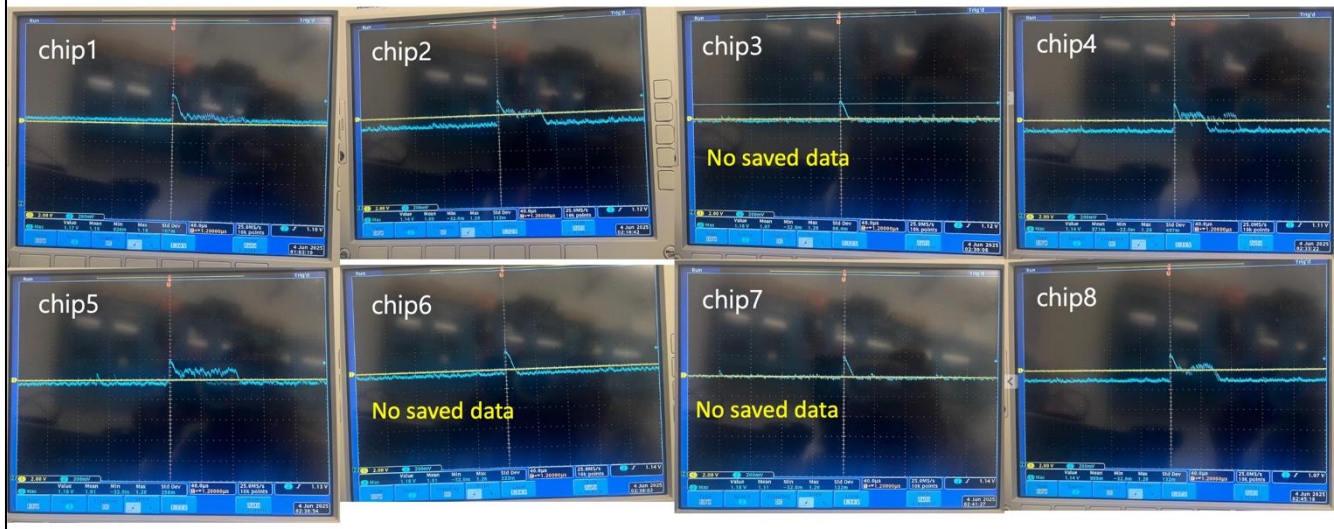
- Three more previous boards: should check wire-bonding and pads on PCB
  - With Kapton underneath chips
  - Without Kapton underneath chips
- Previous issue was about applying HV

Module 1

Module 2

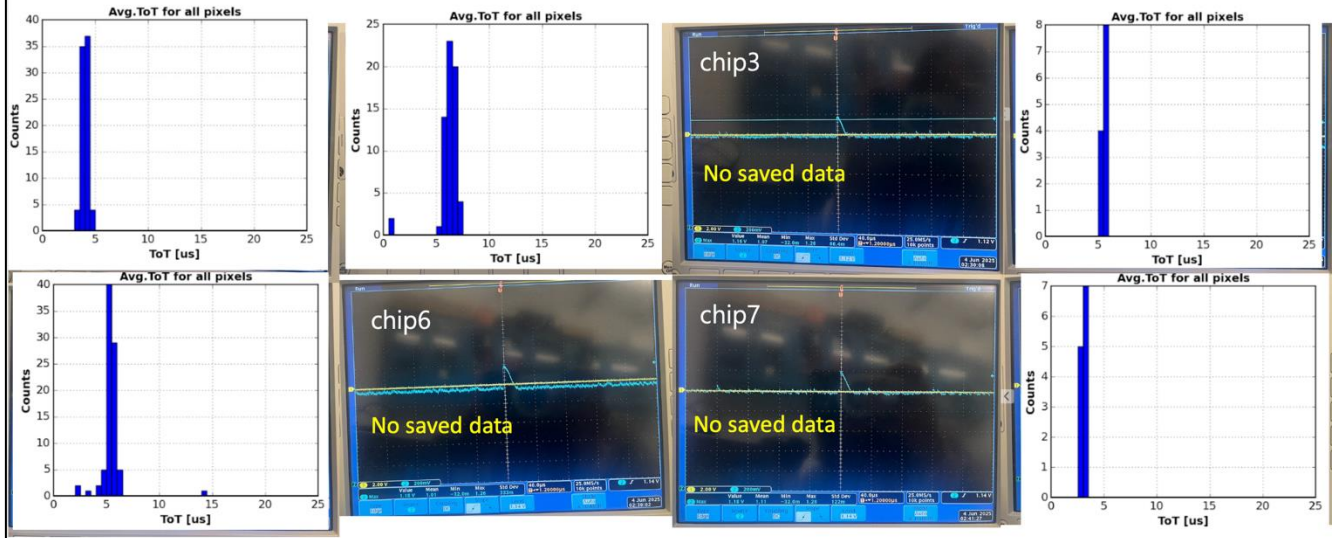
Module 3

9 chip PCB: Analog signal check (2) [col15, row0]



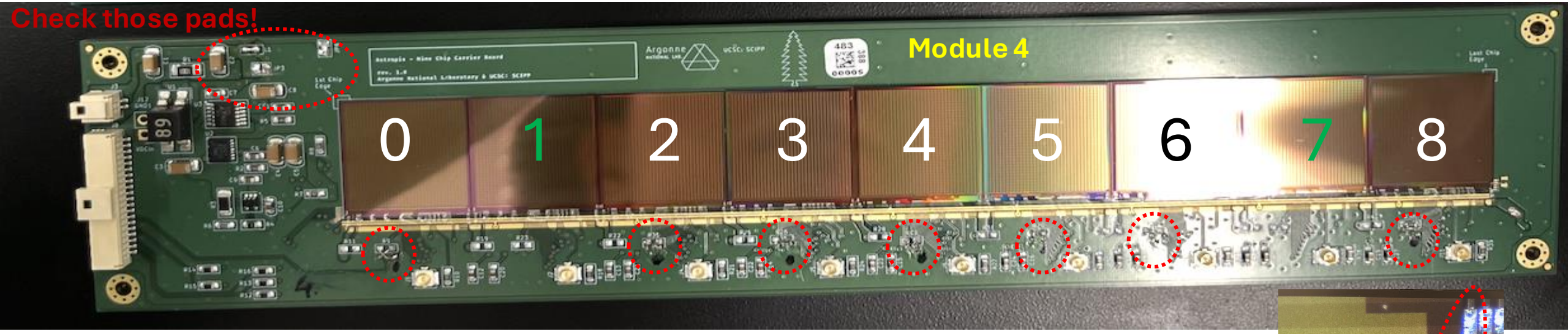
- Analog response plots for Chip 1–8, shown in order.
- Used threshold = 300 mV, Injection voltage = 600 mV

9 chip PCB: Analog signal check (3) [col15, row0]

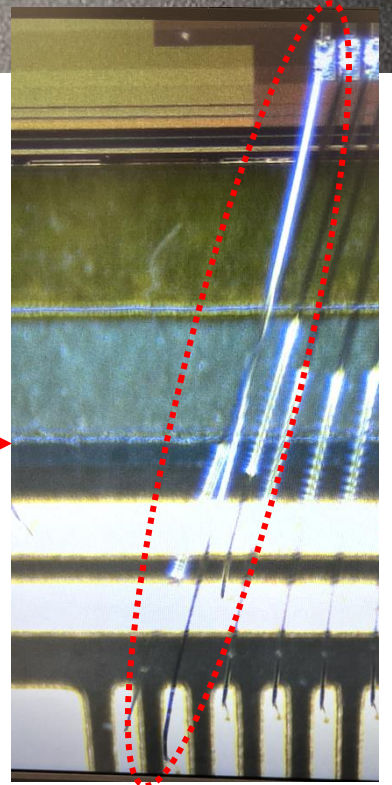


- Analog response plots for Chip 1–8, shown in order.
- Used threshold = 300 mV, Injection voltage = 600 mV

How to Modify Nine-Chip Module PCB (current version)



- At PCB design level, the sampling clock pads have been swapped on **Chips 0, 2, 3, 4, 5, 6, and 8 (except 1 and 7).**
  - In Module 4, the pad swap was implemented via additional soldering. (red circle)
  - After module 4, the pad swap on the assembled nine-chip boards was implemented via wire bonding.
    - The first and second sampling clock pads located in the middle of the chip.



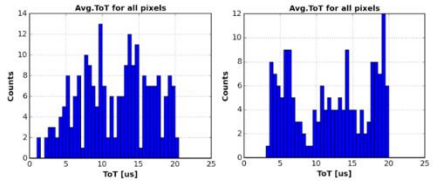
How to fix ToT value = 0 will be updated here

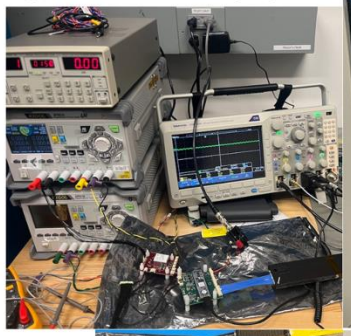
Issue using external HV

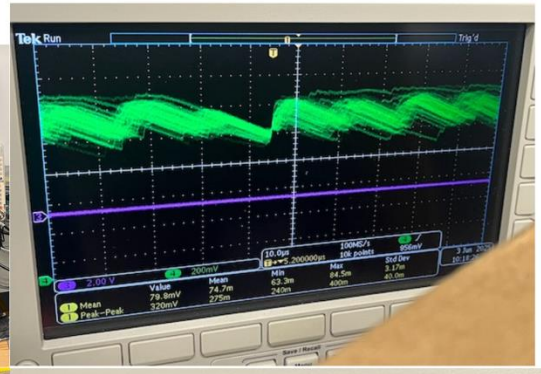
9 chip PCB: Analog signal check (1)

(top) external HV

- Unstable baseline: fluctuation ~ 300 mV
- Example of injection result (All results)

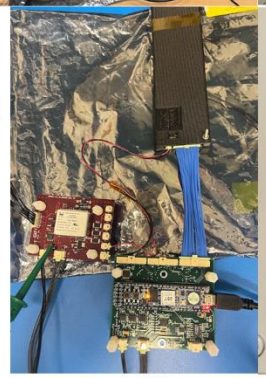


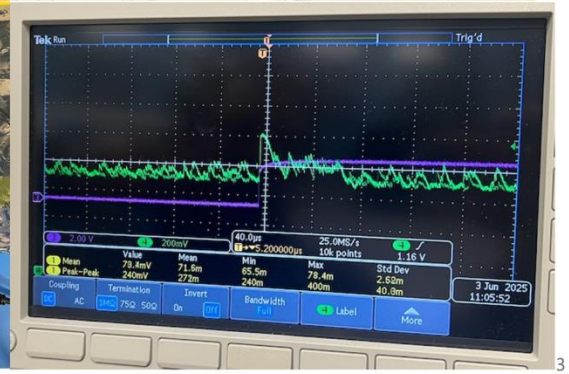




(bottom) internal HV

- Still unstable baseline but improved compared to before.
- Injection to 9 chip PCB worked and corresponding analog signals were observed.
  - But the signal amplitude was smaller compared to single-chip or quad-chip result





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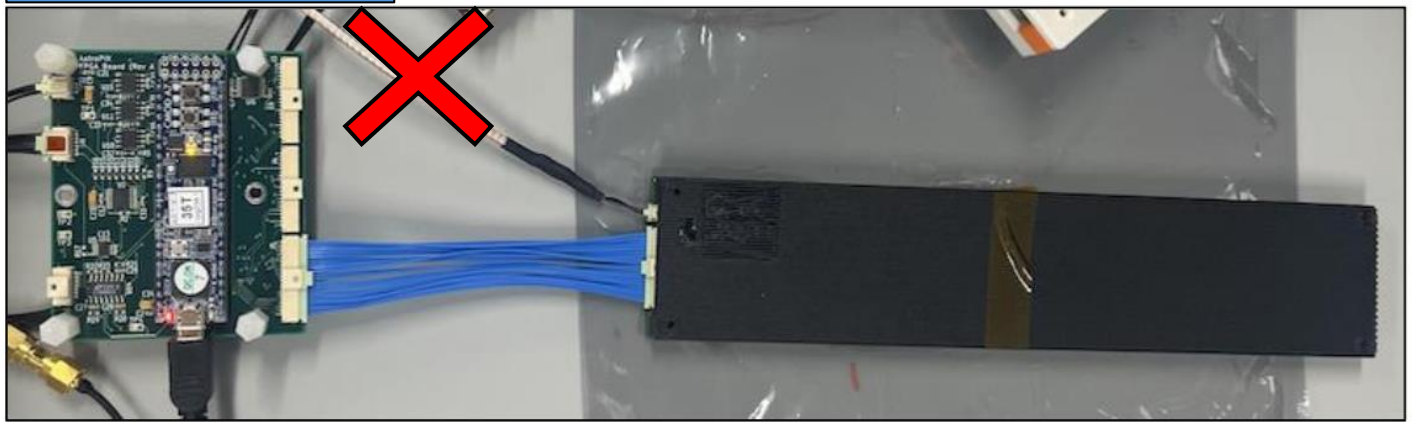
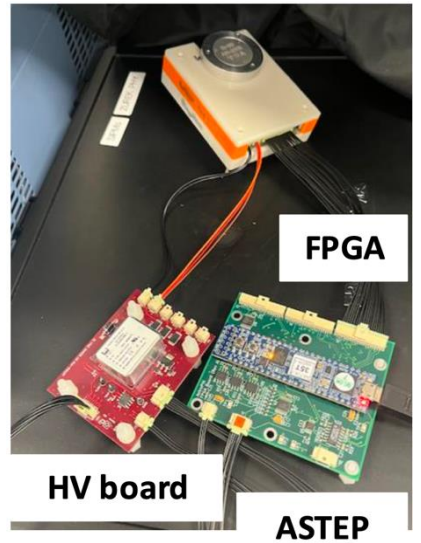
- Using HV board gives good results as expected.
  - Quad-chip/Nine-chip Module + HV board + A-STEP board setup
- **External HV** makes the max buffer issue.
  - Both quad-chip and nine-chip module
- Observed Quad-chip + GECCO setup didn't work; never got real data off of them with the gecco

→ Pretty sensitive to the grounding and having a separate HV supply with its own ground doesn't work well.

CAEN HV Supply





back up