Update on MPW1 testing: irradiation test at BNL

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WP2

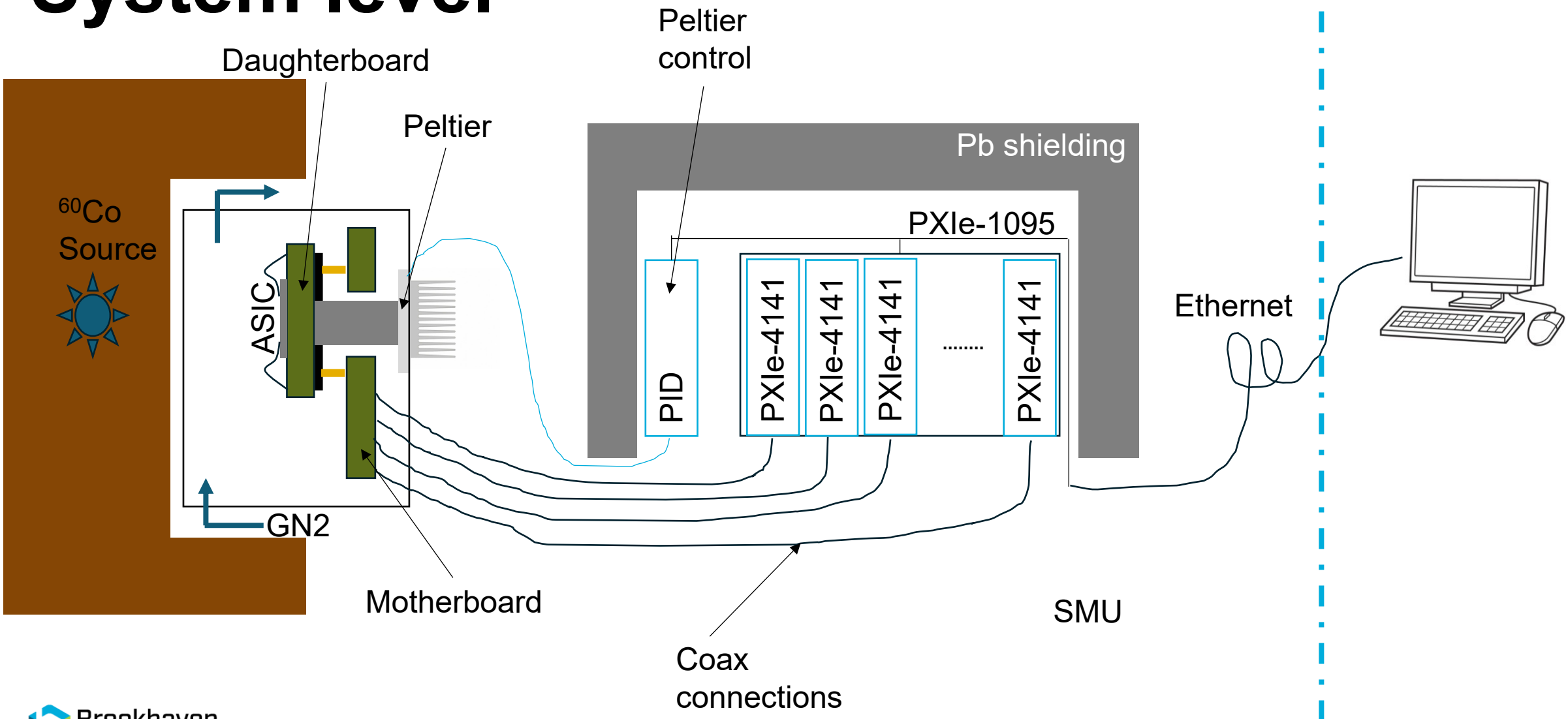
Outline

- Test setup
- Test facility and calibration
- Readiness and plan for test preparation
- Plan for testing
- Summary

Conditions and specs

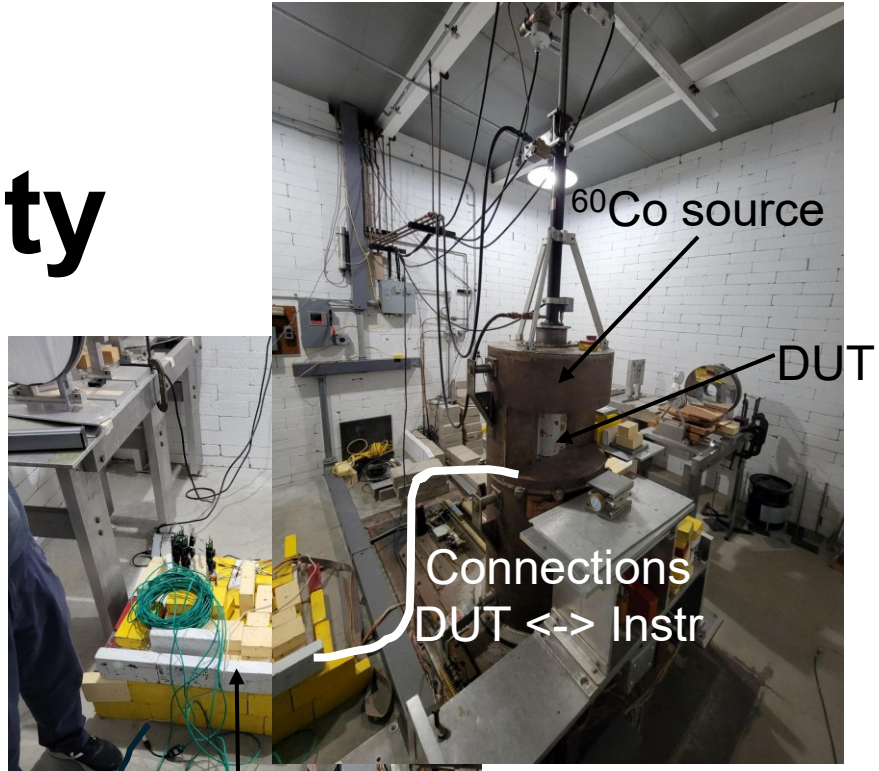
- Irradiating 3 chips per conditions:
  - Temperature= RT, 40 C and 0 C
  - ON and OFF status
- 18 chips to test
- Irradiation rates ~20 krad/h
  - Assuming TID~ 2-3 Mrad
  - 1 Chip <-> 5 days of testing
- Measurements will be live and continues (depending on dose steps)

System level

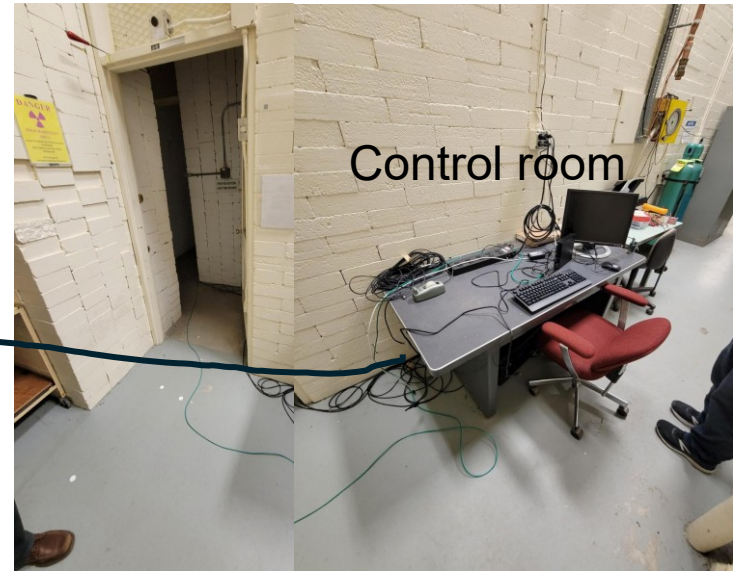


Irradiation Facility

- Three main areas:
  - Irradiation area (1173 keV, 1333 keV)
  - Shielded instruments in irradiation area
  - Control area



Control and data transmission



^{60}Co activity calibration

- The Co-60 sealed source had an expected activity of 302.8 Ci on 11/5/2025
- The goal is to measure the TID as function of distance
- TL dosimeters are utilized to measure dose at different positions:
  - Vertically at 5.5 inches to the base (~ center of aluminum cover)
  - Horizontally: 1/4-1/8”, 1”, 2”, 3”

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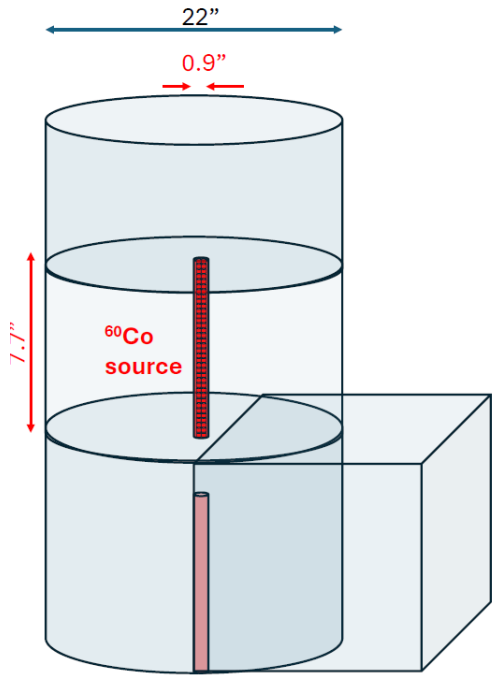
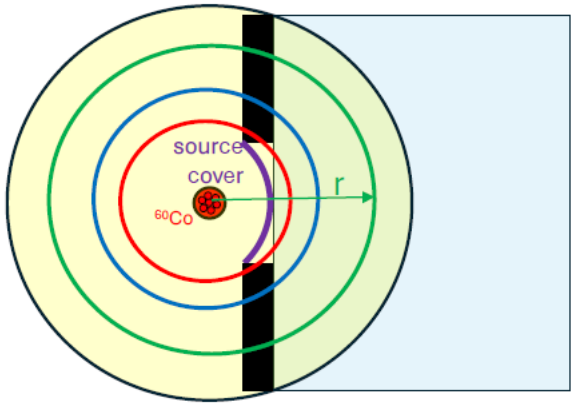
^{60}Co activity calibration

- The TLD are exposed for different times at different position, with the goal to reach about 500 rad in each spot





Irradiation Time (sec)	Dose (rad)	Dose Rate (rad/hr)	Distace from Al cover
60	501.6	33348	1/8 - 1/4 inch
90	519.1	**23008**	**1 inch**
153	611.8	**15951**	**2 inch**
225	580.9	**10298**	**3 inch**

- Accuracy ~7%
- ePIC requirement is 1 Mrad → 3x safety factor
- At 1” rate = 23 krad/h → 3 Mrad are equivalent to 5.5 days exposure

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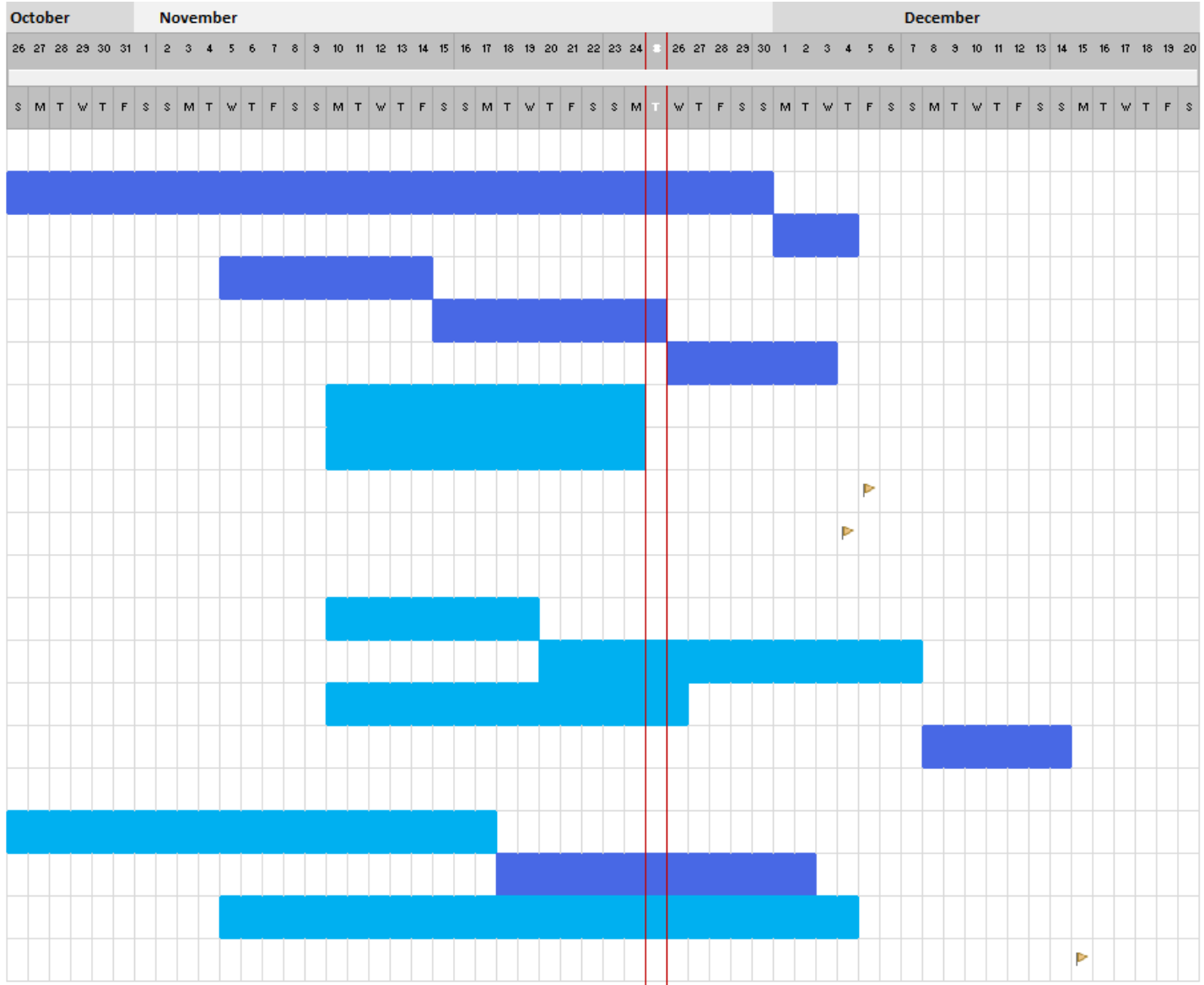
Test stand status

Project start date: 11/25/2025

Scrolling increment: -30

Milestone description	Category	Assigned to	Progress	Start	Days
PCB Design Group					
Daughterboard Purchase	Med Risk	J. Pro	90%	10/3/2025	59
Daughterboard Assembly	Med Risk	HDI	0%	12/1/2025	4
Motherboard Layout	Med Risk	J. Pro	100%	11/5/2025	10
Motherboard Purchase	Med Risk	J. Pro	100%	11/15/2025	11
Motherboard Assembly	Med Risk	HDI	0%	11/26/2025	8
Daughterboard Components	Low Risk	J. Pro	100%	11/10/2025	15
Motherboard Components	Low Risk	J. Pro	100%	11/10/2025	15
Daughterboard delivery	Milestone		0%	12/5/2025	1
Motherboard delivery	Milestone		50%	12/4/2025	1
Mechanics					
Purchase of mech components	Low Risk	E. Tamura / M. Keach	100%	11/10/2025	10
Mechanics mods	Low Risk	E. Tamura / B. Weldon	10%	11/20/2025	18
N2 pruchase/handling	Low Risk	E. Tamura	0%	11/10/2025	17
Commissioning	Med Risk	E. Tamura / N. Gallice / M. Pioti	0%	12/8/2025	7
Other					
SMU bid	Low Risk	L. Cultrera / S. Joshi	100%	10/21/2025	28
SMU PO	Med Risk	L. Cultrera / S. Joshi	50%	11/18/2025	15
Software development	Low Risk	P. Maj / N. Gallice	20%	11/5/2025	30
Start testing	Milestone	E. Tamura / N. Gallice / M. Pioti	0%	12/15/2025	1

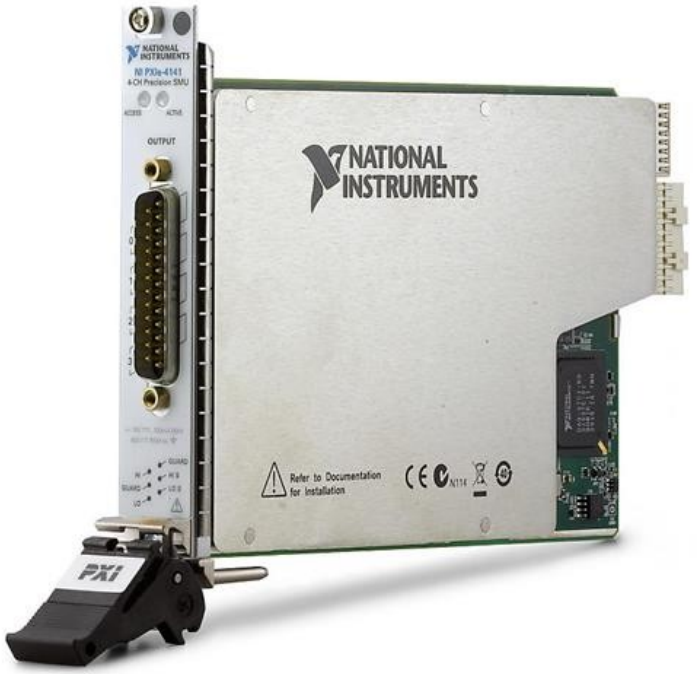


PCB status

- Mezzanine board production is underway at the manufacturer, should be delivered by this week;
- Motherboard has been fabricated and delivered to BNL on 11/24/2025 (yesterday);
- Electrical components are in hand and assembly team has prepared pick-and place machine to assemble motherboard as it gets delivered to instrumentation.

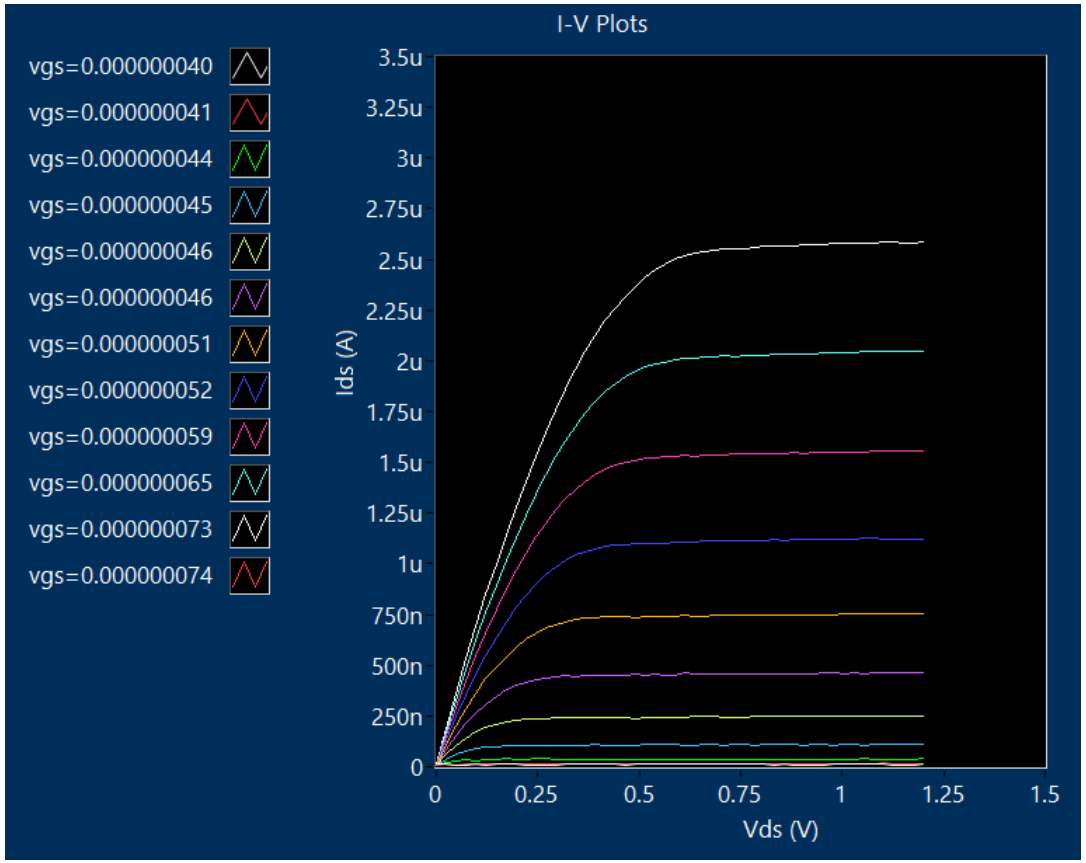
SMU procurement

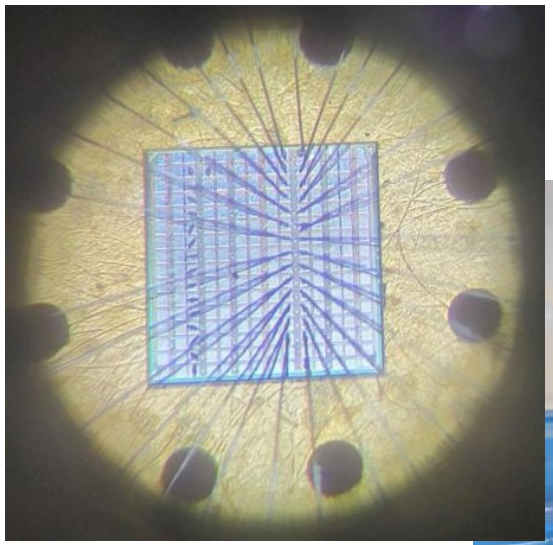
- The requisition for SMU (PXIe 4141) procurement was started on 10/21
- Bidding process was closed on 11/17
- PO was dispatched on 11/19
- Component lead time is about 1 week (per offer)
- We expect the SMUs to be shipped sometime next-week

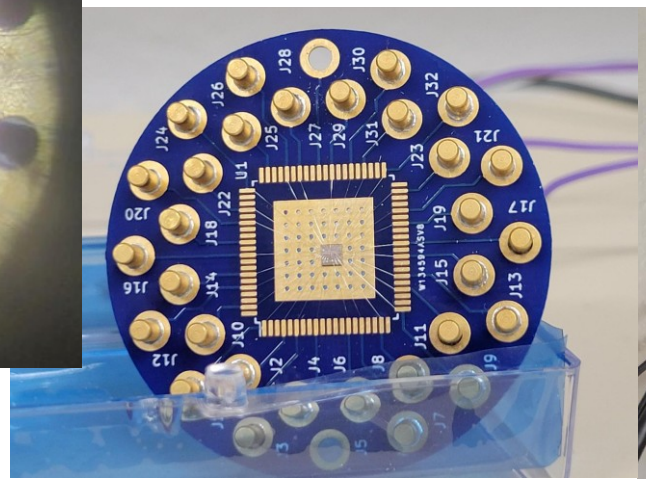


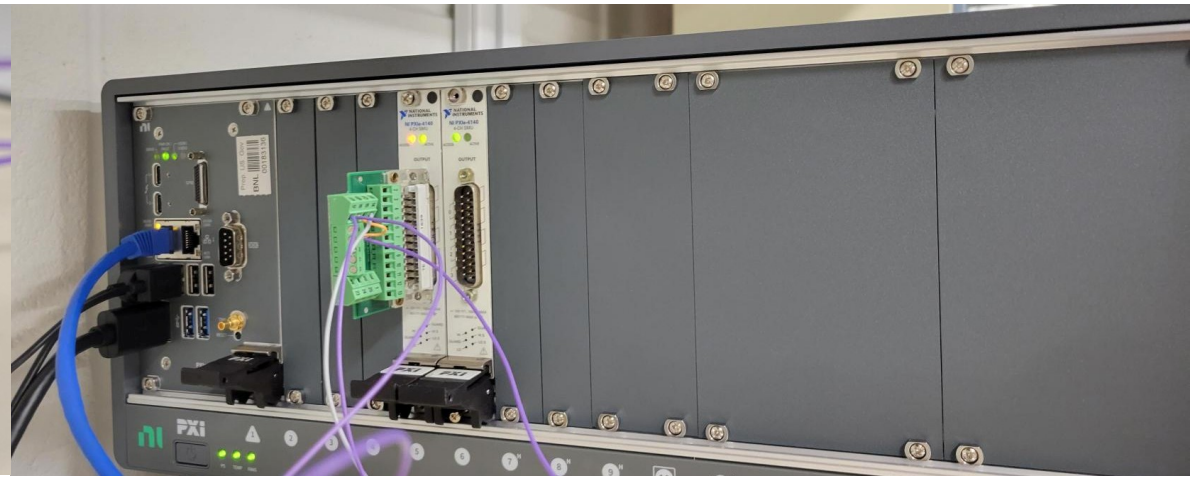
Software development

- SMU functionalities and basic software for measurement has been already testing with 2 samples SMUs and 65nm structures









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Software development

- Integrate programming of NVBG;
- Integrate PID control;
- Manual vs automatic measurement according to TID regime;
- Integrate alert if results do not match expectation → i.e. damage to devices;
- Optimizing and verifying data storing.
- Estimated time ~2 weeks (can be prepared before irradiation starts)

Testing plan

- System in place for dry-run with 65nm technology
  - Parts ready for first week of December
  - Bonding scheme for 65nm chip ready → can be implemented as mezzanine board arrives
  - ~1 week for commissioning with dry run
- Mid December → first run with MPW1:
  - **GOAL1**: verify NVBG functionality vs TID (3 Mrad)
    GOAL2: verify test structures properties vs TID (3 Mrad)
  - TID regime: 1 krad*, 10 krad*, 50 krad*, 100 krad – 3Mrad**
    *stop & measure; **continuous measurement
  - Temperature: Room Temperature
  - ON status
- Perform 5 runs more varying temperature to 40C and 0C and status OFF/ON;
- Assessment: 3Mrad or 1Mrad? 5.5 vs 1.8 days per chip

Summary

- Setup readiness
  - Co-60 source calibrated
  - Motherboard delivered to BNL, assembly performed this week
  - Mezzanine board to be shipped by this week, assembly likely next week
  - SMUs purchase completed, shipment expected next week
- Testing plan:
  - Dry run with 65nm in the first half of December (commissioning phase)
  - First run with MPW1 second half of December (Room temperature, 3Mrad)
  - Following: 40C and 0C testing at 3Mrad
- Decision on TID to be maintained at 3Mrad or scale down to 1Mrad
- Continue with established procedure on all available chips (13)