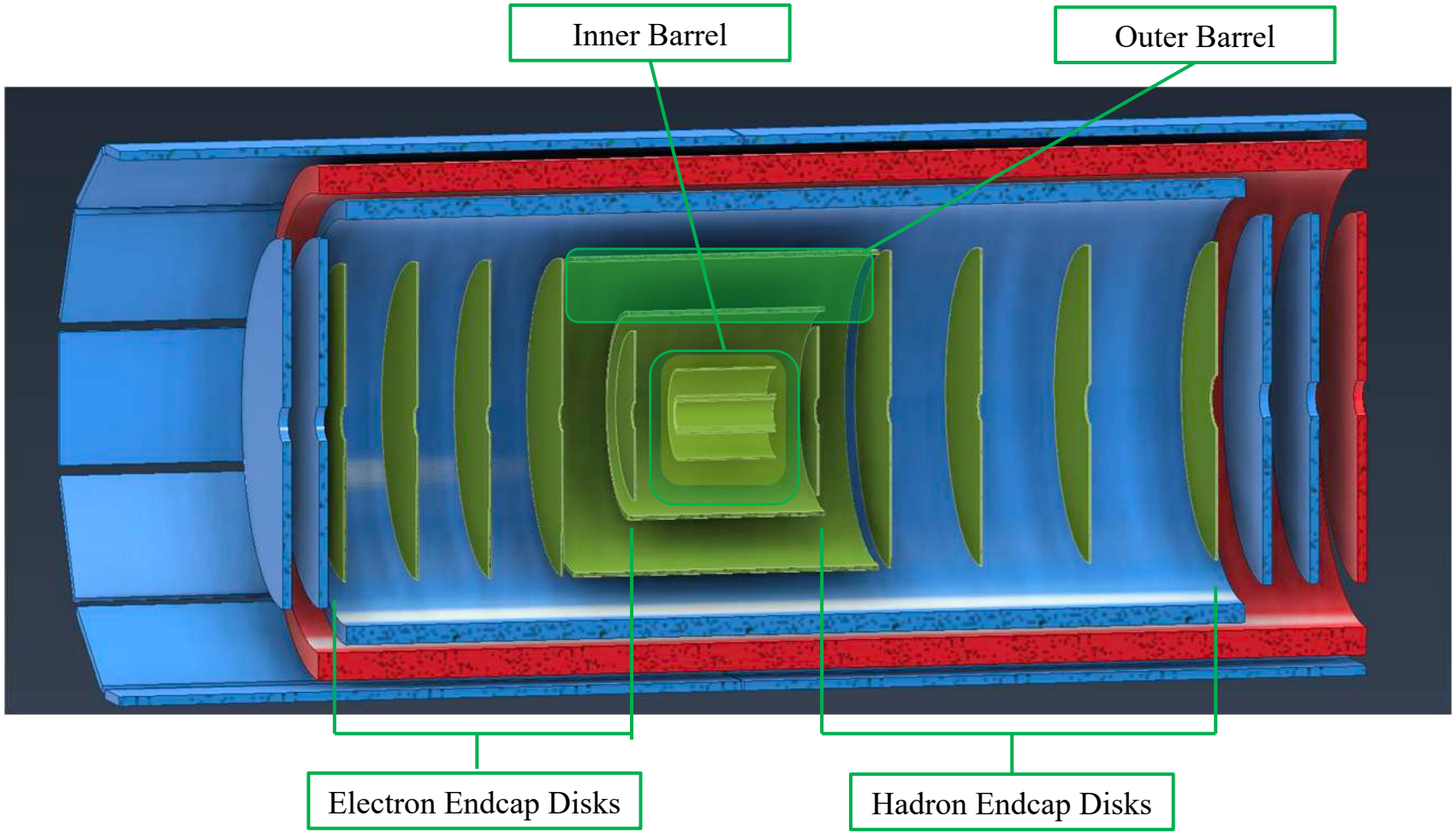
FPCs for SVT

- IT: Trieste
- US: BNL, LANL, LBNL
- UK: Daresbury Lab, Liverpool, Oxford
- UA: LTU

WP3: Electrical Interfaces
Coordinators: Marcello Borri, Zhenyu Ye

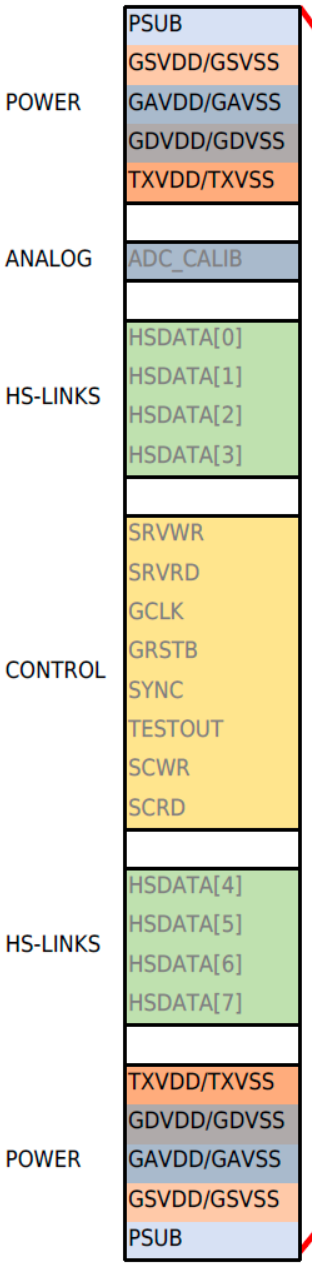
WP3: Electrical Interfaces		
3.1	Electrical interfaces IB (L0—2)	
3.1.1		Definition of specifications for FPCs & electrical interconnection
3.1.2		Design & supplier evaluation
3.1.3		Prototyping & testing of module, FPCs & electrical interconnection
3.1.4		Iterative improvements of FPC design & electrical interconnection
3.1.5		FPC design complete & electrical interconnection validated
3.1.6		Pre-production of FPCs for system test, including QC
3.1.7		Production of FPCs for production detector, including QC
3.2	OB HIC (L3--4)	
3.2.1		Definition of specifications for module, FPCs & electrical interconnection
3.2.2		Design & supplier evaluation
3.2.3		Prototyping & testing of module, FPCs & electrical interconnection
3.2.4		Iterative improvements of module design, FPC & electrical interconnection
3.2.5		OB module design complete
3.2.6		Pre-production of FPC for system test, including QC
3.2.7		Production of FPCs for detector grade modules, including QC
3.3	Disks HIC (ED0-4, HD0-4)	
3.3.1		Definition of specifications for module, FPCs & electrical interconnection & back plate
3.3.2		Design & supplier evaluation
3.3.3		Prototyping & testing of module, FPC, electrical interconnection & back plate
3.3.4		Iterative improvements of module design, FPC, electrical interconnection & back plate
3.3.5		Disk module design complete
3.3.6		Pre-production of FPCs for system test, including QC
3.3.7		Production of detector grade FPCs, including QC

Silicon Vertex Tracker



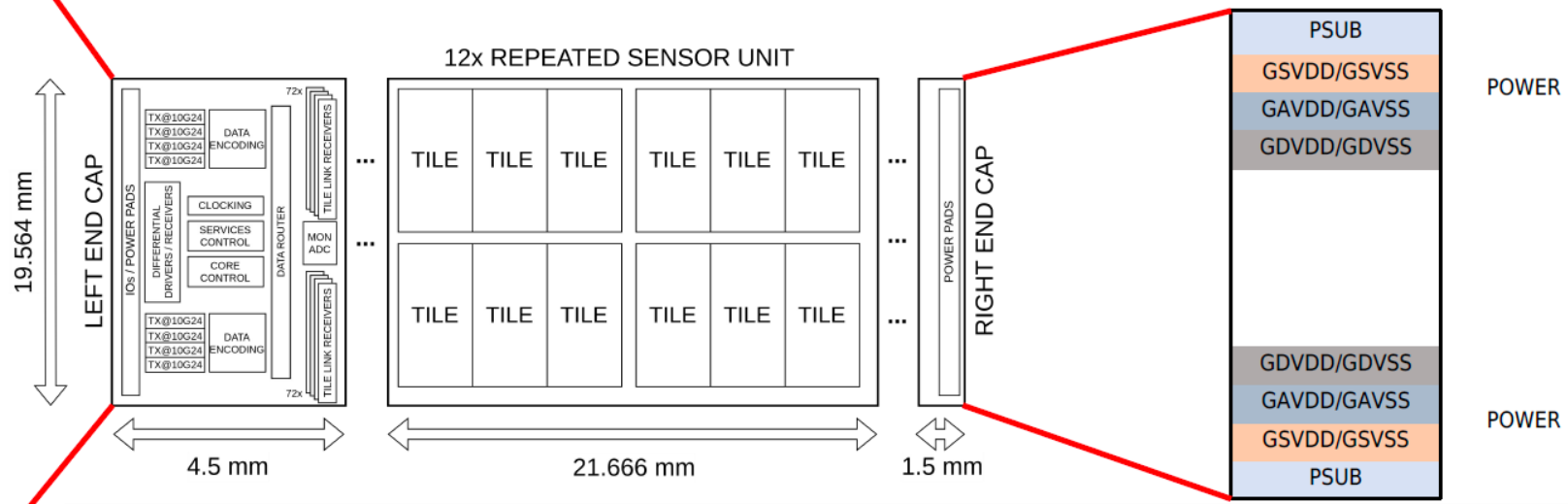
- **L0-2**: MOSAIX — **0.05% X/X_0**
- **L3-4**: EIC-LAS, AncASIC — **0.25/0.55% X/X_0**
- **ED/HD0-4**: EIC-LAS, AncASIC — **0.25% X/X_0**

MOSAIX



Power	Typ (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	50	
GAVDD/GSVSS (1.2V/0V)	340	540
GDVDD/GDVSS (1.2V/0V)	950	1430
TXVDD/TXSVSS (1.8V/0V)	200	

Signal	Frequency
GCLK	160 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5 Mbps
SCWR/RD	5 Mbps
HSDATA[0…7]	5.12/10.24 Gbps

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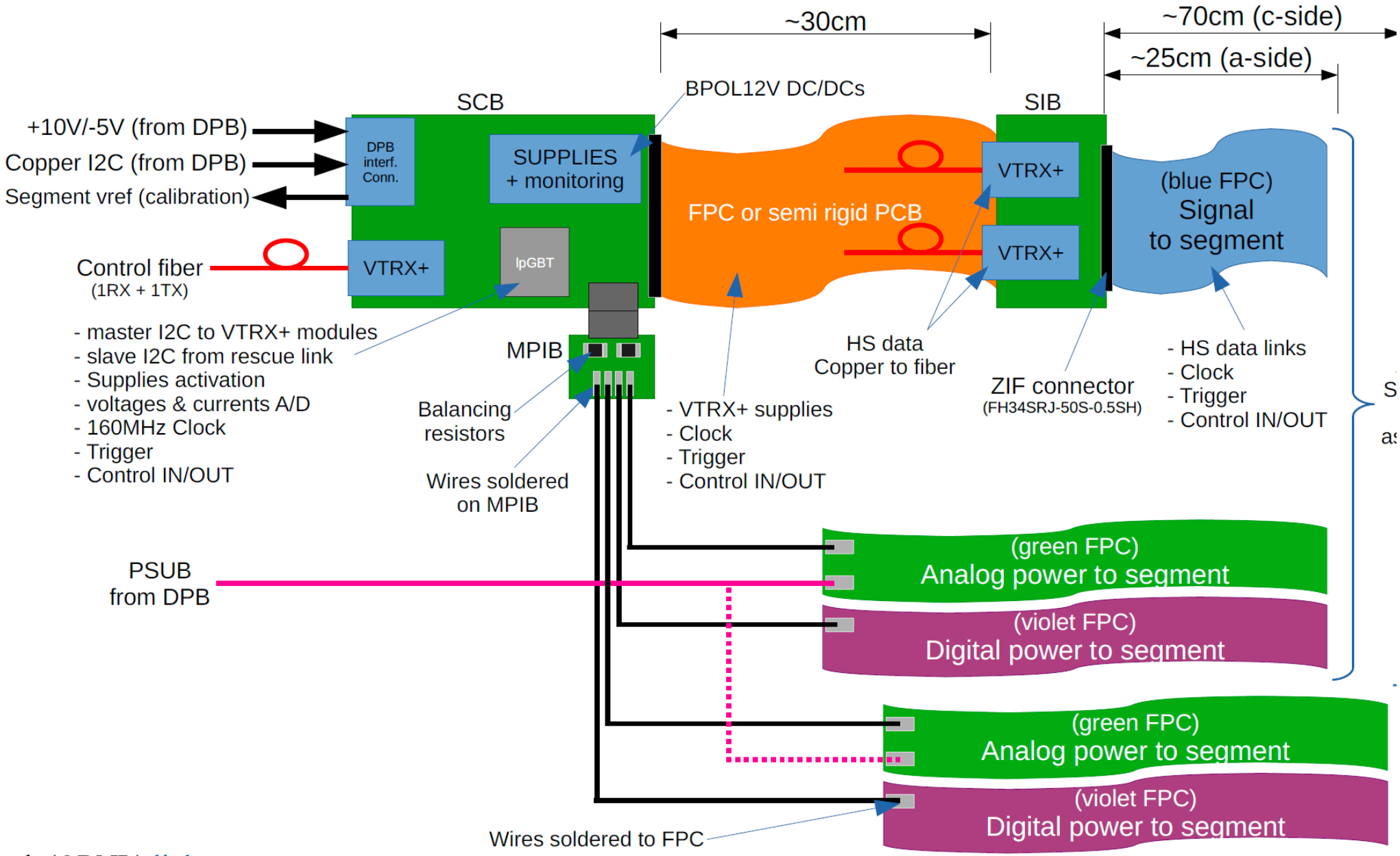
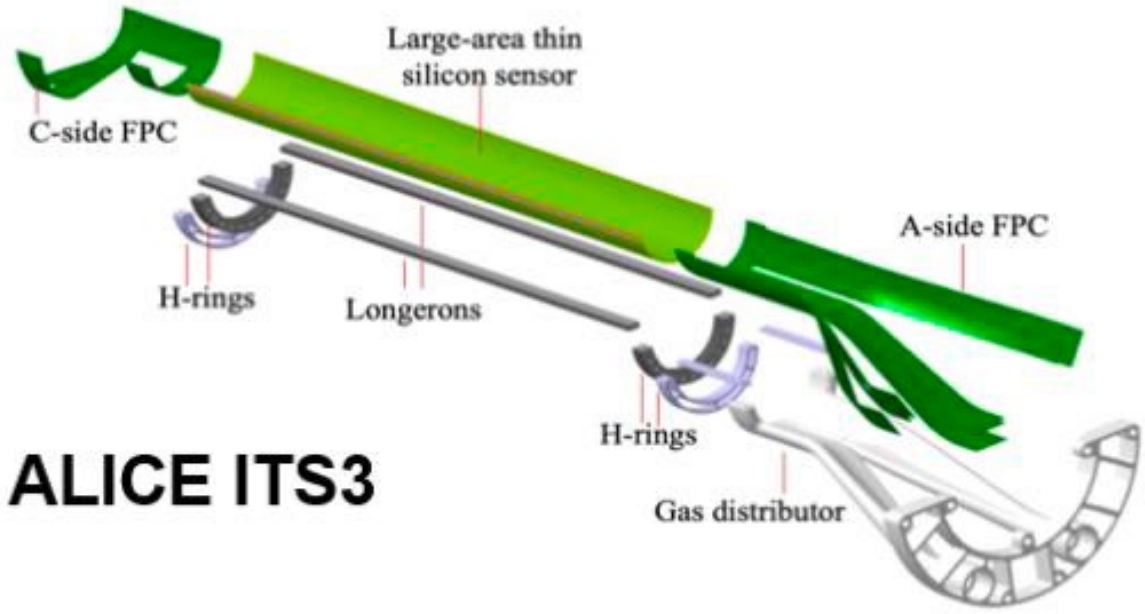
GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
```

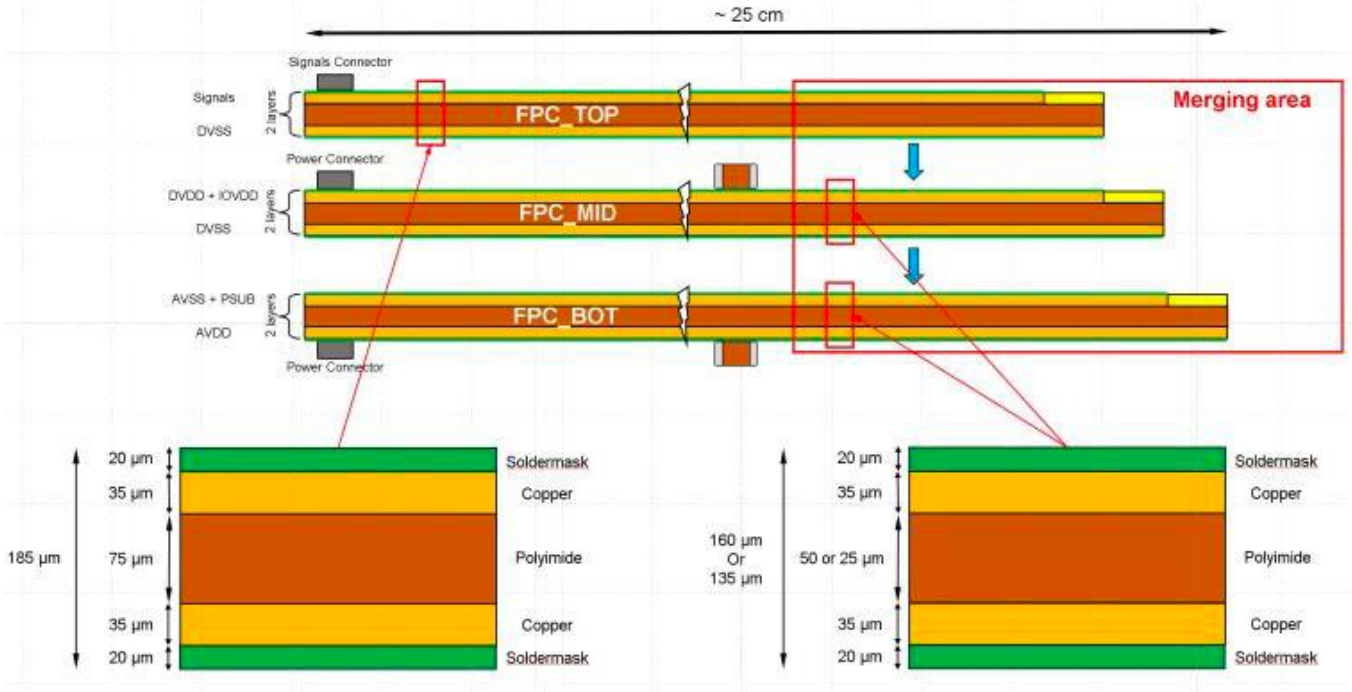
Power/Readout for SVT IB



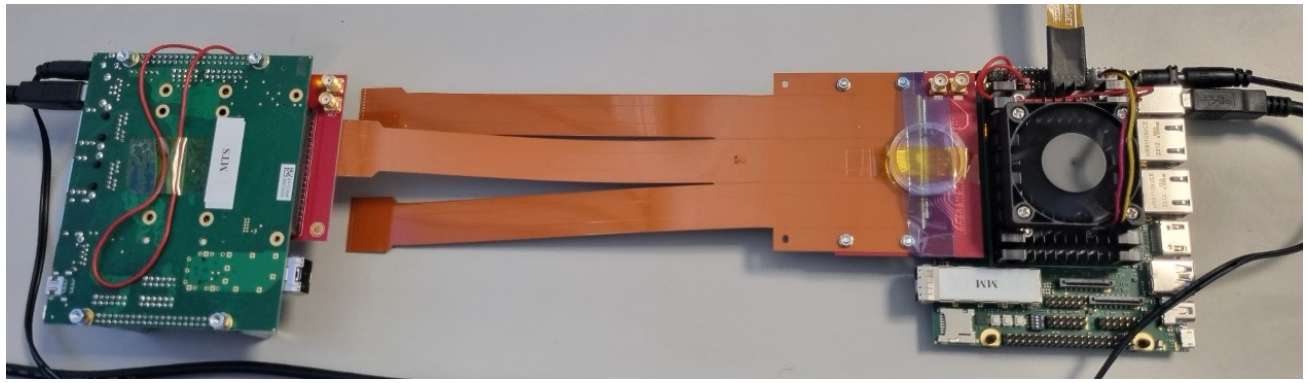
Joachim Schambach (ORNL) link

ITS3 FPCs

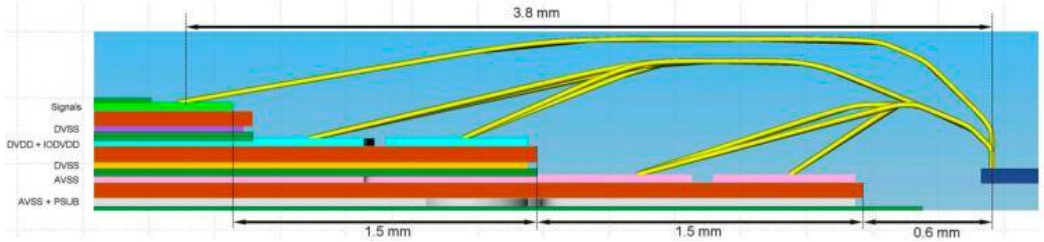




ITS3 test setup



Wire-bond Profile



SVT-IB FPCs

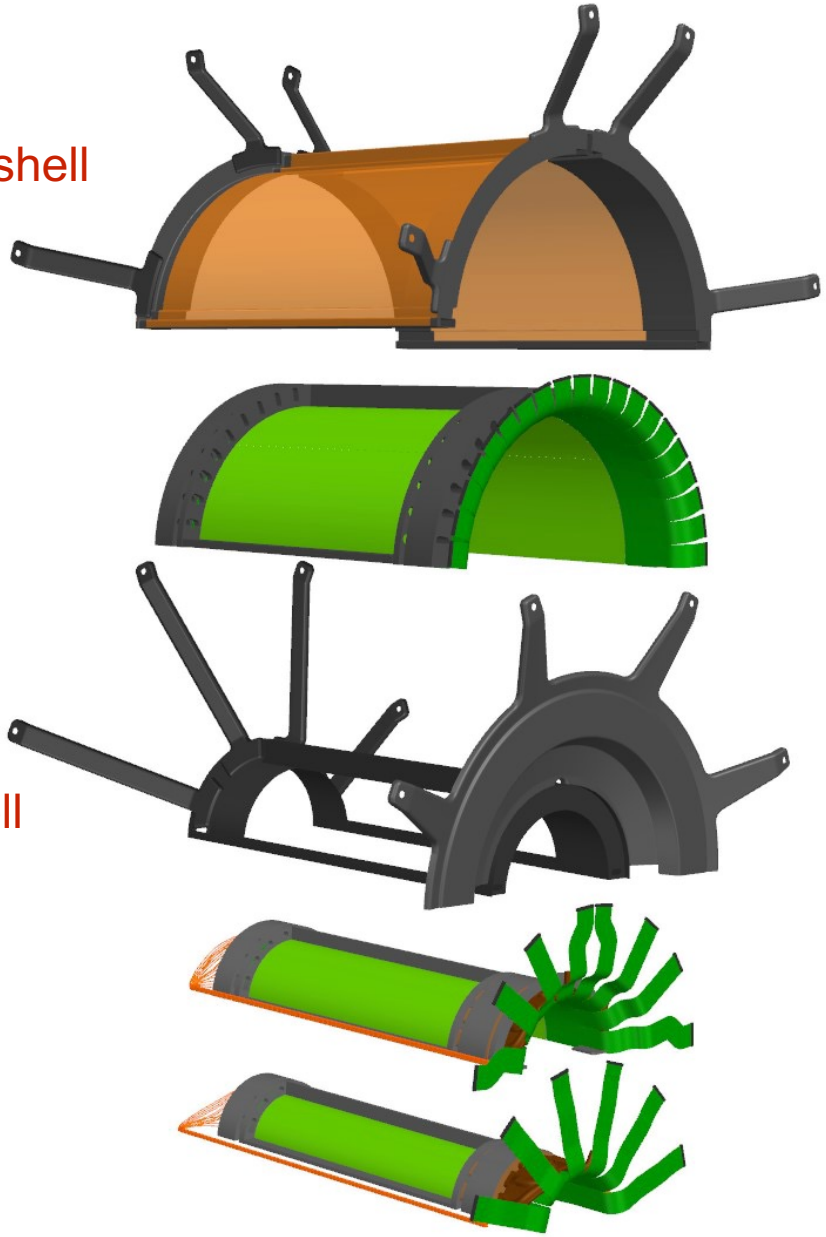
L2 external shell

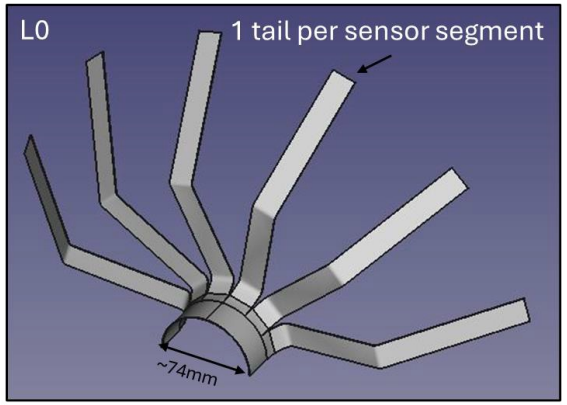
L2

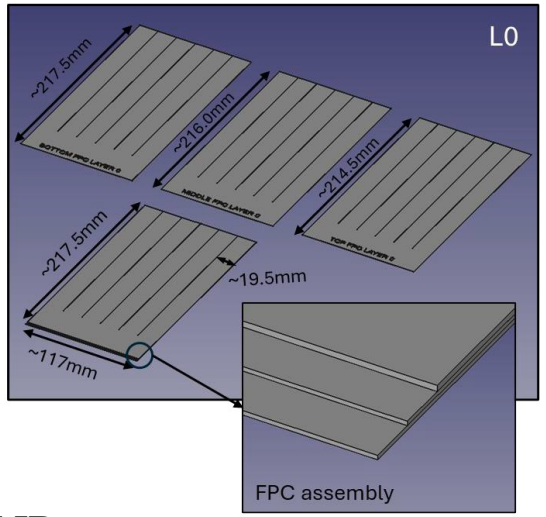
L0-L1 external shell

L1

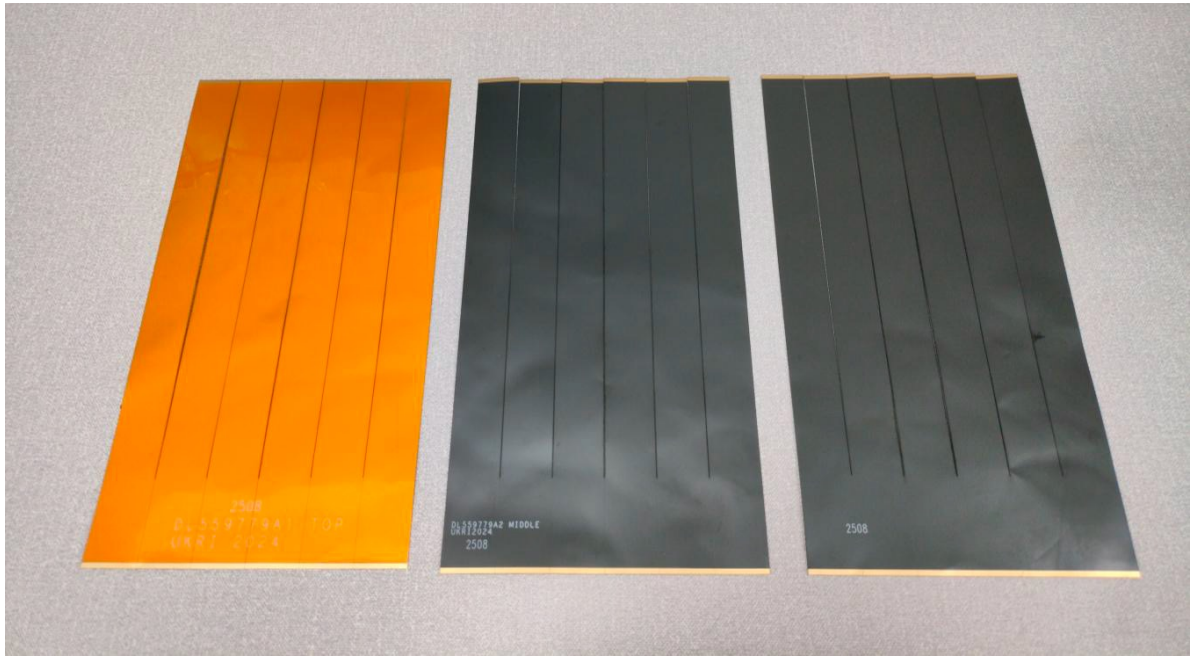
L0







Mechanical FPC prototypes for SVT-IB



SVT-IB FPC Ongoing Activities @ INFN

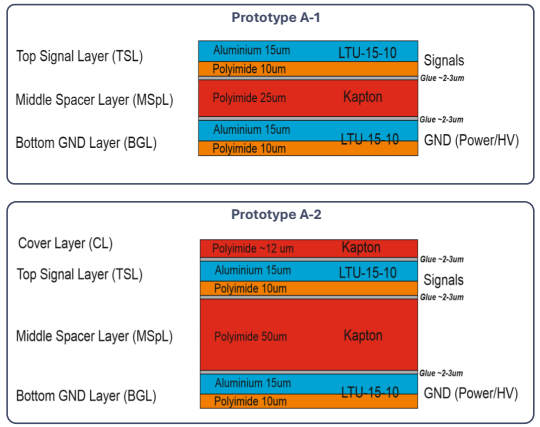
- Development of SVT-IB FPC prototypes with LTU
  - Prototypes for high-speed data transmission and mechanical test (i.e. bending, wire bonding)
  - Design files ready at LTU; procurement of photomasks to start this year; PO being finalized
  - Prototypes expected Q1-26

- Calculation of signal loss to understand signal integrity on Al FPC
  - Results to be shown at Oxford meeting next week

- Procurement of parts to setup an ITS3 FPC test stand almost done
  - Last connectors missing arriving in January

SVT-IB FPC Ongoing Activities

- Prototype A for high-speed data transmission tests

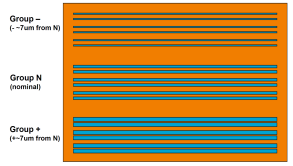


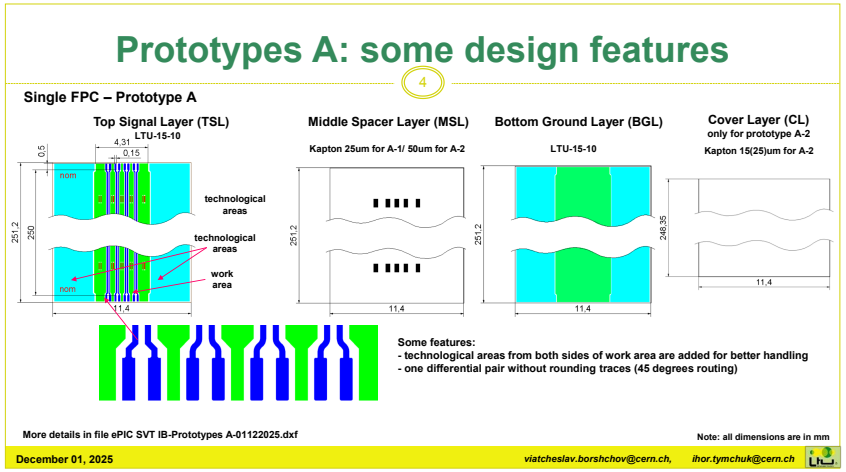
Prototypes to investigate electrical properties

- Differential impedance = 100 Ω
- Trace width = 70 µm
- Trace thickness = 15 µm
- Space between traces = 80 µm
- Trace pitch = 150 µm

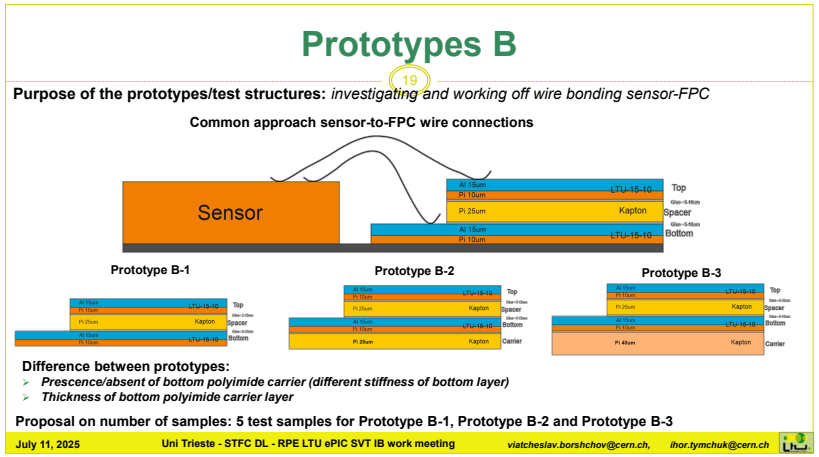
Two broad variants

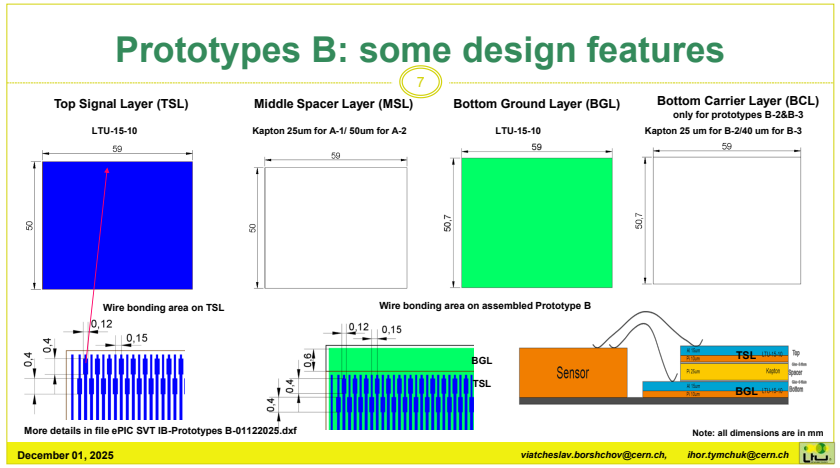
- A-1: Without cover layer, 25 µm middle spacer layer
- A-2: With cover layer, 50 µm middle spacer layer
- Further sub-variants with ±10% trace width
- 5 test samples of each variant (18 cm trace length)



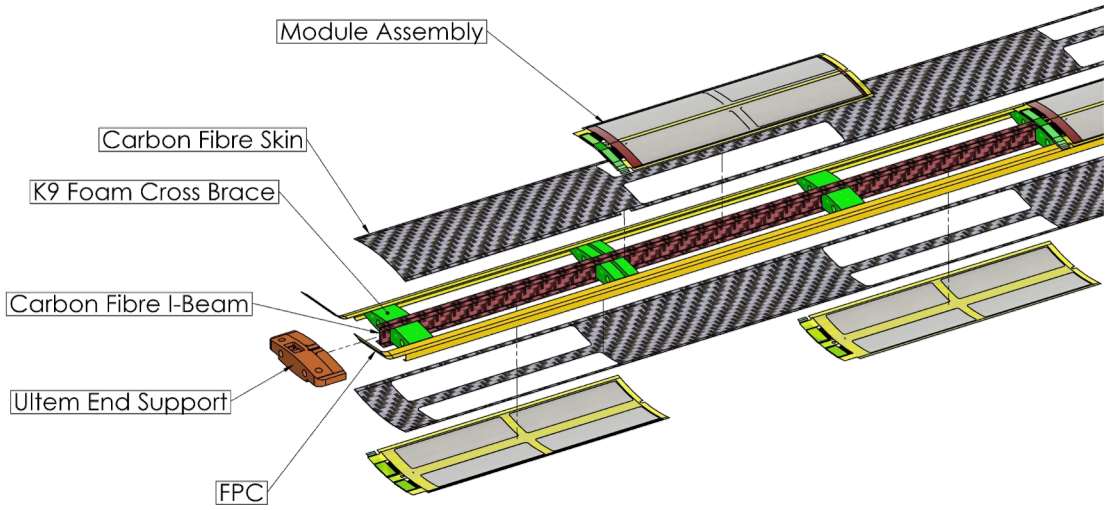


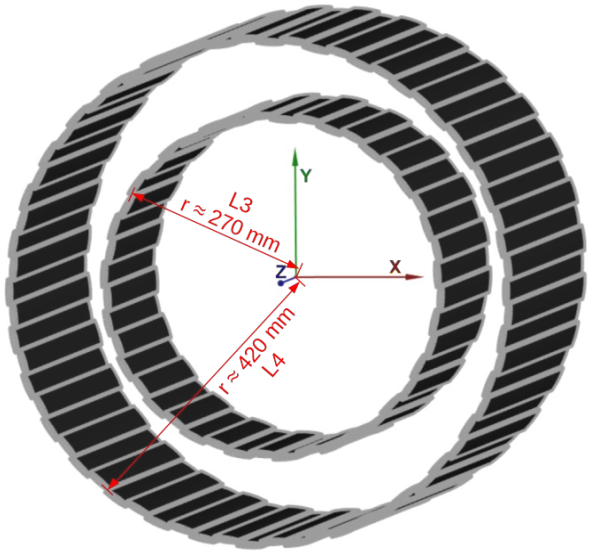
- Prototype B for mechanical tests (i.e. bending and wire bonding)

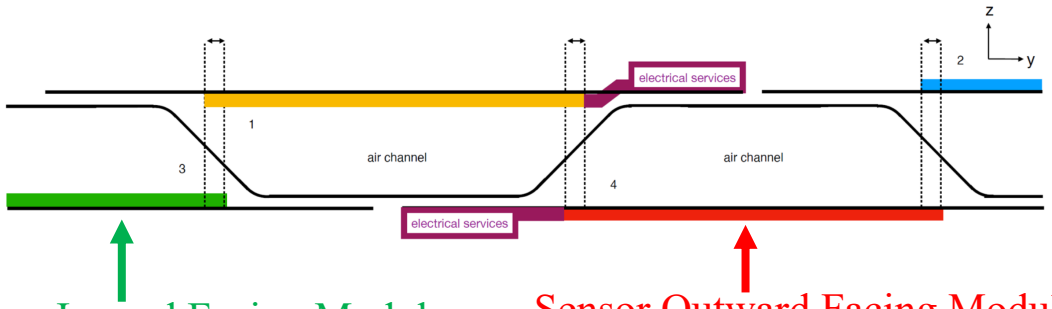




SVT Outer Barrel and Disks

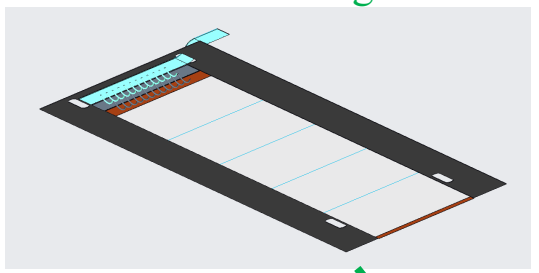


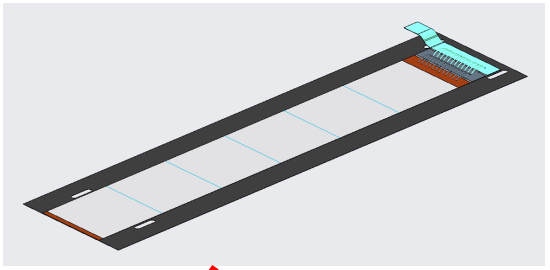


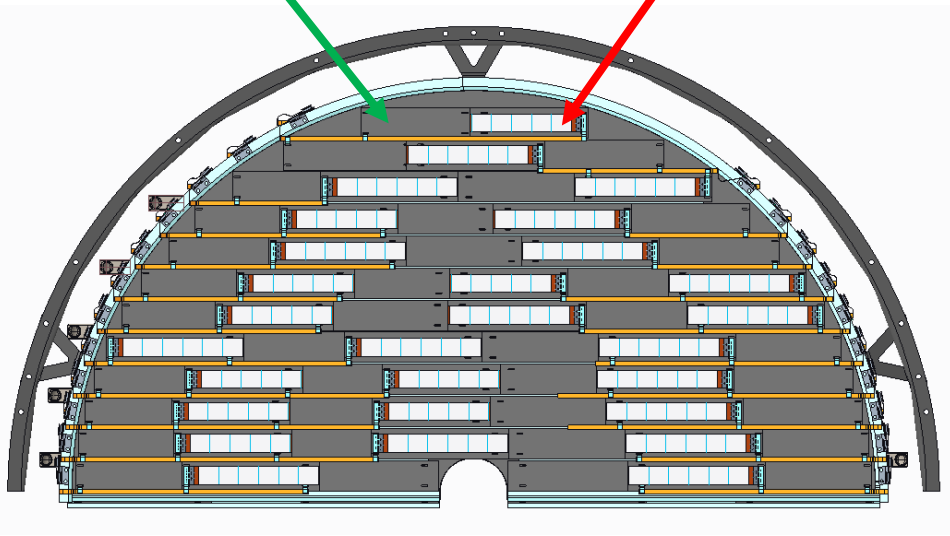


Sensor Inward Facing Module

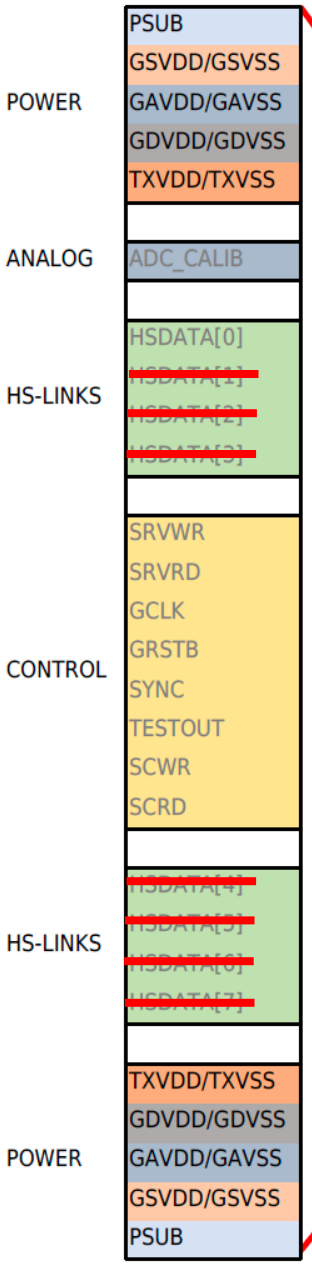
Sensor Outward Facing Module





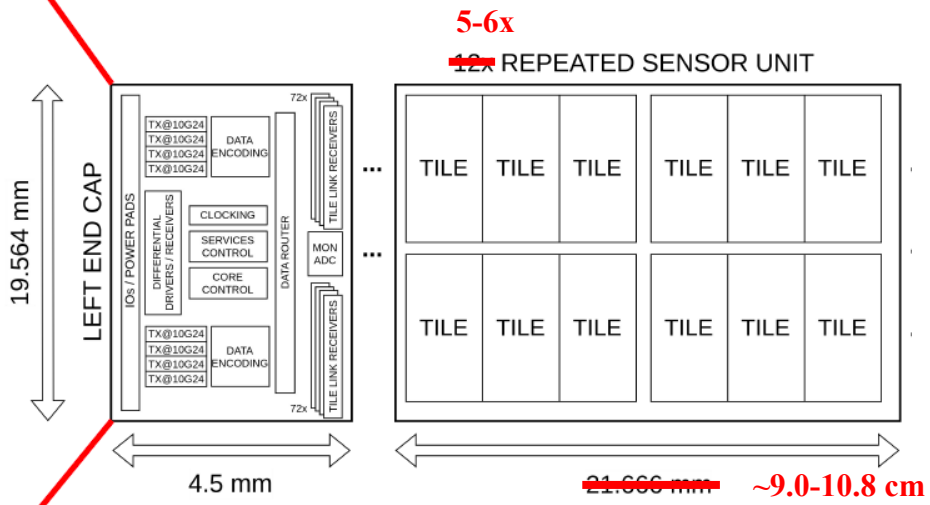


EIC-LAS



Supply	Typ (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.32V/0V)	40	60
GAVDD/GSVSS (1.32V/0V)	170	270
GDVDD/GDVSS (1.32V/0V)	526	816
TXVDD/TXSVSS (1.2V/0V)	200	300

Signal	Frequency
GCLK	80/160 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5 Mbps
SCWR/RD	5 Mbps
HSDATA[0…7]	5.12/10.24 Gbps

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GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (~~1.8V/0V~~ 1.2V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
```
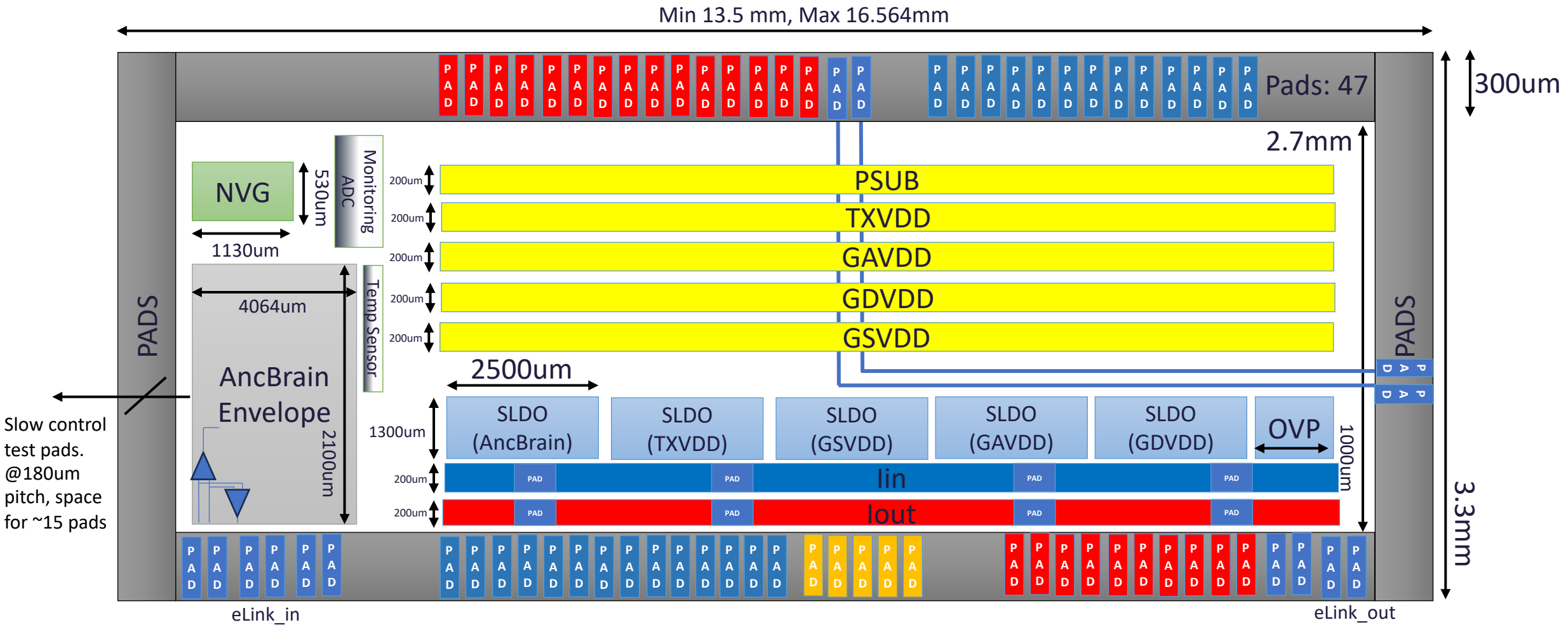
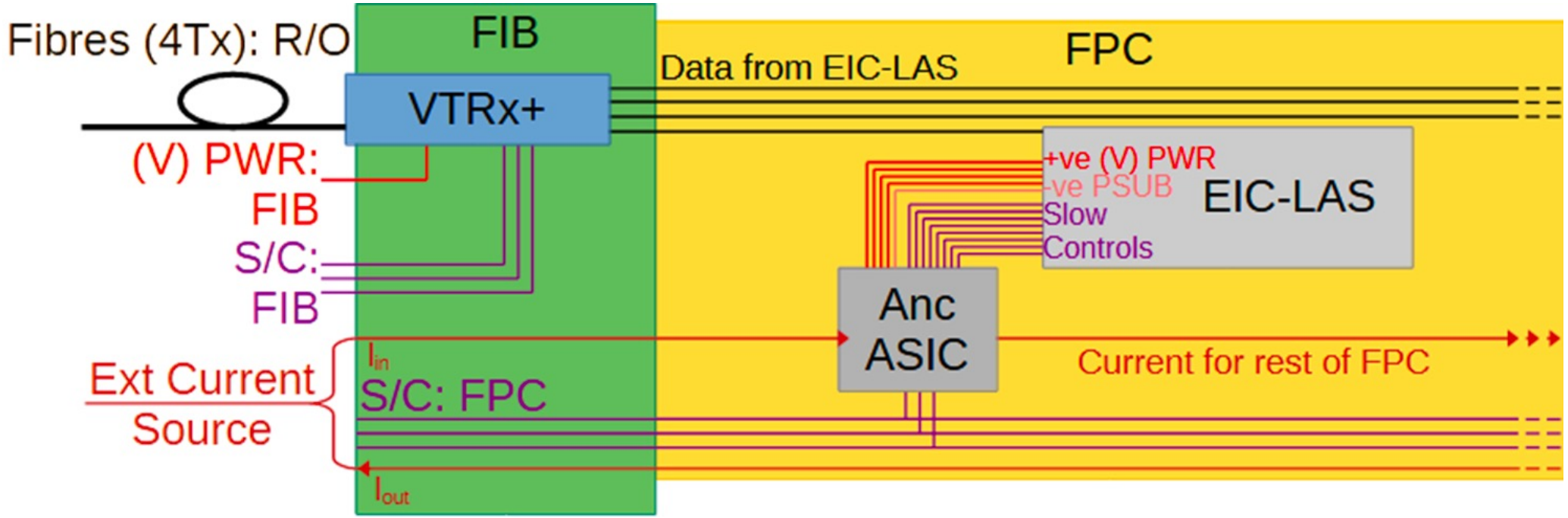

AncASIC

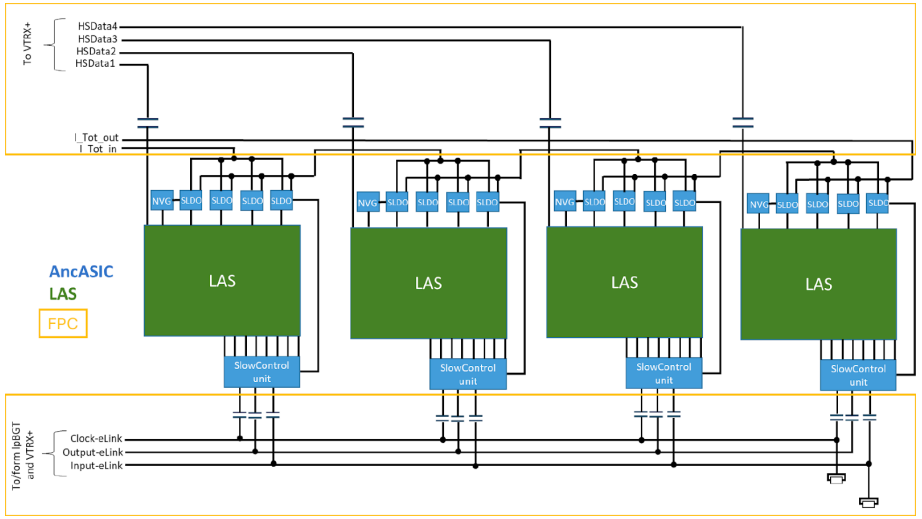
Preliminary



Iain Sedgwick link

Power/Readout for SVT OB/Disks

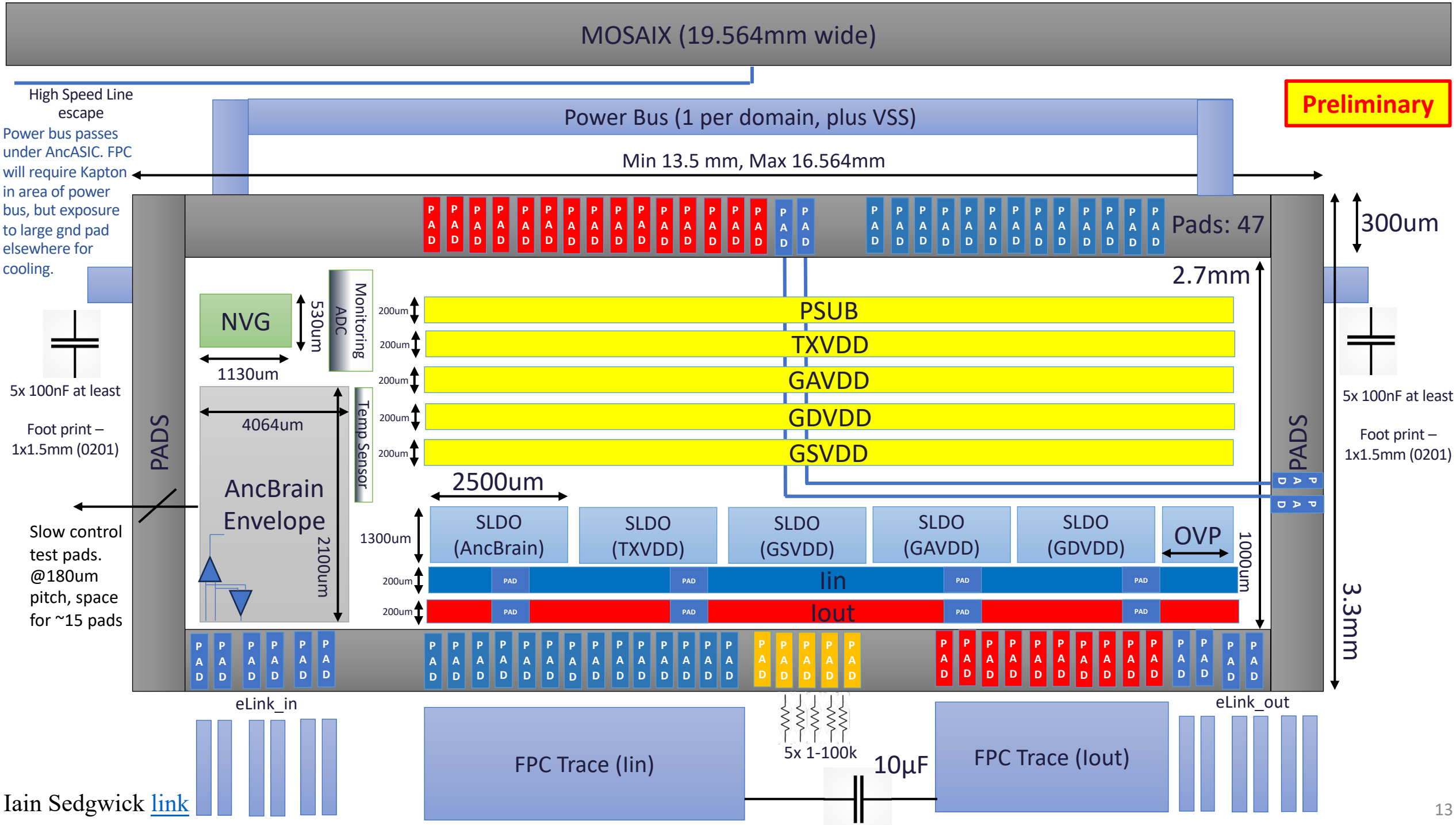




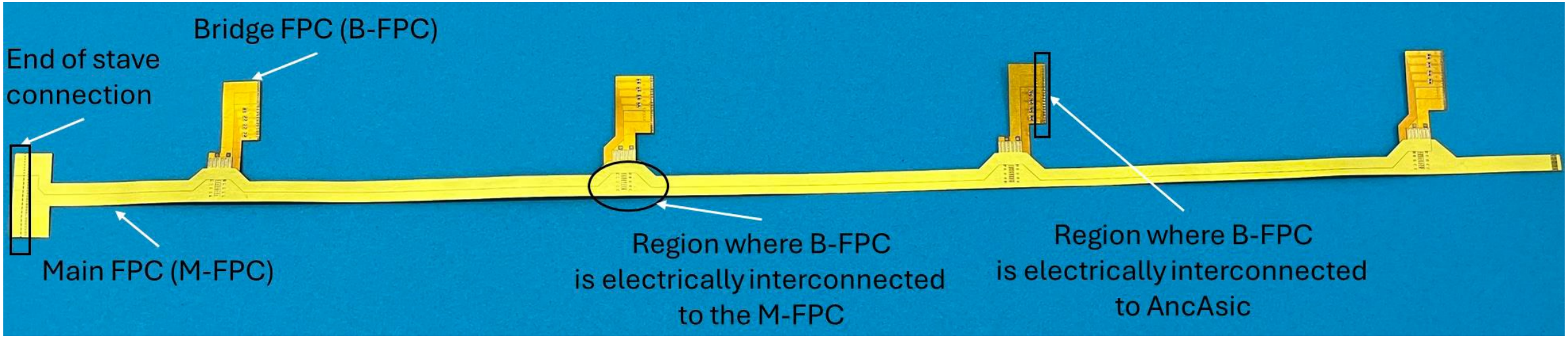
wire-bonding, spTAB bonding, soldering

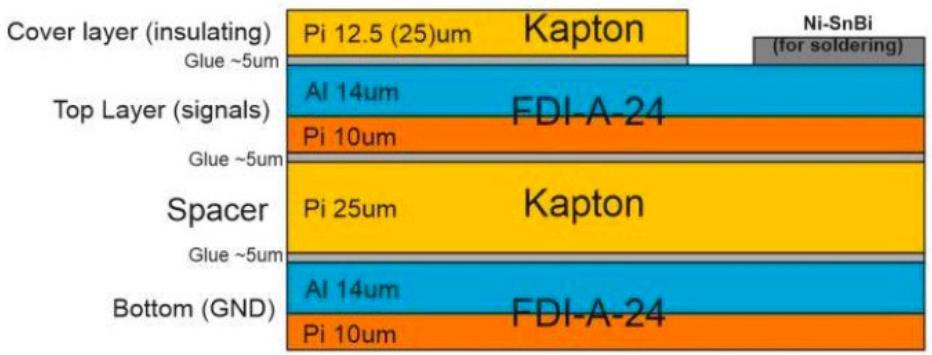
Signal	Type	Comment	Rate
SC_in	AC/DC	from lpGBT to AncASICs	40/160/320 Mbps
SC_out	AC/DC	from AncASICs to lpGBT	40/160/320 Mbps
SC_clk	AC/DC	from lpGBT to AncASIC	40/160/320 MHz
HS data	AC	from EIC-LAS to VTRX+	5.12/10.24 Gbps
Current	DC	from FIB to AncASIC	N/A

James Julian Glover link


MOSAIX (19.564mm wide)
Preliminary
High Speed Line escape
Power bus passes under AncASIC. FPC will require Kapton in area of power bus, but exposure to large gnd pad elsewhere for cooling.
Power Bus (1 per domain, plus VSS)
Min 13.5 mm, Max 16.564mm
Pads: 47
300um
2.7mm
3.3mm
5x 100nF at least
Foot print – 1x1.5mm (0201)
PADS
NVG
530um
1130um
Monitoring ADC
Temp Sensor
4064um
AncBrain Envelope
2100um
200um
PSUB
TXVDD
GAVDD
GDVDD
GSVDD
2500um
1300um
SLDO (AncBrain)
SLDO (TXVDD)
SLDO (GSVDD)
SLDO (GAVDD)
SLDO (GDVDD)
OVP
1000um
Iin
Iout
Slow control test pads. @180um pitch, space for ~15 pads
eLink_in
eLink_out
FPC Trace (Iin)
5x 1-100k
10µF
FPC Trace (Iout)
Iain Sedgwick link

STFC-LTU FPC Prototypes



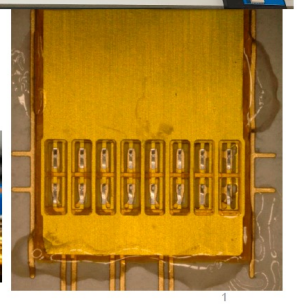


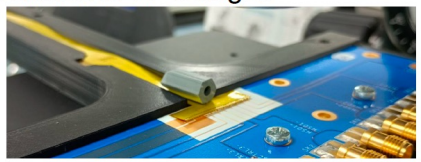
	LTU FPC			
Components	Thickness (um)	Material	X0(cm)	X0(%)
Metal layers	15 + 15*0.69	Aluminum	8.897	0.028
Dielectric	10+10+25+25	Polyimide	28.57	0.023
glue	15	TBC	39.07	0.004
Total				0.055

spTAB vs wire-bonding on LTU FPCs

M-FPC prototype 2

- New FPC installed using an update jig from Oxford.
- Nylon stand-offs used as weights to aid alignment of FPC.
- UV-cure glue-dots used to hold FPC flat and aligned during bonding.
- Additional glue added to FPC edges post-bonding.



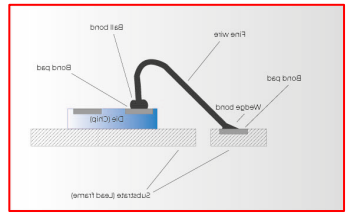


Prototype 1 trials reported in March

Summary

- 2nd FPC prototype has been bonded.
- Bonded went well.
- No (obvious) damage seen from a visual inspection.
- Basic electrical continuity confirmed @ Birmingham
- Sent to Daresbury Lab for further testing.

James Julian Glover link



Parameter matrix & 15 µm overtravel

Parameter Matrix

	Glued on PCB			Thicker Diffuser			Thinner Diffuser			Glued on PCB			Thicker Diffuser			Thinner Diffuser		
	Single Layer			Single Layer			Single Layer			Multi Layer			Multi Layer			Multi Layer		
Parameters	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev
22US% 22CN	20	11.18	0.69	17	7.3	1.18	17	9.88	1.63	19	10.73	1.77	19	11.11	2.24	15	11.65	0.49
25US% 22CN	20	11.46	0.18	17	6.83	1.79	18	10.83	1.4	20	10.45	1.32	20	11.78	0.43	20	12.12	0.34
25US% 25CN	19	11.26	0.59				20	8.53	1.61	19	11.04	0.67	20	11.1	0.79	20	11.95	0.47
28US% 25CN	20	11.21	0.62				20	9.74	2.15	19	11.03	0.25	20	11.95	0.34	20	11.96	0.73
28US% 28CN	20	11.33	0.36				12	6.61	1.84	20	11.04	0.88	20	11.11	1.09	20	11.77	1
30US% 28CN	20	11.04	0.8		Failed		17	7.96	2.94	20	11.06	0.69	20	11.87	0.53	20	11.43	1.41
30US% 30CN	16	10.49	0.82				17	5.89	2.1	20	11.03	0.49	20	11.87	0.68	20	10.99	1.38
32US% 30CN	20	10.99	0.65				13	5.66	1.95	20	10.8	0.82	20	12.07	0.58	20	12.16	0.75
32US% 32CN	20	10.66	0.77				6	5.68	1.32	20	9.45	1.2	20	11.18	1.39	20	11.04	1.99

15 µm Overtravel

	Glued on PCB			Thicker Diffuser			Thinner Diffuser			Glued on PCB			Thicker Diffuser			Thinner Diffuser		
	Single Layer			Single Layer			Single Layer			Multi Layer			Multi Layer			Multi Layer		
Parameters	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev
25US% 22CN	20	11.21	0.47		Failed		18	10.67	1.03	20	11.48	0.44	17	11.27	1.19	19	11.99	0.88
25US% 25CN	20	10.89	0.88	20	8.09	1.69	20	9.42	1.45	20	10.96	1.09	20	11.93	0.22	20	10.63	1.55
28US% 25CN	20	11.34	0.39	18	8.97	1.1	17	9.24	2.1	20	11.34	0.65	20	11.94	0.63	20	12.06	0.55
28US% 28CN	20	10.79	0.94	11	3.8	1.09	15	8.27	1.54	20	11.09	0.43	17	10.98	1.58	20	11.89	0.9
30US% 28CN	20	11.06	0.82				15	8.58	2.33	19	11.09	0.64				20	11.23	1.28
30US% 30CN	20	11.3	0.65		Failed			Failed		18	10.82	0.76		Failed		17	9.4	1.57
32US% 30CN	20	11.25	0.38							20	11.06	0.66				11	10.74	1.33

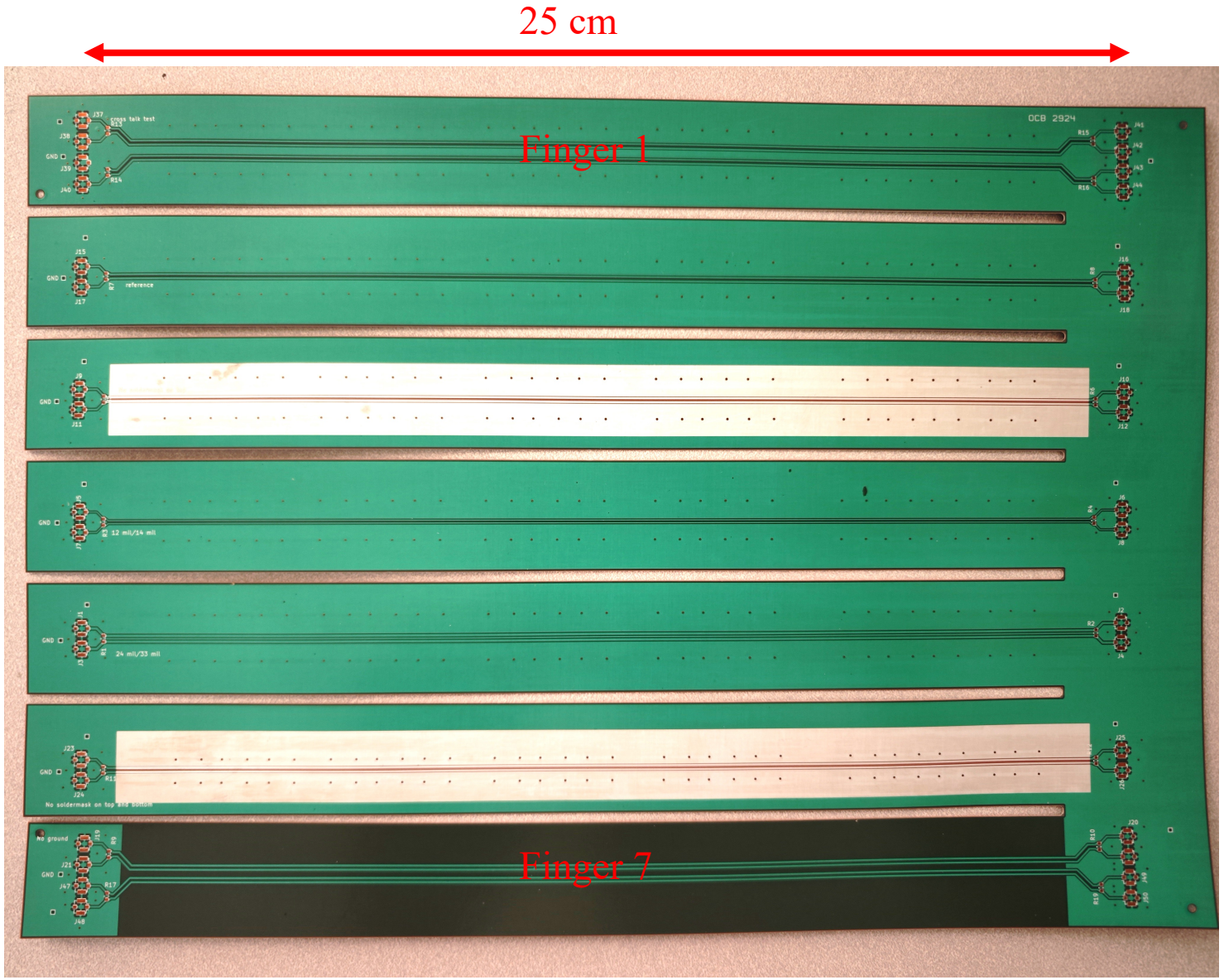
Summary

- Bonding quality was superior when foils were glued to a PCB, likely due to the added mechanical stability
- The thinner diffuser significantly improved vacuum-assisted bonding, though some stability challenges remain
- Multi-layer foils consistently offered easier and more reliable bonding, regardless of method
- The study demonstrated that acceptable mean strength and standard deviation values can be achieved

- Next steps:
  - Investigate further improvements for single-layer foils under vacuum. Any suggestions are welcome
    - Consider adjusting touchdown force or tail length
  - Plan comparative tests with alternative wire materials

Jian Liu link

LBL-OMNI FPC Prototypes



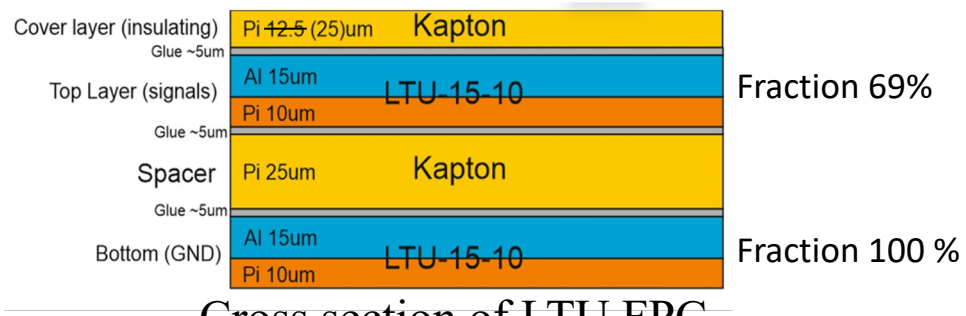
12 FPCs, 2 for each of the following:

- Different metals: Al, Cu
- Different dielectric: FR4, polyimide, EM 528K

Each FPC has 7 fingers with different layouts:

1. 2 pairs of differential lines with GND
2. 1 pair of differential line with width/space of 18mil/22mil
3. No soldermask on top
4. 12 mil/14 mil
5. 24 mil/33mil
6. No soldermask on top or bottom
7. 2 pairs of differential lines without GND on top

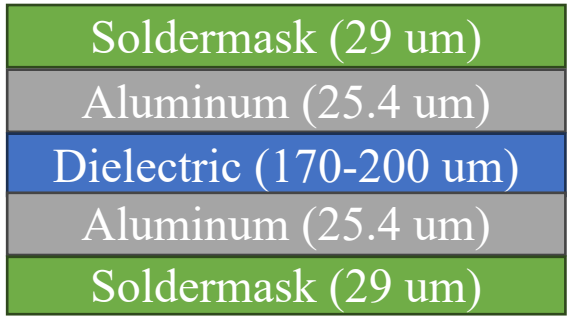
OMNI



Fraction 69%

Fraction 100 %

Cross section of LTU FPC



Top (Signals), Fraction74%

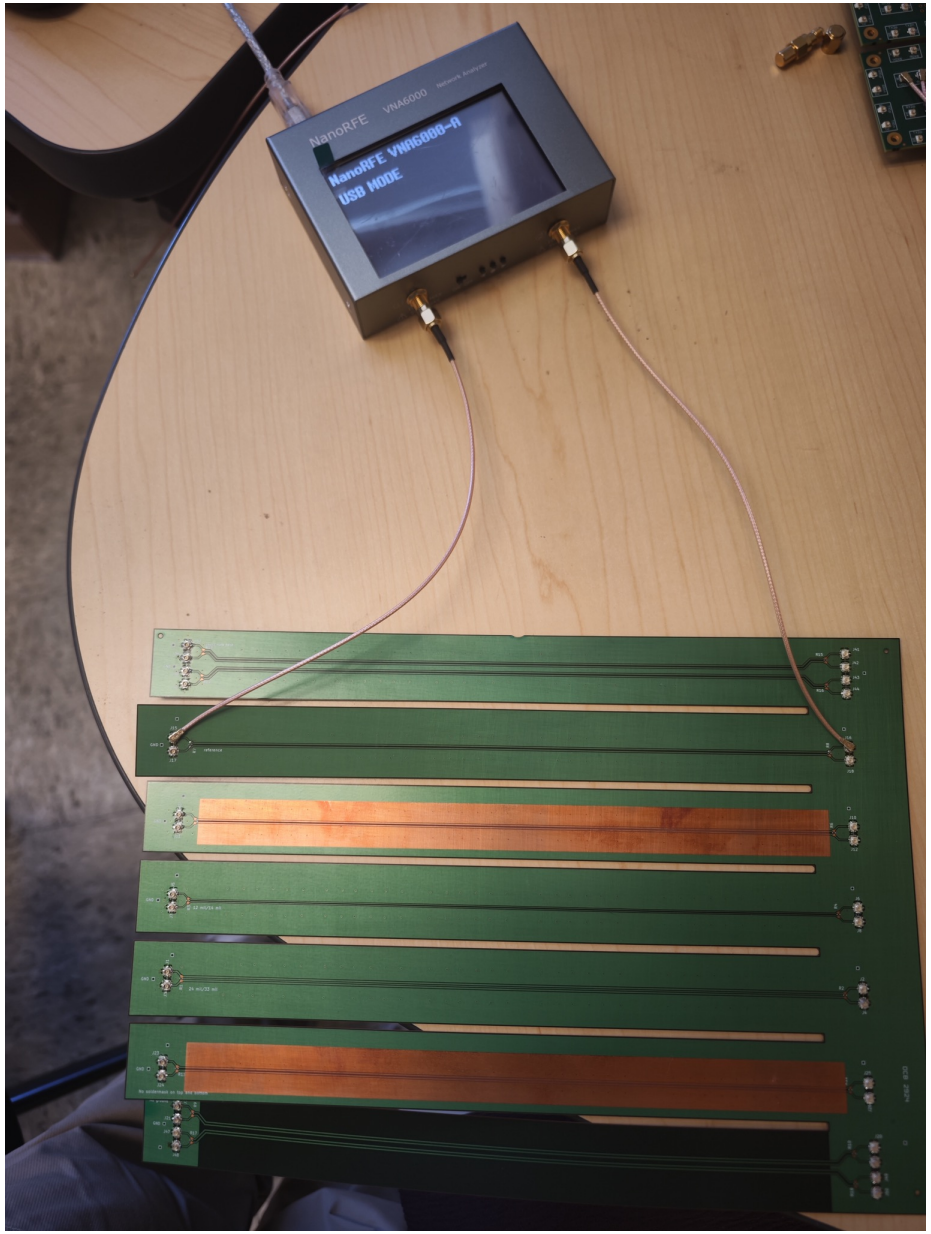
Bottom (GND), Fraction 100%

Cross section of OMNI

	LTU FPC				OMNI FPC in 2nd set			
Components	Thickness (um)	Material	X0(cm)	X0(%)	Thickness (um)	Material	X0(cm)	X0(%)
Metal layers	15 + 15*0.69	Aluminum	8.897	0.028	25.4+25.4*0.74	Aluminum	8.897	0.05
Dielectric	10+10+25+25	Polyimide	28.57	0.023	58 + (170~200)	Soldermask Ink + Arlon 528K	28.57	0.08~0.09
glue	15	TBC	39.07	0.004				
Total				0.055				0.13-0.14

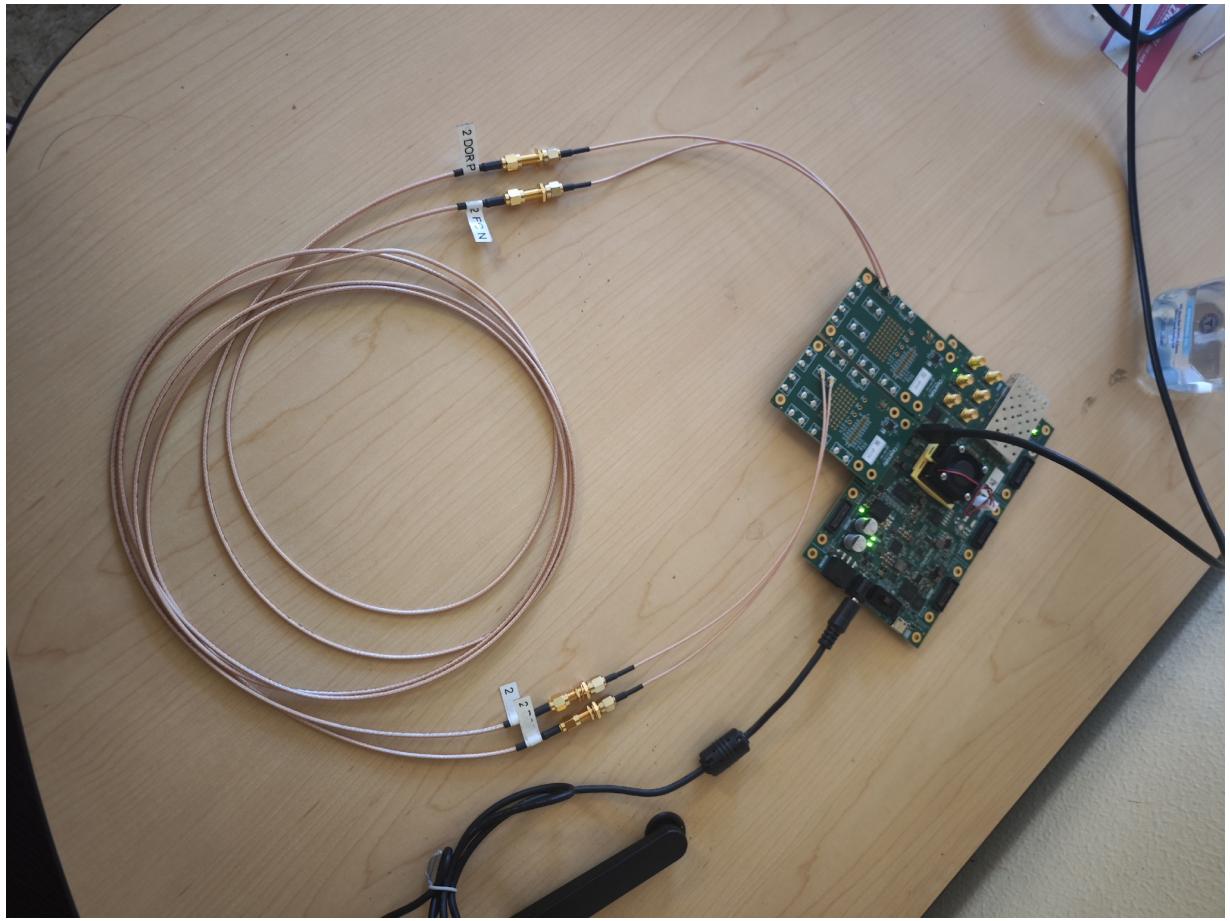
The average material budget over the full area of a module/stave/disk may be within specs

Measurements with VNA

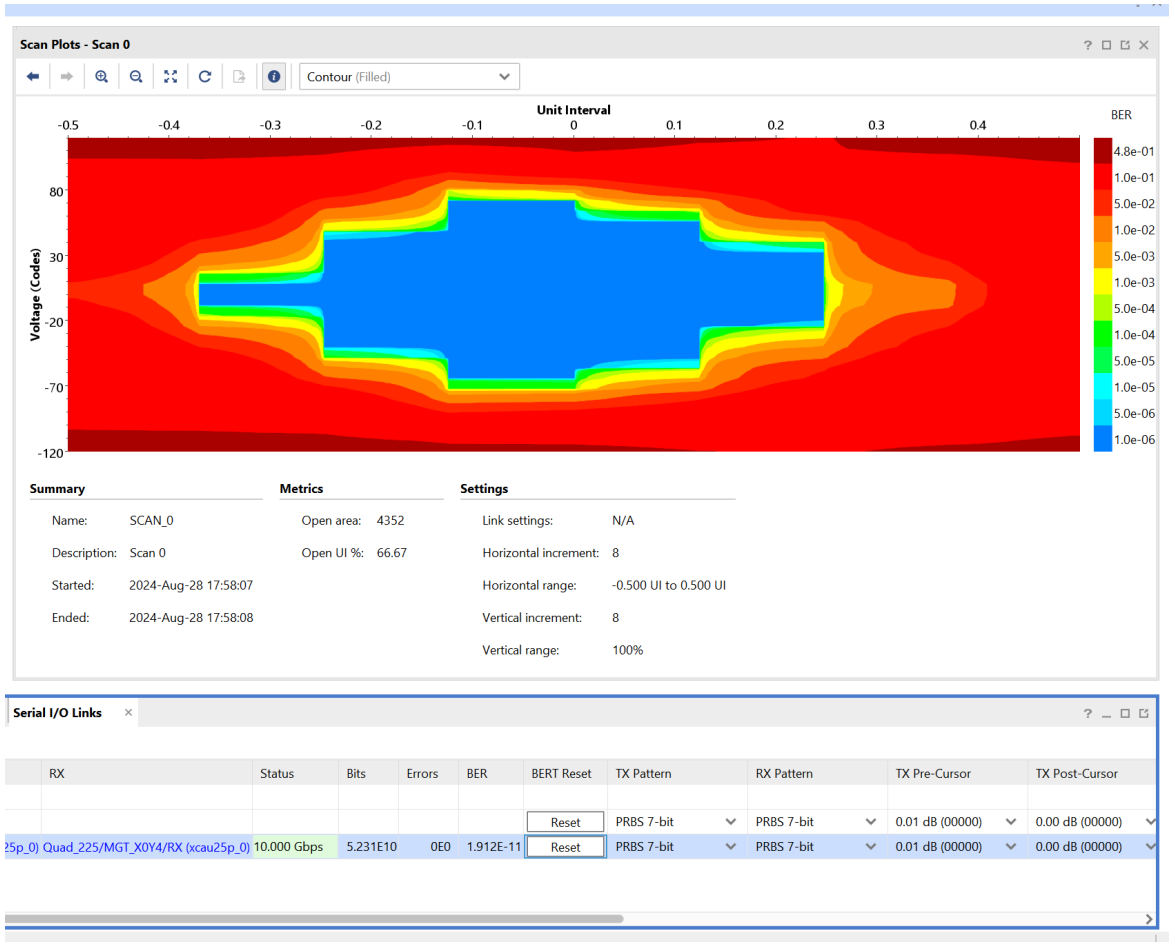


- Based on VNA 6000A vector network analyzer;
- For each trace, Scanned the Smith Chart and S-parameter from 1MHz to 4 GHz;
- Evaluated the signal loss on each finger by comparing their S21 parameters.

IBERT Test with Direct Cable Connection

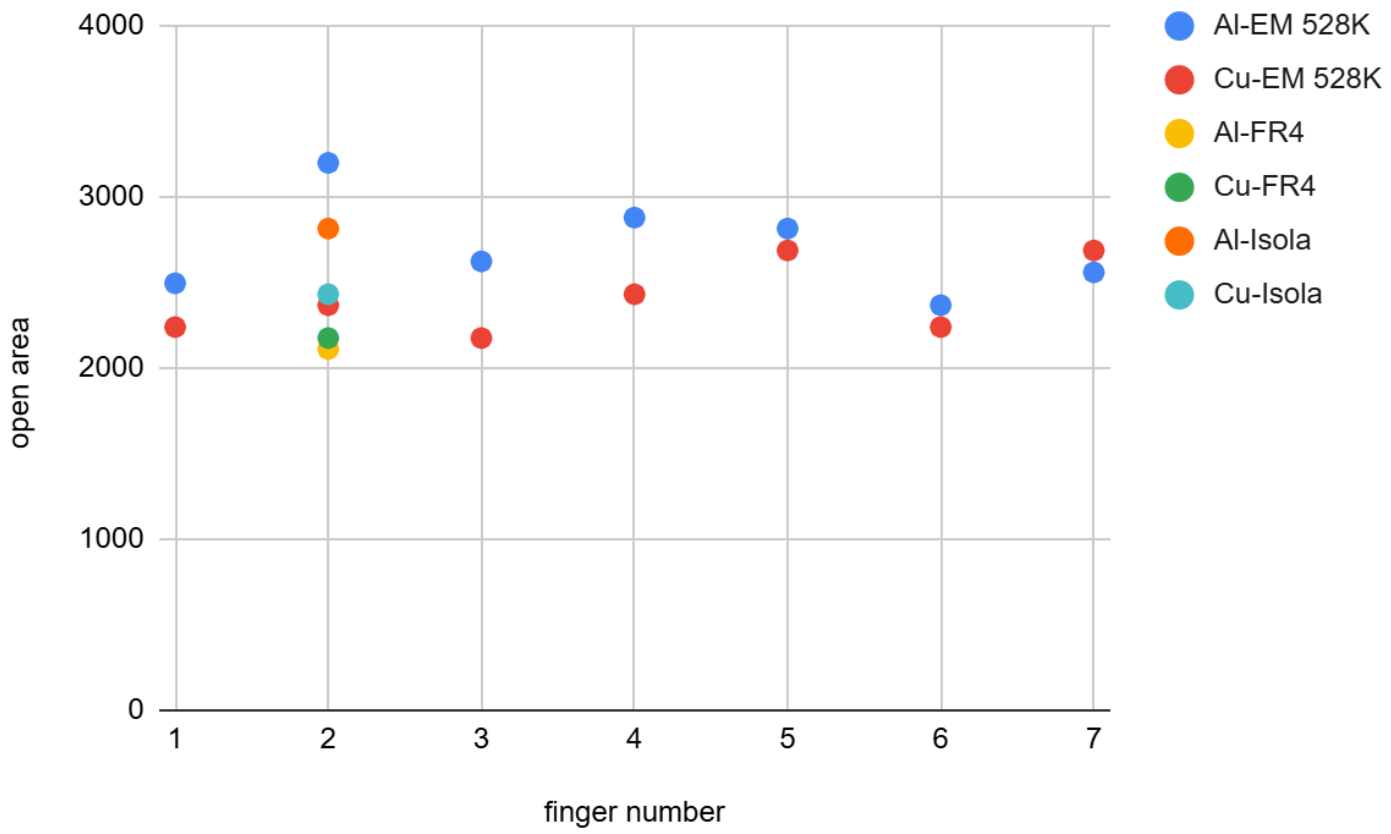


Connect two GTY port with 6 ft SMA cable



Open area : 4352

IBERT Results - Summary

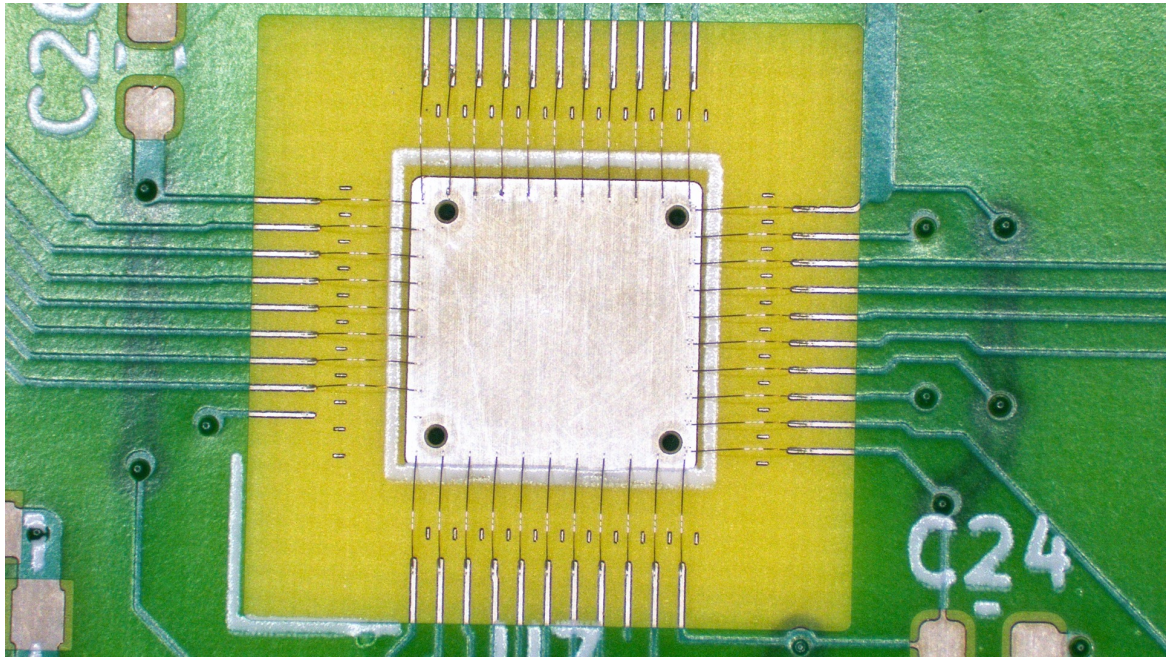


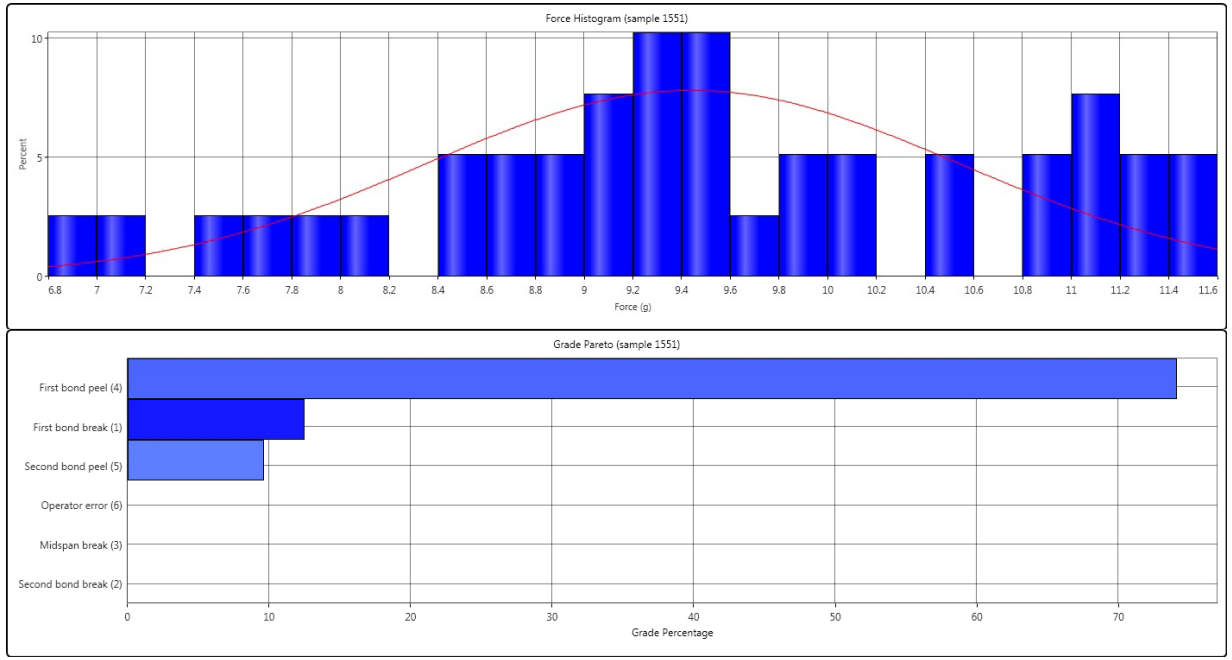
Layouts

1. 2 differential lines with gnd
2. Reference, width/space 18mil/22mil
3. No soldermask on top
4. 12 mil/14 mil
5. 24 mil/33mil
6. no soldermask on top and bottom
7. 2 differential lines without gnd on top

- ArlonEM 528K has a larger open area than FR4 and Isola

Wire-bonding and Pull Tests





- Number of tests: 39
- Mean - 3 * standard deviation: 5.7782 g
- Minimum load: 6.9011 g
- Maximum load: 11.570 g
- Mean: 9.5195 g
- Standard Deviation: 1.2471 g

Summary and Outlook

- Flexible Printed Circuit Boards need to provide good power and high-speed signal transmission properties, while keeping minimum material budgets (Al preferred). Design and prototype work on-going, with few potential vendors (LTU, OMNI).

- Several thousands pieces of FPCs, tailored separately for IB, OB, and disks, will need to be produced, tested before and after assembly, for the SVT.