

## CALOROC status

December 2025

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❑ TSMC will finish CALOROC wafers next week (Dec 12)

❑ Then will start the travel to the packaging

❑ TSMC -> IMEC -> CERN -> OMEGA -> NCAP -> OMEGA

❑ CERN is often in reduced activity from Dec 19<sup>th</sup> to Jan 5<sup>th</sup>

❑ Chinese new year Feb 17<sup>th</sup> – Mar 3<sup>rd</sup> 2026

❑ Substrate approved mid-November (manufacturer)

❑ 8 weeks to fabricate

❑ Waiting effective status

❑ ASICS testboards at OMEGA

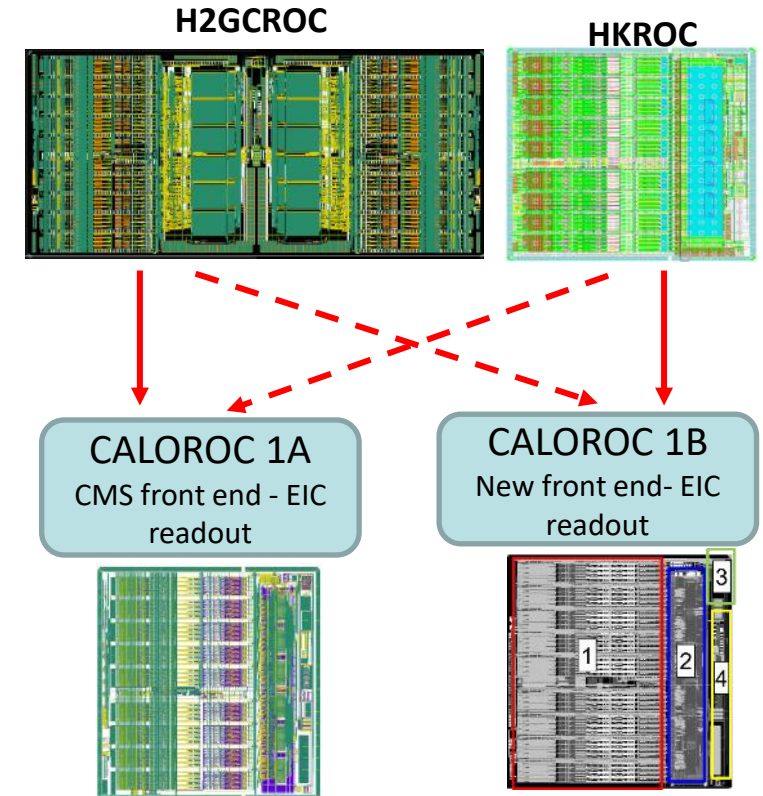
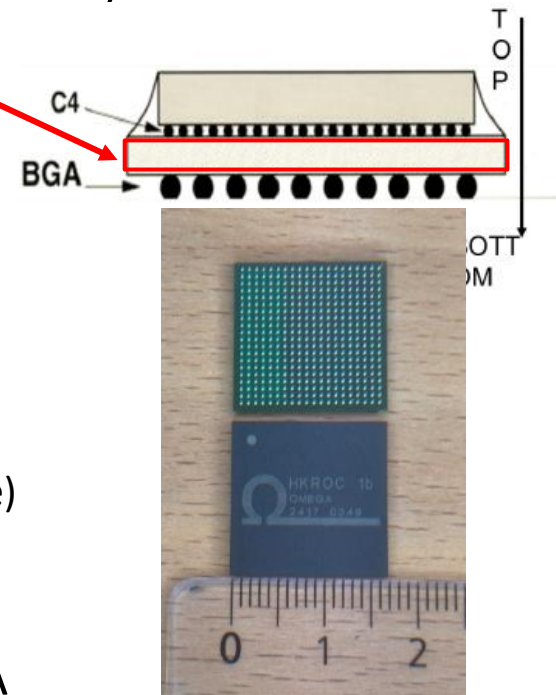
❑ EICROC 32x32 is under fabrication (started Nov 25)

❑ EICROC 4x4 + 4x32 will be sent to fab next week

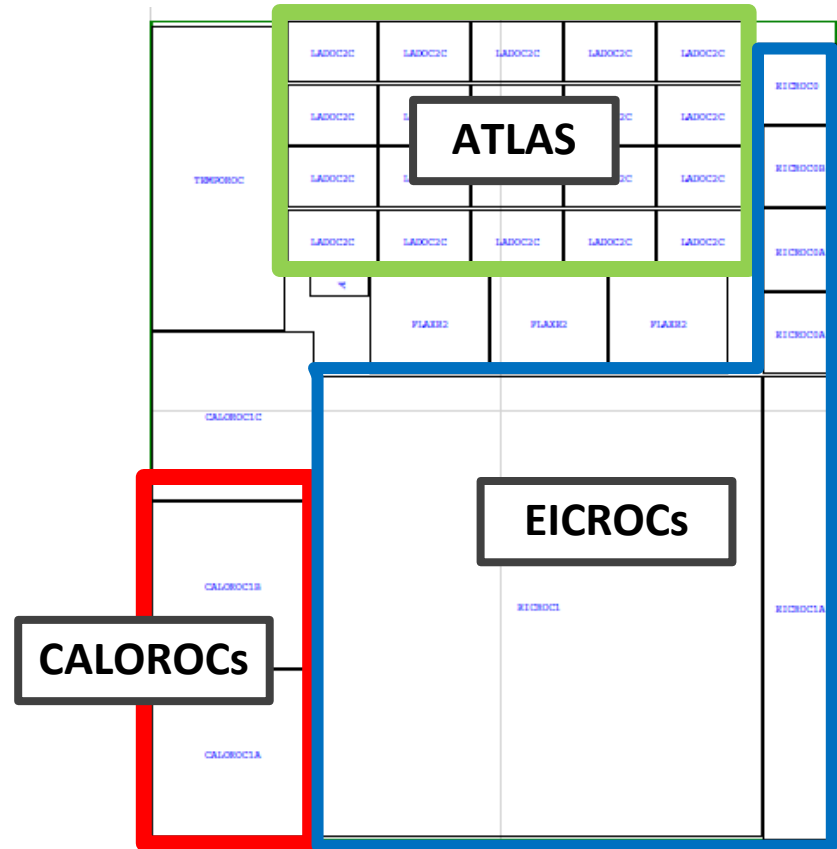
❑ Then CALOROC will be the next one (schematic done)

❑ Same testboard for CALO-A and B

❑ Targeting March for packaged ASIC at OMEGA

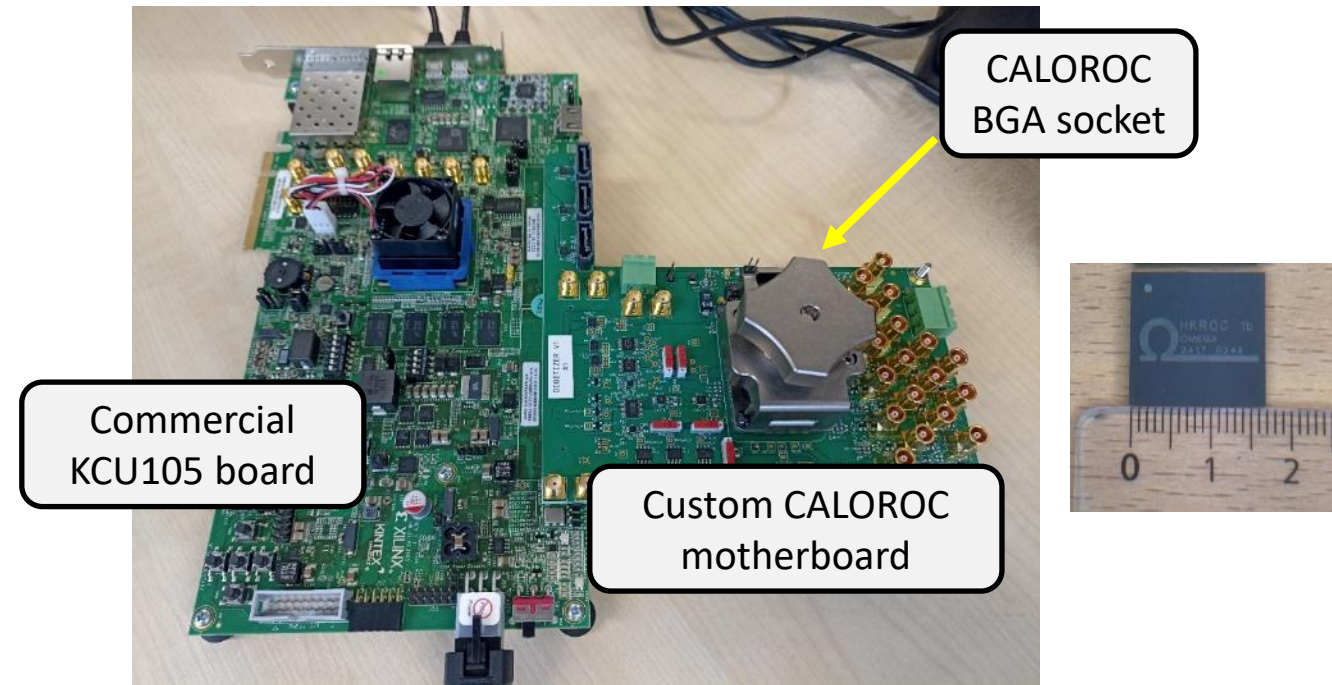


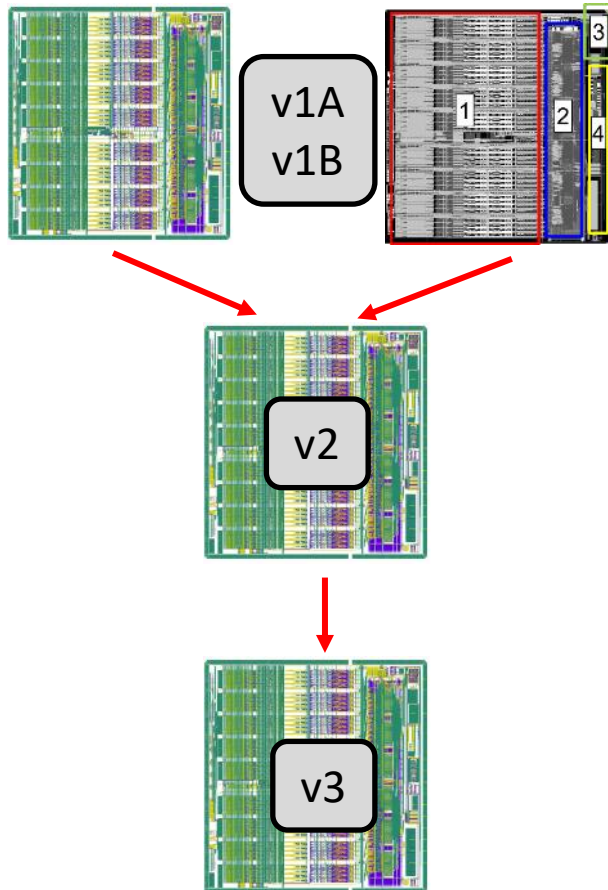






- ❑ CALOROC testboard (motherboard) design started in June
  - ❑ Prototypes v1 will be ordered **by the end of 2025**
- ❑ 1x CALOROC socket ordered and received (Sept)
  - ❑ 1 will be reused from another project
- ❑ KCU available (now at IJCLAB)





- ☐ Jan 2026: produce and distribute testboards
  - ☐ Characterization (with socket to be ordered)
  
- ☐ 2026 - Extensive tests and comparison of CALOROCs
  - ☐ End of 2026: selection on performances and system needs
  - ☐ Substrate validation
  - ☐ Same channel count
  
- ☐ 2027: Submission of selected CALOROC2
  - ☐ If needed new substrate
  - ☐ Substrate validation
  - ☐ Irradiation tests
  - ☐ Robot testboards
  
- ☐ Q2 2028: Submission of final CALOROC3
  - ☐ To be adjusted with EICROC tech node (130 vs 65 nm)