DE LA RECHERCHE À L'INDUSTRIE

www.cea.fr

Status report of the eRD109 project on SALSA chip development

Damien Neyret (CEA Saclay IRFU) for Sao Paulo University and CEA IRFU teams

EPIC DAQ/electronics WG meeting

4/12/2025

STATUS OF THE PROTOTYPES

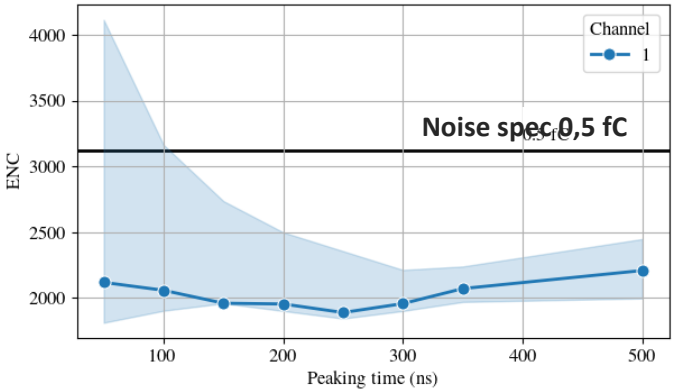
PRISMEv1 prototype (PLL test chip)

- Radiation tests foreseen in November postponed to March (BPOL12)

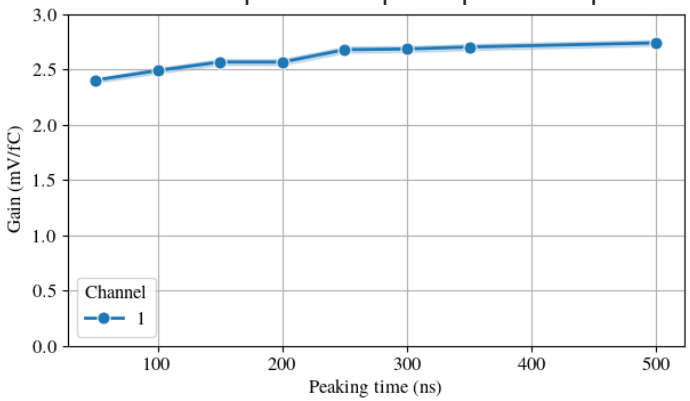
SALSA1 prototype

- Studies mostly finished
- Tests on MPGD prototypes foreseen soon
- Some last results
  - good gain and noise stability vs peaking time
  - good gain stability vs detector capacitance
- Radiation tests postponed to February

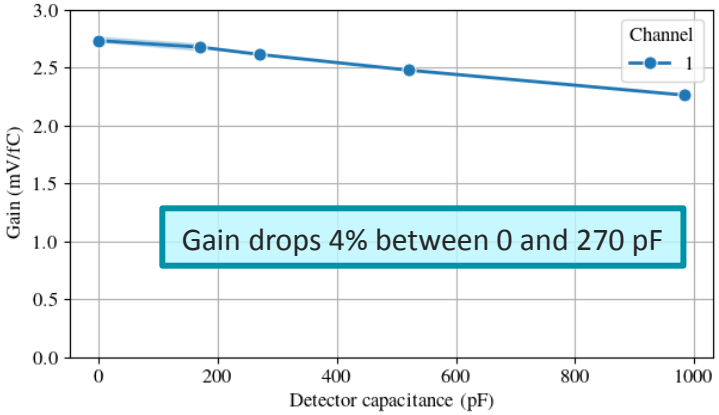
ENC vs tpeak for input capa of 170 pF



Gain vs tpeak for input capa of 170 pF



Gain vs Cdet for peaking time of 250 ns



CURRENT STATUS: SALSA2

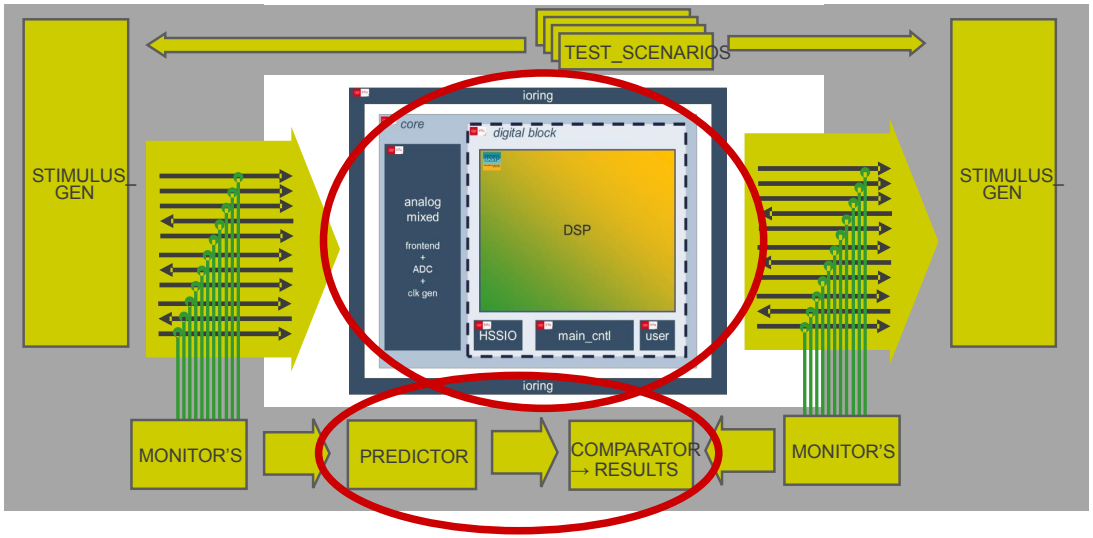
SALSA2 development status

- DSP mostly finished (with exception of modules delayed to SALSA3), integration ongoing with rest of digital environment
- Updates on multiplexer (done and tested) and high speed link (ongoing) interfaces to insure good communication between them
- Input link synchronization state machine done and tested on FPGA
- Reed-Solomon encoder and serializer of output links done and tested in simulation, to be tested on FPGA
- Work ongoing on main state machine and fast synchronous command decoding
- Clock generator to feed several modules done, tests ongoing
- Floor plan in progress, study ongoing on I/O driver behavior with BGA bumps
- UVM environment: integration of I/O ongoing

Timeline

- Still a lot of works ahead:
  - code validation ongoing
  - integration of all modules, validation
  - digital layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen 1st semester 2026
- Tests from end of 2026
- Distribution to users in 2027

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming beginning of 2026
- Beginning of SALSA2 tests → 2nd semester 2026

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 1st semester 2026
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

Very next steps

- SALSA1 tests → TID tests in February
- PRISMEv1 chip → Tests on MPGD prototypes, TID tests in March
- SALSA2 development → in progress