Discussion on pfRICH electronics

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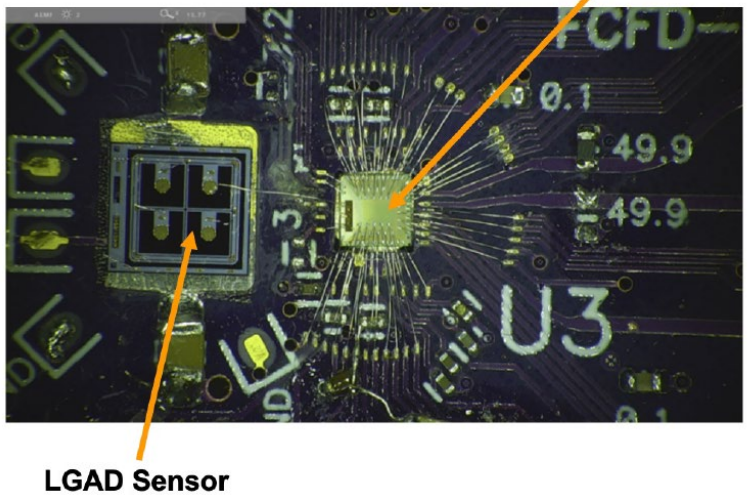
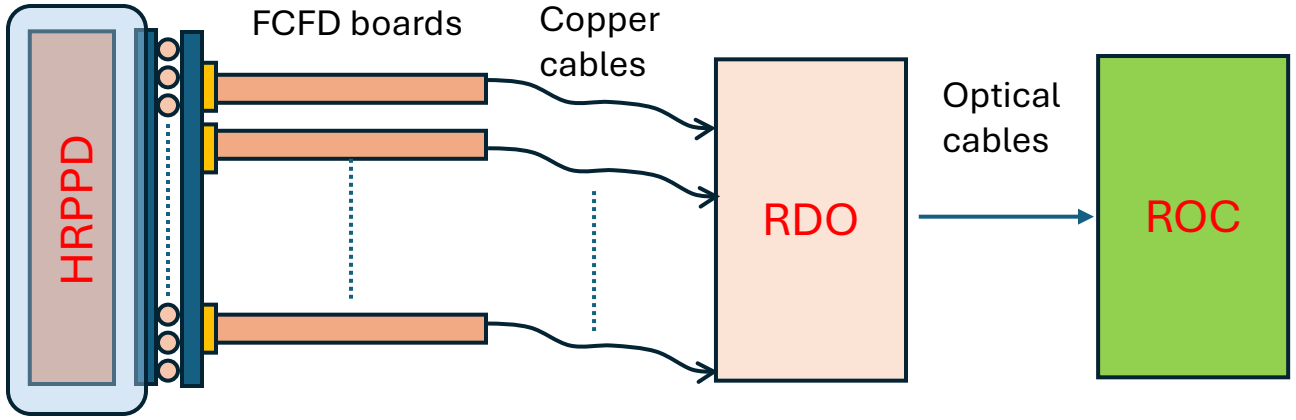
Readout Chain

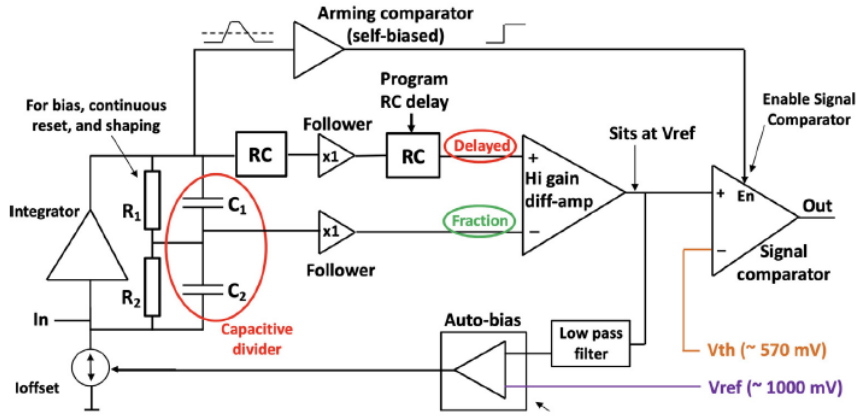
- FCFD is the candidate readout chip.
  - ADC/TDC each channel
    - TDC with CFD
  - 128 channels (in the production version)
  - Power: 2.5V and 1.2V, 2mW/ch

- Digitized output will be sent to RDO via copper cables
  - RDO send data to backend (ROC?) through optical links

From Artur's slides



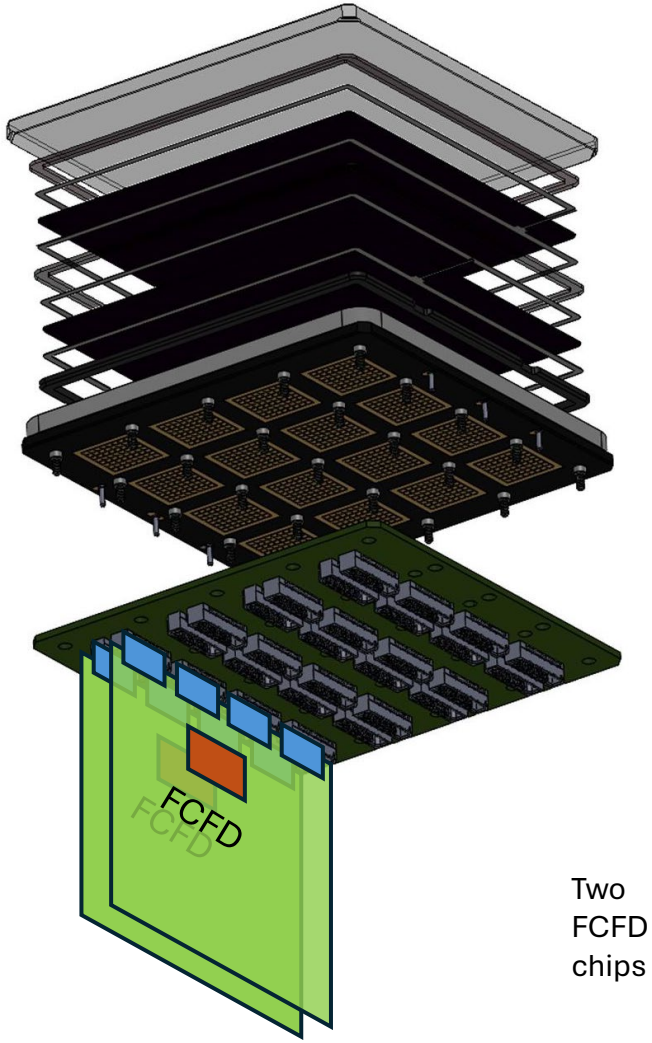


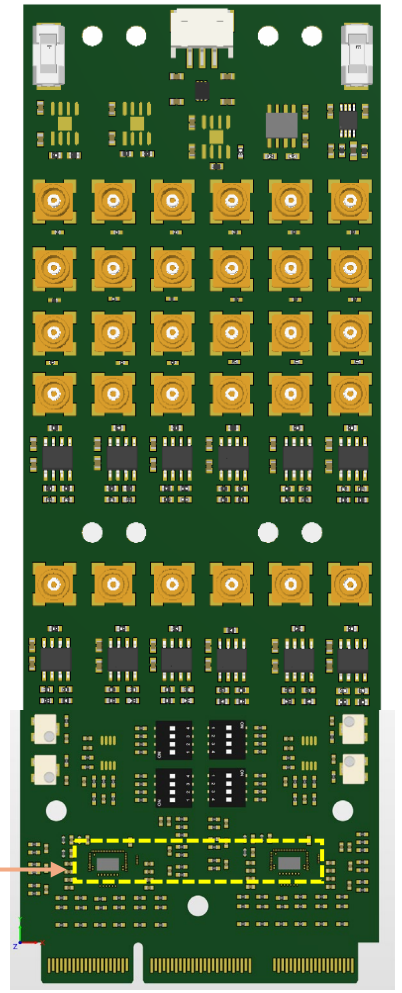


Granularity

- One HRPPD module = 1024 pads
  - 64 connectors per module for the current design
  - 32 channel per connector.
- An FCFD chip is to have 128 channels
  - One chip per board is minimum. The board will occupy 4 connectors per board (as illustrated)
  - Spanning over a row is a natural choice.
- If there is a mechanical constraint, we should ask for 64 channels version of the FCFD chip?
  - Or use the same chip, with other 64 channels are unused.
- Board configuration on a module is critical for keeping low noise and low cross-talk
  - GND side to face parts side of the other board?

FCFD test card
By Raymond





Power distribution

- FCFD chip uses 2.5V and 1.2V.
  - ~2mW/ch = 260mW/chip.
  - Assume equal power split between 2.5V and 1.2V:
    - 52mA for 2.5V, and 108mA for 1.2V
  - We need to regulate from a bit higher voltage.
  - Single voltage: ~3V → 3V*(52+108) =480mW/board
  - Dual voltages: ~3V (2.5V), ~1.8V (1.2V) → 350mW/board

- Connecting one board to one power channel is best
  - Big capacitance on cables from LV module to the board
    - Sizable time constant on turning on the LVs.
  - Resetting a board (via I^2C etc) may drop the voltage on the other boards on the same line
    - Unintentional reset of the other boards

- Lower voltage drops calls thicker cables.
  - Needs rigid mechanical design to support them.
  - Close coordination with other mechanical designs is important

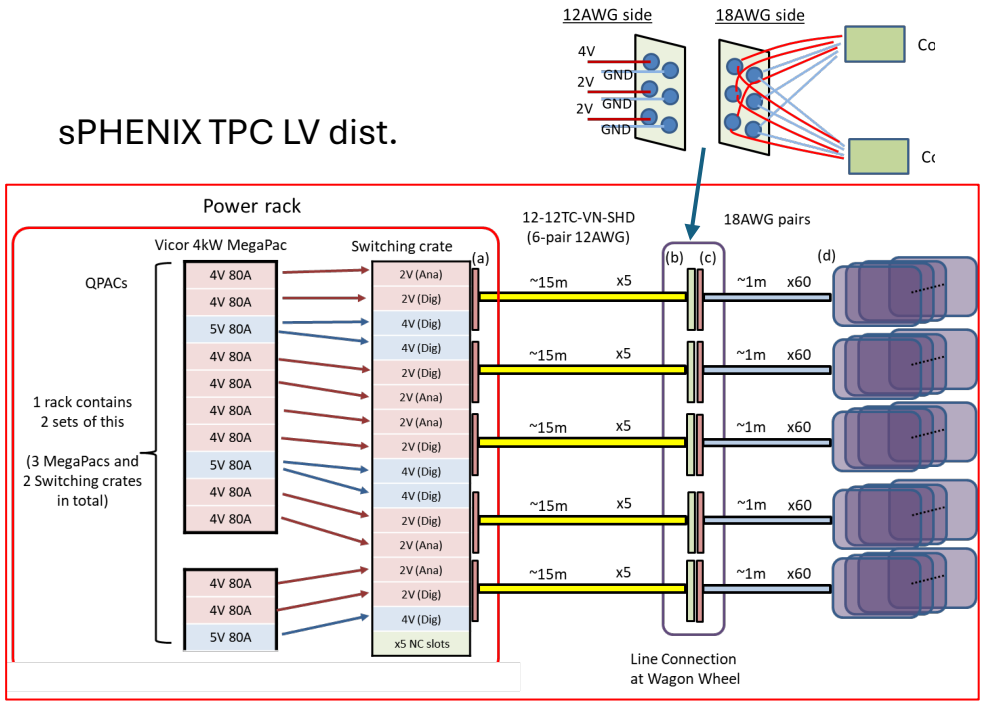
From Artur's slides

Total power

- Target power per channel:

Circuit Component	Power per Channel [mW]	Power per ASIC[mW]
Preamp + Discr (low-*high power*)	2.1 - 3.8	269 - 486
TDC+ADC	0.2	26
Supporting Circuitry	0.2	26
Global Circuitry		*200**
Total (*high power*)		521 - 738

sPHENIX TPC LV dist.



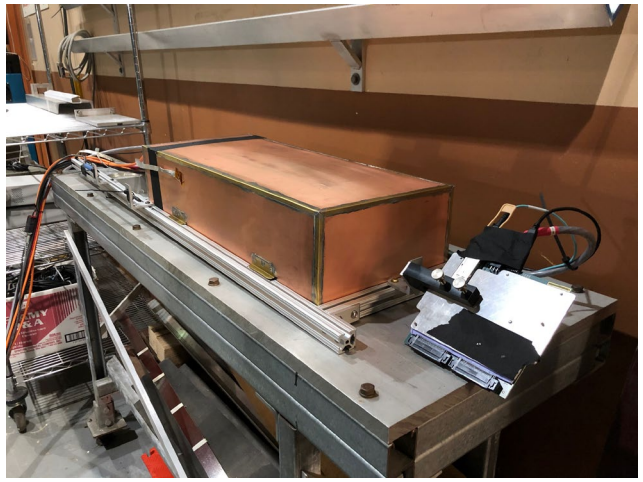
Testing parts used around FCFD

- Magnetic field test
  - Inductor is usually the parts affected by B-field
  - Optical module, DC-DC converter, etc.
  - We should use LDO to regulate powers.
  - Connectors.

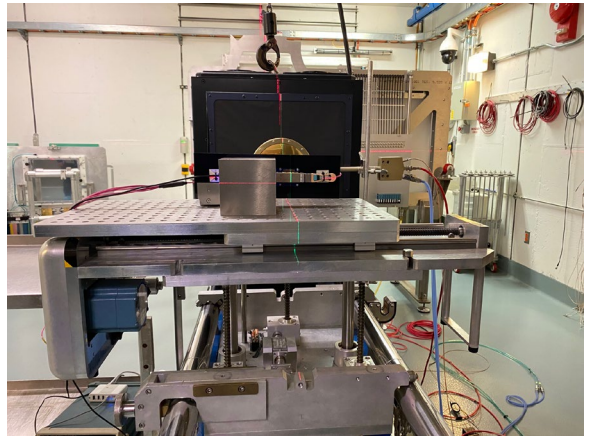
- Radiation hardness test
  - TID with gamma source: there is one in Instrumentation
  - TID with neutrons: Need to go to LANL? (LANSCE)
  - SEU with protons: Needs very high intensity beam to test. Not many places to test. LANSCE may be a candidate.

- Finding the place to test is crucial as this process takes time.
  - Early planning is important.

At superconducting magnet div.



At Instrumentation

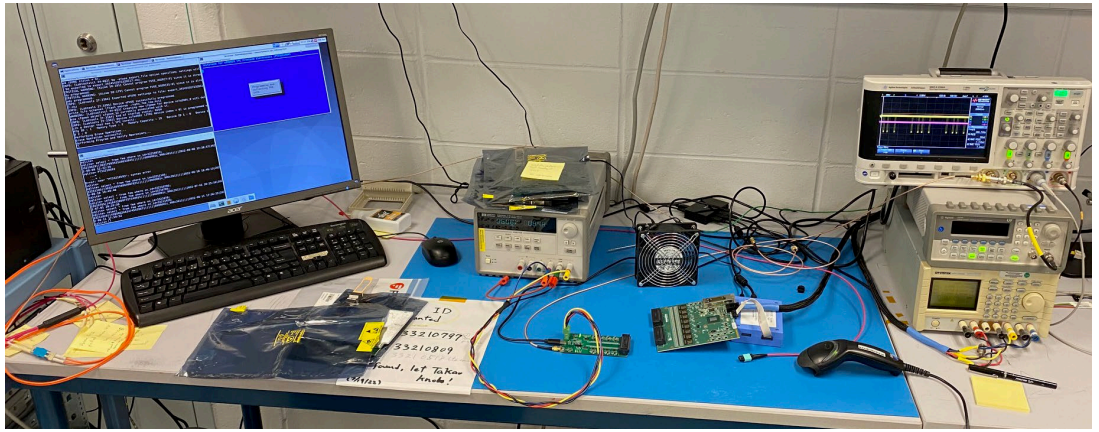


At NSRL

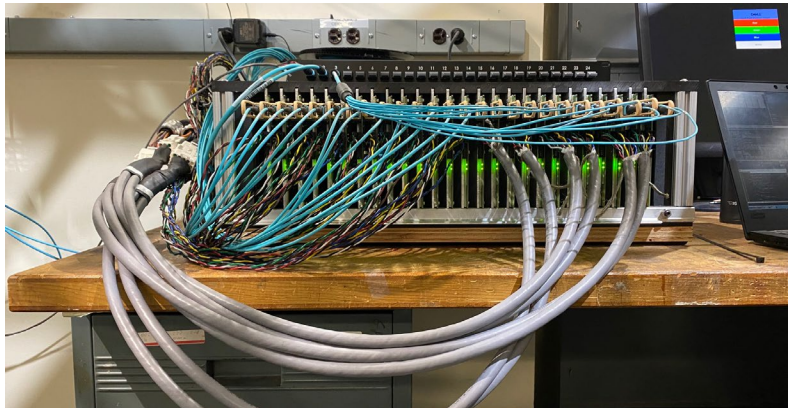
Testbench for electronics and others.

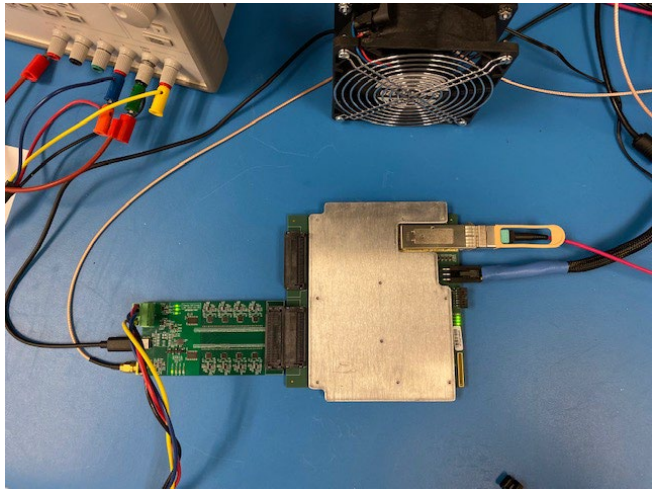
- Injecting known pulse
  - Need high slew-put pulse generator
  - Network analyzer
  - Pulse distribution/controlling board
- DAQ system currently being used is enough
- Burn-in station (for production)
  - We may want to burn ~1 month before we test boards

sPHENIX TPC testbench in physics



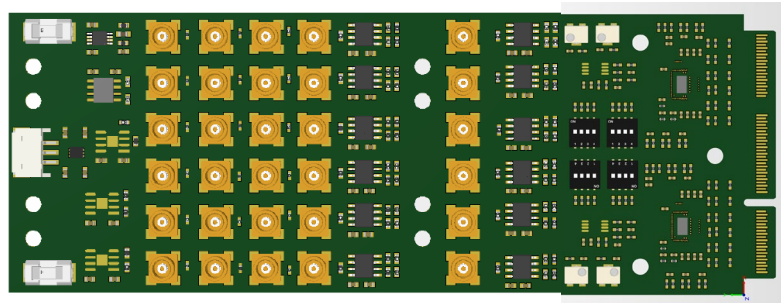
Burn-in jig at 1008





Development cycles for FCFD board

- Typical approach: three prototyping + production
  - One small-scale prototype (to come soon)
  - Two full-scale prototype
  - Pre-Production version-> Production



- FCFD is also under development
  - We could ask for additional feature if we want.
  - LED in addition to CFD?

- Fabrication and test of one prototype takes ~1-1.5 year.
  - ~5 years to close development cycle

- How many boards we should make?
  - Yield is usually 90% at best. I would set 80% for safety.
  - 20% spares will be ideal:
  - 68 tiles * 1.20 / 0.8 = 102 boards?

- Availability of parts changes a lot. We should buy enough parts whenever possible.

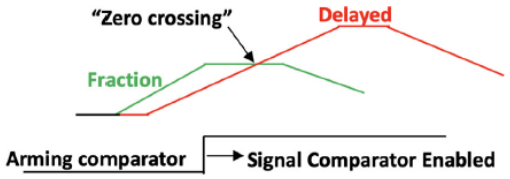
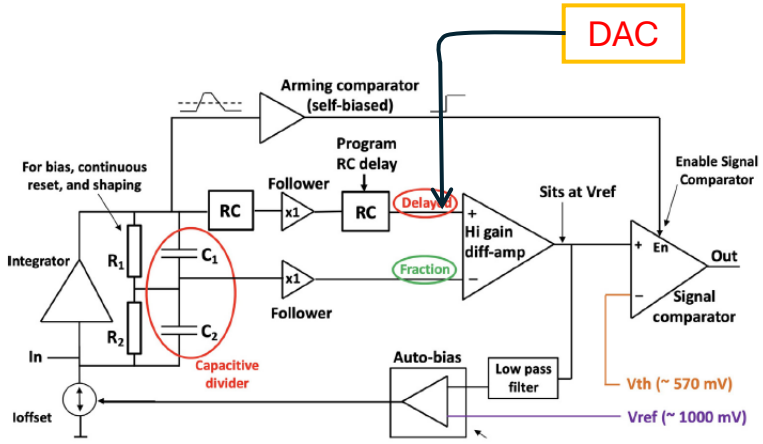


Fig. 2. Diagram showing the Zero Crossing Comparator.



Backup